Testing of Frequency Synthesizers for ZigBee Transceivers

A Project Report

submitted by

SAMEED HAMEED

in partial fulfilment of the requirements
for the award of the degree of

BACHELOR OF TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY MADRAS.

MAY 2011

THESIS CERTIFICATE

This is to certify that the thesis titled **Testing of Frequency Synthesizers for ZigBee Transceivers**, submitted by **Sameed Hameed**, to the Indian Institute of Technology Madras, for the award of the degree of **Bachelor of Technology**, is a bona fide record of the work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dr. Nagendra Krishnapura
Advisor,
Associate Professor,
Dept. of Electrical Engineering,
IIT-Madras, 600 036

Place: Chennai
Date: 27 May 2011

ACKNOWLEDGEMENTS

I am extremely grateful to Prof. Nagendra Krishnapura for guiding me through the entirety of the project. The frequent meetings with him helped clear most of my doubts. I was also attracted towards analog design due to the courses 'Analog Circuits' and 'Analog IC Design' taken by Prof. Nagendra.

I would like to thank the analog group members working in DSD Lab, TI Lab and VLSI Testing Lab for their help in making me familiar with Cadence circuit design tools and PCB design using OrCAD. I would also like to thank all my classmates, the faculty and staff at the Department of Electrical Engineering in IIT Madras for making my stay here a very enjoyable experience.

ABSTRACT

ZigBee is a wireless standard defined for low data rate applications with ultra-low power requirements. Devices based on this standard are expected to be low cost with a large battery life or use energy harvesting techniques.

As a part of a major project for developing a fully functional RF transceiver chip complying with the standard, frequency synthesizers have been designed based on integer-N phase lock loops which are expected to work as local oscillators for both the transmitter and the receiver. The standard required the PLLs to be programmable to 16 channels in the 2.4-2.5 GHz range. One of the PLLs used an LC VCO while the other used a ring VCO. This work was meant to test these PLLs to make sure that they met the specifications required of them as per the standard.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS i

ABSTRACT ii

LIST OF TABLES v

LIST OF FIGURES vii

ABBREVIATIONS viii

1 Introduction 1

1.1 PLLs as Frequency Synthesizers 1

1.2 Organization 1

2 The ZigBee Standard and an Introduction to PLLs 3

2.1 The ZigBee Standard 3

2.1.1 System Specifications 3

2.2 Phase Lock Loops 4

2.2.1 Type II PLL 5

3 Implementation of the Ring VCO 8

3.1 VCO Requirements 8

3.2 Ring VCO Architecture 8

3.3 Ring Oscillator 9

3.3.1 Differential Ring Oscillator 9

3.4 VCO Design 9

3.4.1 Choice of Delay Cell 9

3.4.2 Delay Cell Tuning 10

3.4.3 Tuning Circuit 14

3.5 Multipliers . . . 15
3.5.1 Gilbert Multipliers . . . 15
3.5.2 Output Buffer . . . 18

4 Implementation of the PLL **19**
4.1 Fixed g_m Bias Generation . . . 19
4.1.1 Basic Fixed g_m Bias Cell . . . 19
4.1.2 Improved Fixed g_m Bias Cell . . . 20
4.2 Programmable Frequency Divider . . . 21
4.2.1 Implementation of a 2/3 Divide Cell . . . 22
4.2.2 Implementation of the Divide Chain . . . 23
4.3 Differential to Single-ended Converter . . . 24
4.4 Phase Frequency Detector . . . 24
4.5 Charge Pump . . . 26

5 PCB Design and IC Characterization **27**
5.1 IC Characteristics . . . 27
5.2 IC Measurements . . . 28
5.2.1 VCO Measurements . . . 28
5.2.2 PLL Measurements . . . 33
5.3 Problems Encountered . . . 34
5.3.1 Problems with the Chip . . . 34
5.3.2 Problems with the PCB . . . 35
5.4 Conclusion . . . 35

A PCB Design **36**
A.1 PCB Schematic . . . 36
A.1.1 Frequency Synthesizer Chip Schematic . . . 36
A.1.2 Bias, References, Supply & Bypass Capacitors Schematic . . . 36
A.1.3 Control Logic Schematic . . . 37
A.1.4 Analog Inputs & Outputs Schematic . . . 37
A.2 PCB Layout . . . 42

LIST OF TABLES

5.1 Observed k_{vco} Values for the Ring VCO 33

LIST OF FIGURES

2.1 ZigBee Transmitter 3
2.2 ZigBee Receiver 4
2.3 Type II PLL Block Diagram 5
2.4 Type II PLL Loop Gain Bode Plot 6

3.1 Ring VCO Architecture 9
3.2 Four Stage Ring Oscillator 9
3.3 Differential Delay Cells 10
3.4 Delay Cell with Replica Bias 11
3.5 Schematic of the Delay Cell 12
3.6 Schematic of the Op-amp 13
3.7 Magnitude Response of the Op-amp 13
3.8 Schematic of the Tuning Circuit 14
3.9 Characteristics of the Tuning Circuit 15
3.10 Basic Gilbert Cell 16
3.11 Block Diagram of a Symmetric Multiplier 16
3.12 Active Inductor Realization 17
3.13 Active Inductor Small Signal Equivalent 17
3.14 Schematic of the Symmetric Multiplier 18
3.15 Schematic of the Output Buffer 18

4.1 Basic Fixed g_m Bias Cell 19
4.2 Schematic of the Improved Fixed g_m Bias Cell 20
4.3 Schematic of the Op-amp used in Fixed g_m Bias Cell 21
4.4 Programmable divider Implementation 22
4.5 2/3 Divide Cell Implementation 22
4.6 Schmatic of the CML Latch with an Embedded AND Gate 23
4.7 Schmatic of Differential to Single Ended Converter 24

4.8 Block Diagram of the PFD 25
4.9 Schematic of the TSPC D flip-flop 25
4.10 Schematic of the Charge Pump 26

5.1 Layout of the Chip 27
5.2 Measurement Screenshot 28
5.3 PCB for Testing the VCOs 29
5.4 Measured Ring VCO Tuning Characteristics for (V_{dd},V_{ref})=(1.8V,1.3V) 30
5.5 Measured Ring VCO Tuning Characteristics for (V_{dd},V_{ref})=(1.7V,1.3V) 30
5.6 Measured Ring VCO Tuning Characteristics for (V_{dd},V_{ref})=(1.875V,1.3V) 31
5.7 Measured Ring VCO Tuning Characteristics for (V_{dd},V_{ref})=(1.9V,1.3V) 31
5.8 Measured Ring VCO Tuning Characteristics for V_{ref}=1.3V 32
5.9 Measured Ring VCO Tuning Characteristics for V_{dd}=1.8V 32
5.10 PCB for Testing the PLL with the Ring VCO 34

A.1 Frequency Synthesizer Chip Schematic 38
A.2 Bias, References, Supply & Bypass Capacitors Schematic 39
A.3 Control Logic Schematic 40
A.4 Analog Inputs & Outputs Schematic 41
A.5 Layout of PCB TOP Layer 42
A.6 Layout of PCB BOTTOM Layer 43

ABBREVIATIONS

PLL	Phase Lock Loop
VCO	Voltage Controlled Oscillator
PFD	Phase Frequency Detector
PCB	Printed Circuit Board
CML	Current Mode Logic
PFD	Phase Frequency Detector
CP	Charge Pump
IC	Integrated Circuit
PTAT	Proportional to Absolute Temparature

CHAPTER 1

Introduction

1.1 PLLs as Frequency Synthesizers

The frequency synthesizer is one of the most important parts of a wireless communication system using coherent demodulation techniques. The frequency of the local oscillator must be set to a high level of precision. Hence, an open loop oscillator is not a suitable candidate as the frequency cannot be controlled precisely and so other methods of clock generation are required.

One possibility is to use a fully digital frequency synthesizer whose frequency can be accurately controlled by digital logic. However due to the ultra low power nature of the application, this option is also not viable since the power consumption at high frequencies becomes prohibitively large. A phase lock loop (PLL) is thus the perfect solution as it allows the frequency to be controlled accurately and is also comparitively low power. A PLL is a negative feedback system with a low-frequency crystal oscillator at the input and a frequency divider circuit in feedback. The frequency of the output is approximately the input frequency times the divider value in the feedback loop.

1.2 Organization

Chapter 2 introduces the ZigBee standard and its transceiver and also covers some of the basics of Phase Lock Loops. Specifications of the frequency synthesizer are also considered.

Chapter 3 gives the details of the circuit implementation of ring VCO.

Chapter 4 discusses the implementation of the other parts of the PLL such as the loop filter, the phase frequency detector (PFD) and the frequency divider.

Chapter 5 presents details regarding the printed circuit board (PCB) design, prototype IC characterization and measured results.

CHAPTER 2

The ZigBee Standard and an Introduction to PLLs

2.1 The ZigBee Standard

'ZigBee' (officially 'IEEE 802.15.4') was a standard developed for building low-data rate wireless transceivers with an emphasis on very low power consumption. It was developed as a wireless standard for Wireless-Personal Area Networks working at data rates upto 250 kbps. Typical operational range of target appliances is around 10 metres. It can be easily incorporated into devices used in home automation, PC peripherals and health care appliances.

2.1.1 System Specifications

The basic block diagrams of the transceiver sections are shown below.

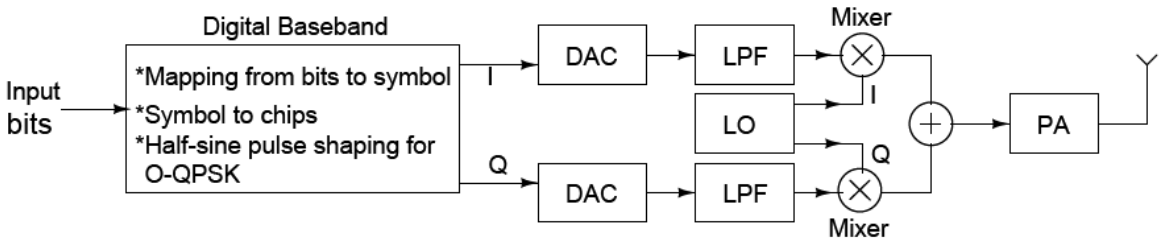


Figure 2.1: Block diagram of a ZigBee transmitter

The modulation scheme used here is O-QPSK with sine pulse shaping. Transmit data rate is 250 kbps and a spread factor of 1:8 is applied, so the chip rate going in is actually 2 Mcps. The channel bandwidth is approximately 2 MHz. The band extends from 2.405 GHz to 2.480 GHz with 16 channels spaced at 5 MHz each.

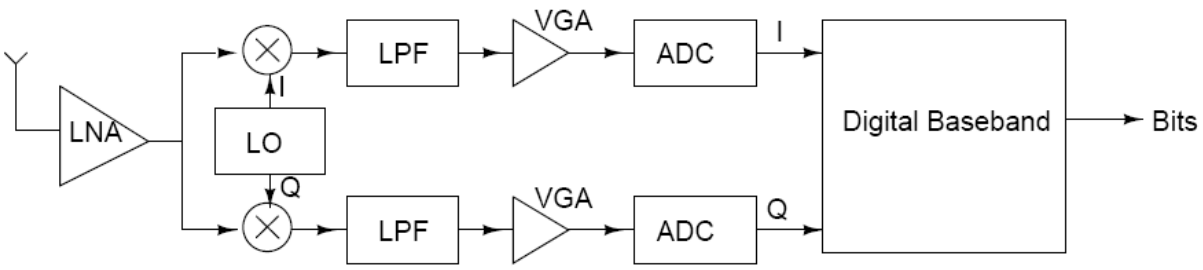


Figure 2.2: Block diagram of a ZigBee receiver

As far as the PLL is concerned, the relevant specifications are:

- The settling time must be less than $192\mu s$.
- The final settling value must have an accuracy of ± 40 ppm. Hence with a center frequency of around 2.5 GHz, the maximum allowed frequency deviation is ± 100 kHz.
- Phase noise must be below -92 dBc/Hz at an offset of 3.5MHz from the carrier.
- Additional constraints posed by the trasmit mask in the band and receiver noise considerations.

2.2 Phase Lock Loops

The PLL is a block that locks the frequency and phase of a locally generated signal to a reference signal. It is a negative feedback loop which tends to make the phase error between the fed back output signal and the reference signal zero. By placing a programmable frequency divider in the feedback loop, one can generate any frequency which is a multiple of the reference frequency. An integer-N PLL ('N' denotes the divide value used in the programmable divider) use integer values for the programmable frequency divider. The basic blocks in an integer-N PLL are the Voltage Controlled Oscillator(VCO), programmable divider, phase detector and the loop filter.

2.2.1 Type II PLL

A type II PLL consists of two integrators in the feedback loop, one due to the VCO and the other due to the loop filter. This ensures that the phase error goes to zero while a type I PLL can only ensure that the frequency error goes to zero. However, additional zeros have to be added to the loop gain to stabilize the loop. The general block diagram of a type II PLL is given below: With phase as the variable, the small signal loop gain

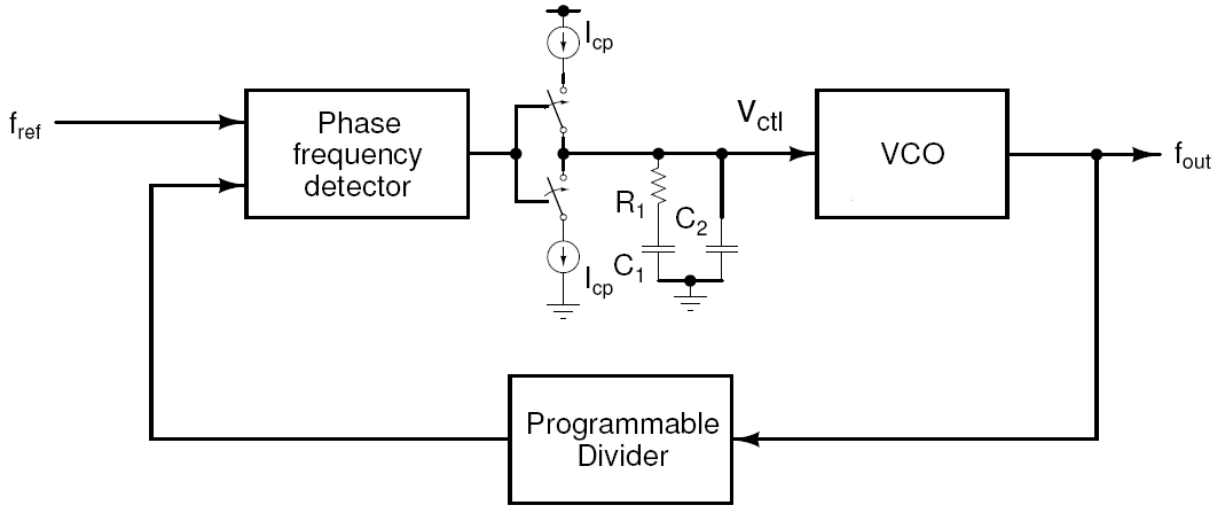


Figure 2.3: Block diagram of a type II PLL

in this case is given by

$$L(s) = \left(k_{PD} + \frac{k_{PD,i}}{s}\right)\left(\frac{1}{1+\frac{s}{p_1}}\right)\left(\frac{2\pi k_{vco}}{s}\right)\left(\frac{1}{N}\right)$$

where k_{vco} is the gain of the VCO, N is value of the frequency divider and $\left(k_{PD} + \frac{k_{PD,i}}{s}\right)$ is the tranfer function of the phase detector and loop filter. In this case, $k_{PD} = \frac{I_{cp}R}{2\pi}$ and $k_{PD,i} = \frac{I_{cp}}{2\pi C_1}$ as shown in [1]. Hence the two poles of the loop gain are at 0 while the zero is at $-z_1 = -\frac{1}{RC_1}$ which means that the loop bandwidth $\omega_{u,loop} = k_{vco}\frac{I_{cp}R}{N}$. The capacitor C_2 adds another pole at $-p_1 = -\frac{C_1+C_2}{RC_1C_2}$. For the loop to be stable, $z_1 < f_{u,loop} < p_1$. For the spurious components to be further attenuated, $f_{u,loop} < p_1 < f_{ref}$.

The bode plot of the loop gain is shown below:

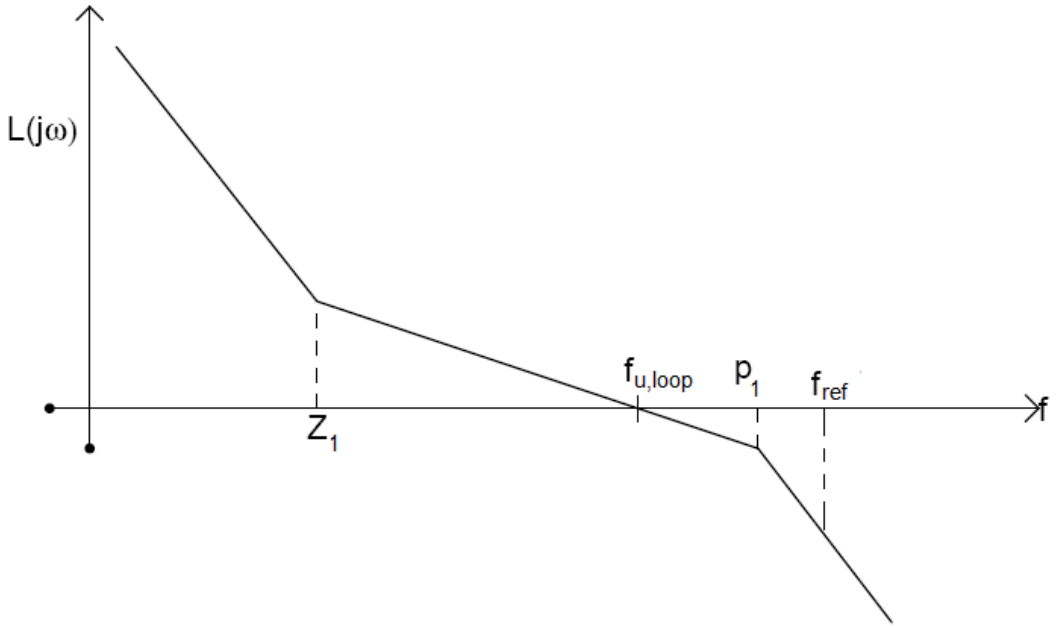


Figure 2.4: Type II PLL Loop Gain Bode Plot

The closed loop gain G(s) is given by

$$G(s) = N\frac{1}{1+\frac{1}{L(s)}} = N\frac{1}{1+\frac{Ns^2\left(1+\frac{s}{p_1}\right)}{k_{vco}I_{cp}\left(sR+\frac{1}{C_1}\right)}}$$

This gives

$$G(s) = N\frac{k_{vco}I_{cp}\left(sR+\frac{1}{C_1}\right)}{k_{vco}I_{cp}\left(sR+\frac{1}{C_1}\right)+Ns^2\left(1+\frac{s}{p_1}\right)}$$

For the condition of $p_1 >> f_{u,loop}$ and on simplifying,

$$G(s) = N\frac{(sRC_1+1)}{s^2\frac{NC_1}{k_{vco}I_{cp}}+sRC_1+1}$$

Comparing this with the denominator of the standard biquad transfer function $\left(\frac{s^2}{\omega_0^2}+\frac{s}{Q\omega_0}+1\right)$ we get

$$\omega_0 = \sqrt{\frac{k_{vco}I_{cp}}{NC_1}}$$

$$Q = \frac{1}{R}\sqrt{\frac{N}{k_{vco}I_{cp}C_1}}$$

The settling time (T_s) can be calculated by the fact that the response to a step will be an exponential with time constant $\frac{2Q}{\omega_0}$. According to the specifications, the final value should settle to within $\pm 0.004\%$ (to satisfy the ± 40 ppm constraint) of the ideal value. Hence

$$e^{-\frac{\omega_0 T_s}{2Q}} = 4 \times 10^{-5}$$

$$\Rightarrow T_s = 10.126 \left(\frac{2Q}{\omega_0} \right) = \frac{20.252N}{k_{vco} I_{cp} R}$$

CHAPTER 3

Implementation of the Ring VCO

The VCO is one of the most important parts of the PLL and serves as a voltage to frequency converter. The factors governing VCO design are the frequency tuning range, phase noise limit, power and area occupied.

3.1 VCO Requirements

ZigBee uses O-QPSK as its modulation scheme, which needs both in-phase(I) and quadrature(Q) components. Hence, the choice of VCO is influenced by the ability to produce I and Q signals. Another concern is that the transmitted signal can be coupled to the receiver input and be fed back to the frequency synthesizer through the LNA and mixers, due to finite isolation between different ports of each block (even if the receiver is off) as mentioned in [2]. To reduce the sensitivity of the frequency synthesizer to the modulated transmit signal leaking back into it, it is better if the oscillator is not operating in the transmitted signal band.

3.2 Ring VCO Architecture

The VCO contsists of a ring oscillator operating at a frequency of 1.25 GHz followed by two multipliers to multiply quadrature signals at 1.25 GHz and produce a signal at 2.5 GHz. Again the signals produced by the multipliers are in quadrature(90^0 apart in phase).

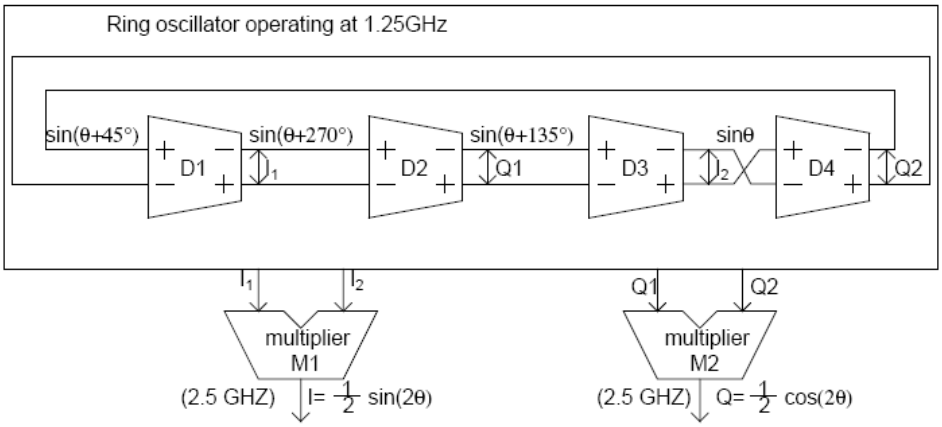


Figure 3.1: Ring VCO Architecture

3.3 Ring Oscillator

3.3.1 Differential Ring Oscillator

A ring oscillator consists of a number of gain stages in a loop. Single ended rings are limited to an odd number of delay stages making them incapable of providing quadrature outputs. As a result differential ring oscillators are the only choice for systems which require quadrature signals. Differential implementations can also utilize even number of stages by simply configuring one stage such that it does not invert. With a four stage differential ring oscillator, quadrature signals can be produced easily.

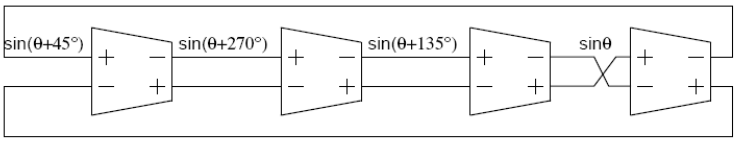


Figure 3.2: Four Stage Ring Oscillator

3.4 VCO Design

3.4.1 Choice of Delay Cell

Differential delay cells are of two types:

1. Full swing delay cells
2. Partial swing delay cells

Full swing delay cells are basic inverters with some positive feedback to make the rail to rail transitions sharp so that the output is rail to rail and looks like a square wave. Fast transitions and rail-to-rail swing, cause the full swing ring oscillator to reject intrinsic noise better than a partial swing ring oscillator. Partial swing delay cells have smaller voltage swing and slow transitions leading to poor intrinsic noise rejection, but have a higher power supply rejection capability than full swing oscillators. They are also more practical to implement due to higher bandwidth and higher power supply noise rejection.

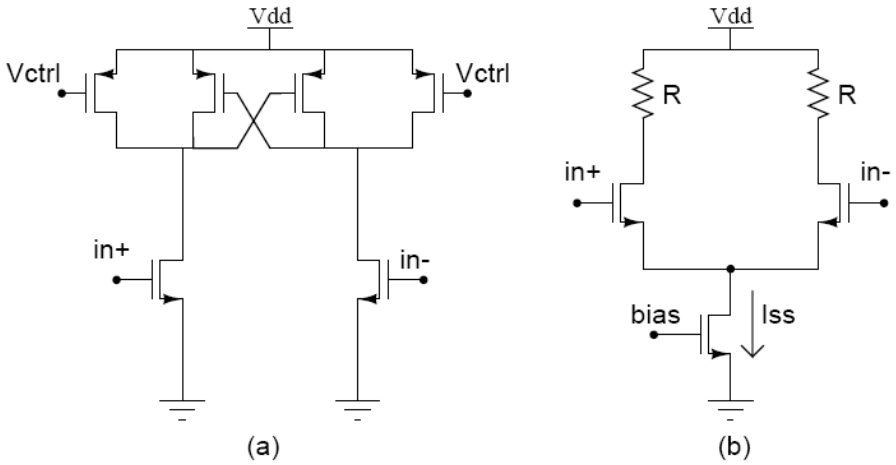


Figure 3.3: Differential Delay Cells (a) Full Swing Delay Cell (b) Partial Swing Delay Cell

Because of lack of high quality resistors in CMOS technologies the the partial swing delay cell shown above is not suitable for practical implementation. Most of the practical delay-cells use PMOS transistors operating in deep triode region as the loads.

3.4.2 Delay Cell Tuning

The oscillation frequency of an N-stage ring oscillator with a large signal delay of T_d per stage is given by

$$f_{osc} = \frac{1}{2NT_d}$$

Hence, the frequency can be tuned by changing T_d which is given by $T_d = \frac{C_L V_{SW}}{I_{SS}}$ where V_{SW} is the voltage swing at the output of the delay cell, C_L is the load capacitance and I_{SS} is the tail current. Thus T_d can be changing either by changing the load resistance (thus varying V_{SW}) or changing the tail current. Load resistance can be varied by changing the gate or drain voltage of the PMOS transistors. However, this can lead to a large VCO gain which affects PLL stability. Hence varying the tail current is the better option.

To decrease amplitude variation with tuning, the following topology was used. The PMOS transistors should be biased in the deep triode region for better linearity while the NMOS transistors should always be in saturation.

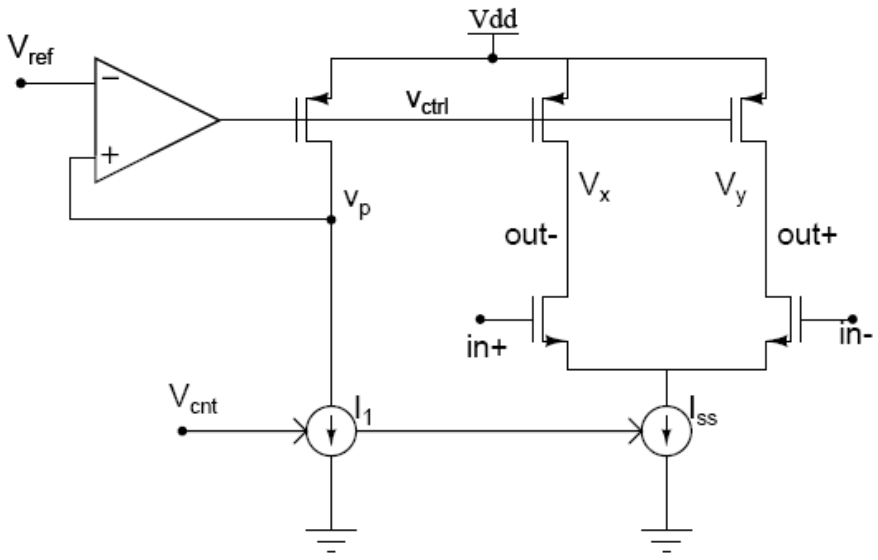
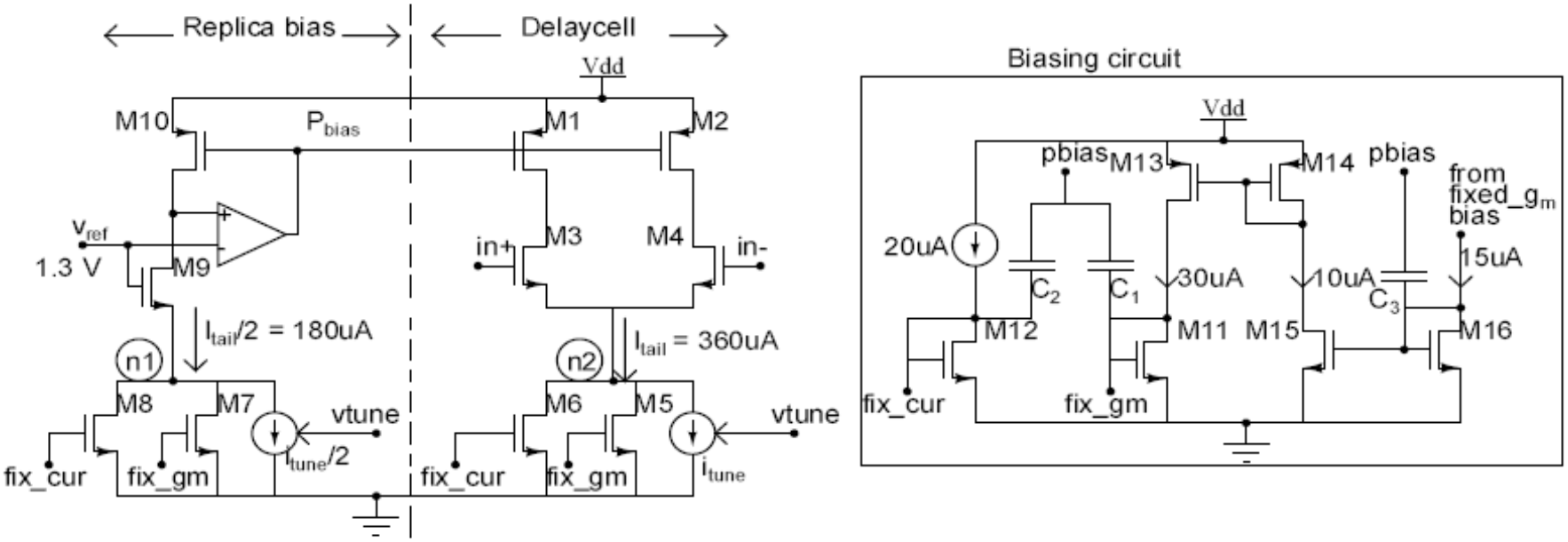


Figure 3.4: Delay Cell with Replica Bias

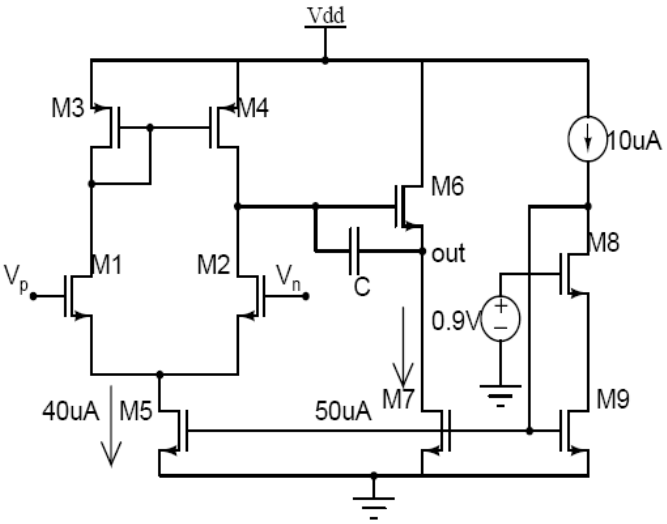
If R_{on} is the on resistance of the PMOS load, then with complete switching each stage provides a differential output swing of $2I_{ss}R_{on}$. So the circuit needs a constant $I_{ss}R_{on}$ product through out the tuning range to maintain a constant output swing. This can be achieved by the topology shown above. The negative feedback loop formed by the op-amp makes the voltage at node v_p always equal to V_{ref}. Therefore any increase in tail current causes the gate voltage of PMOS device to decrease because of fixed drain to source voltage which decreases the on resistance of the PMOS. The schematic of the delay cell from [3] is given below for reference.



M1 = M2 = (8)* 0.96u/0.3u	M5 = (16)* 1.5u/2u	M11 = (2) * 1.5u/2u	M16 = 6 * (0.25u/2u)
M3 = M4 = (8)* 1.23u/0.3u	M6 = (8)* 1u/2u	M12 = (2) * 1u/2u	M15 = 4 *(0.25u/2u)
M10 = (4)* 0.96u/0.3u	M7 = (8)* 1.5u/2u	M14 = (4) * 0.5u/1u	C1 = 1pF C2 = 0.3pF
M9= (8)* 2u/0.25u	M8 = (4)* 1u/2u	M13 = (12) * 0.5u/1u	C3 = 1pF

Figure 3.5: Schematic of the Delay Cell

The op-amp used for replica biasing forms a negative feedback circuit which maintains the drain voltage of the PMOS load at the appropriate value. The only constraint on its design is that its bandwidth should be greater than the PLL's which is easily achieved. The schematic and magnitude response of the op-amp is shown below.



M1 = M2 = (4) * 1.2u/0.9u	M5 = (16) * 1.25u/0.3u
M3 = M4 = (8) * 1u/0.3u	M7 = (20) * 1.25u/0.3u
M6 = (2) * 2u/1.8u	M9 = (4) * 1.25u/0.3u
M8 = (2) * 1.5u/0.6u	C=500fF

Figure 3.6: Schematic of the Op-amp

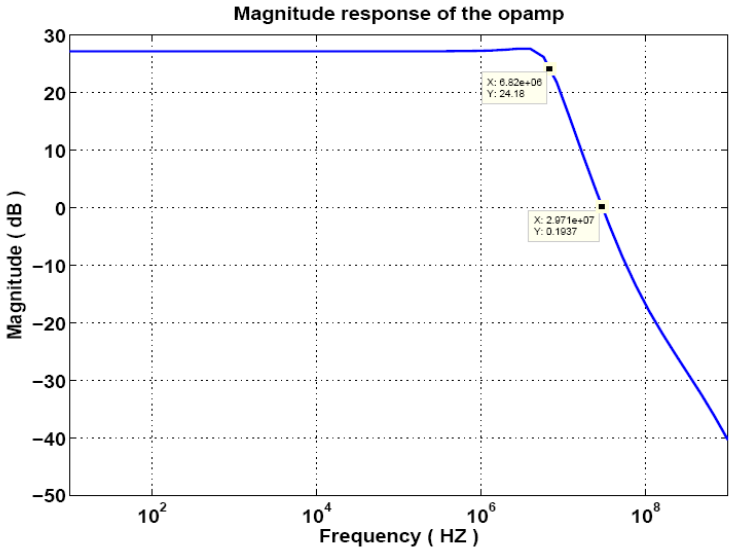


Figure 3.7: Magnitude Response of the Op-amp

3.4.3 Tuning Circuit

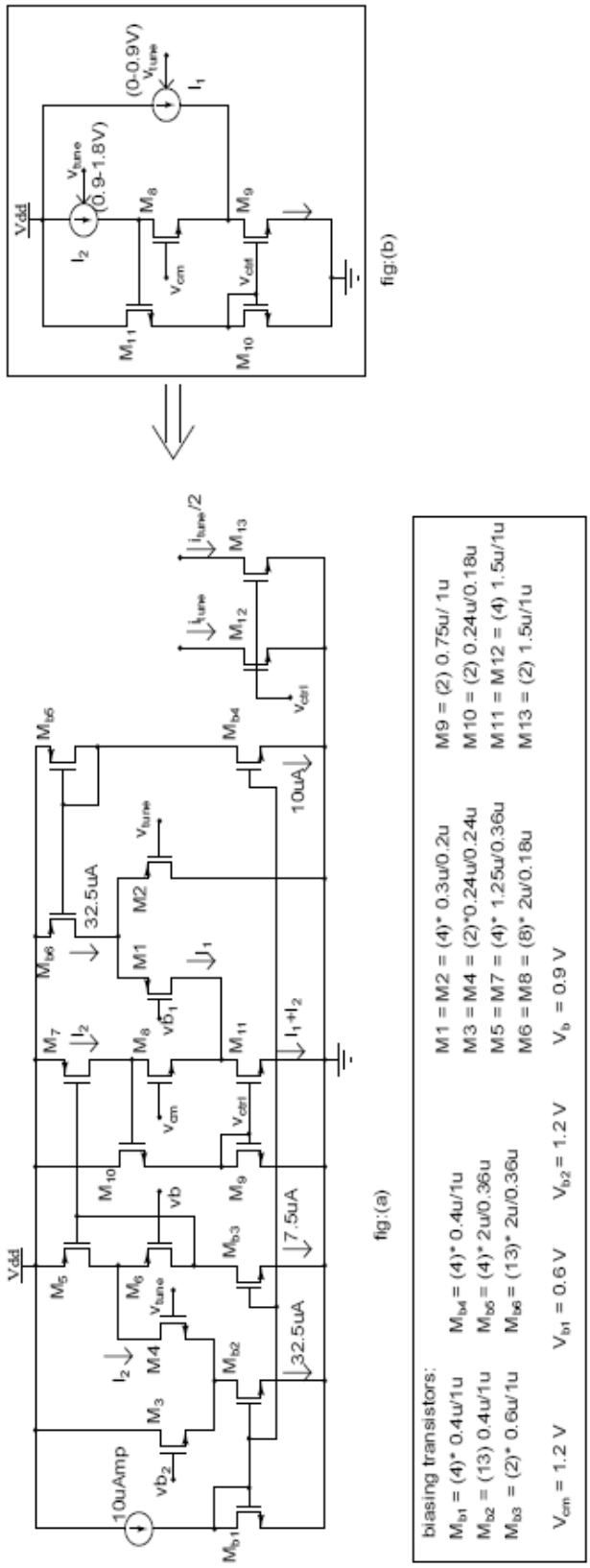


Figure 3.8: Schematic of the Tuning Circuit

The schematic of the tuning circuit is shown above. It is basically a linear voltage to current converter. The current I_1 varies linearly with respect to tuning voltage (v_{tune}) in the range of 0 to 0.9V. This is realized by the PMOS differential pair (M1, M2). I_2 varies linearly with respect to v_{tune} in the range of 0.9V to 1.8V. This is realized by the NMOS differential pair (M3, M4). Therefore the total current I_1+I_2 flows through M11 varies linearly with respect to tuning voltage in the range of 0V to 1.8V. This current is replicated to the tail current of the delay cell.

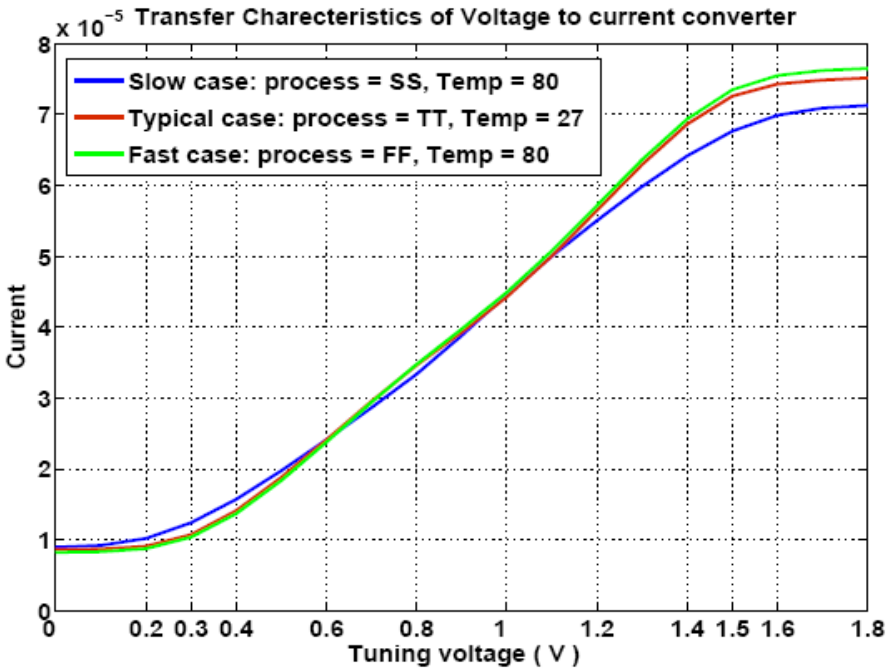


Figure 3.9: Characteristics of the Tuning Circuit

3.5 Multipliers

3.5.1 Gilbert Multipliers

Gilbert multipliers are used to obtain quadrature signals from the outputs of the various stages of the ring oscillator. A simple gilbert cell used for this multiplication is shown below which is equivalent to a CML XOR gate. On applying two signals with the same frequency with one haveing a quarter cycle delay an output with a frequency twice that of input signals is obtained. This circuit has two problems:

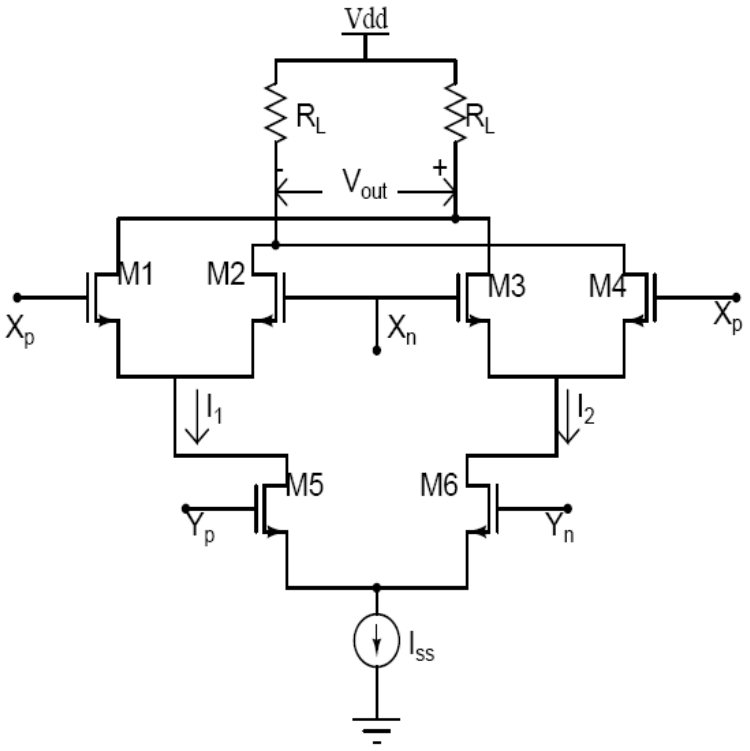


Figure 3.10: Basic Gilbert Cell

- Unequal rise and fall times at the output. This can result in unsymmetrical output with respect to the output common mode voltage.
- Unequal load seen by the input signals of the multiplier. This can lead to unequal phase shifts in different stages of the ring oscillator.

These problems can be solved by using a symmetrical multiplier architecture as shown below.

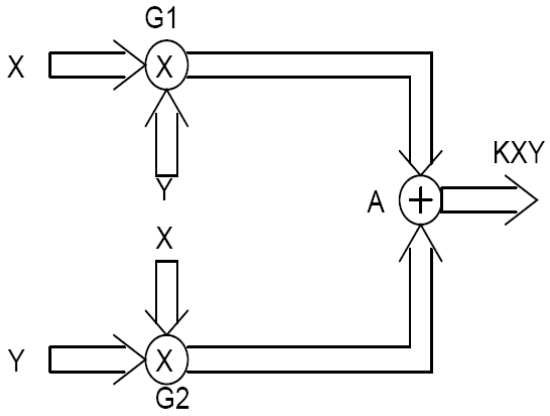


Figure 3.11: Block Diagram of a Symmetric Multiplier

To increase the bandwidth of the cells, an inductor can be added in series with the resistance. The Q of the inductors can be small since the series resistance can be incorporated into the load resistance. The ideal solution is thus an active-inductor realization with a single MOS transistor.

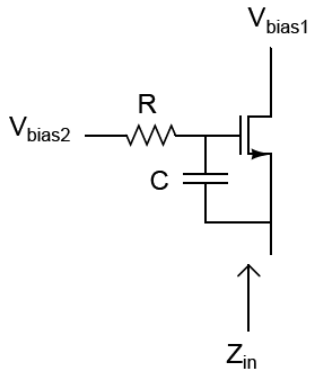


Figure 3.12: Active Inductor Realization

The small signal equivalent of the circuit is

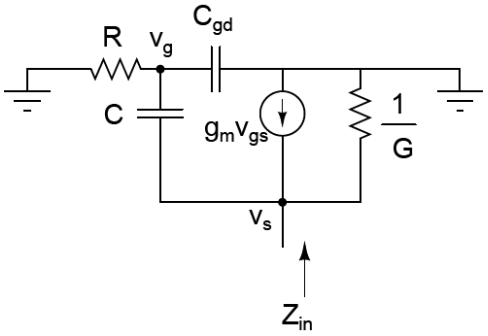


Figure 3.13: Active Inductor Small Signal Equivalent

Neglecting C_{gd}, the input impedence Z_{in} which is given below has the form of a lead-lag network and hence improves bandwidth.

$$Z_{in} = \frac{1 + sCR}{(g_m + G) + sC(GR + 1)}$$

One practical issue is that there may not be enough head-room for another transitor. Thus, the gate of the active inductor transistor needs to be biased at 2.4V(V_{dd} = 1.8V)

which is obtained using a voltage boosting circuit. The final schematic of the multiplier is shown below.

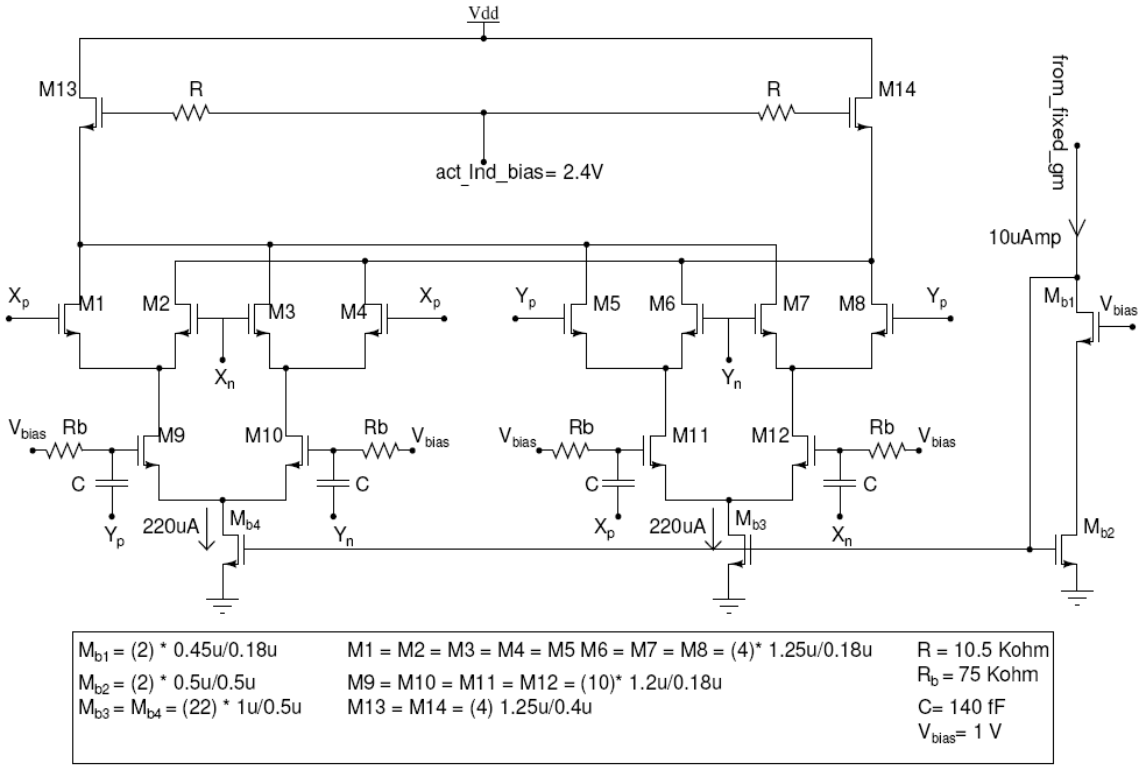


Figure 3.14: Schematic of the Symmetric Multiplier

3.5.2 Output Buffer

A buffer composed of a simple differential pair with active inductor loads is used for the multiplier outputs to drive the loads of the VCO.

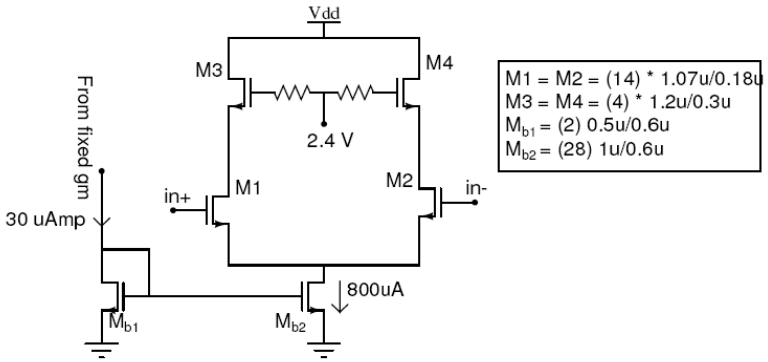


Figure 3.15: Schematic of the Output Buffer

CHAPTER 4

Implementation of the PLL

Till now, the implementation of both the ring and LC VCOs have been discussed. Now, the implemetation details of the rest of the circuit such as the programmable frequency divider, phase frequency detector (PFD) and charge pump circuit which complete the PLL have to be discussed.

4.1 Fixed g_m Bias Generation

Many parts of the VCOs utilize a fixed g_m bias current source to reduce circuit sensitivity to temperature variations.

4.1.1 Basic Fixed g_m Bias Cell

The basic fixed g_m bias generation cell is shown below.

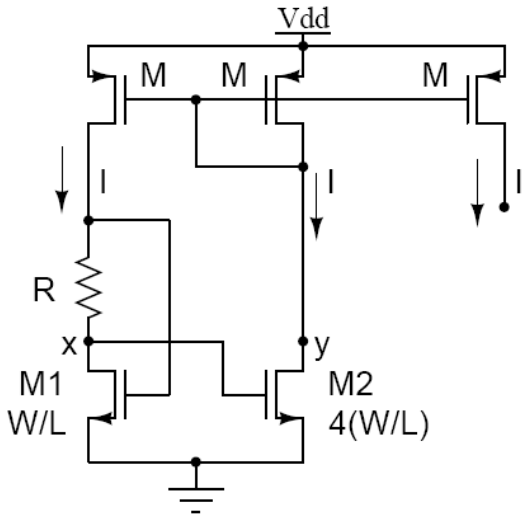


Figure 4.1: Basic Fixed g_m Bias Cell

Assuming transistors are in saturation, the voltage drop across the resistor R is

$$IR = V_{gs1} - V_{gs2} = (V_{Tn} + v_{ov}) - \left(V_{Tn} + \frac{v_{ov}}{2}\right) = \frac{v_{ov}}{2}$$

$$g_{m,M1} = \frac{2I}{v_{ov}} = \frac{1}{R}$$

If the current I is used to bias another transistor with identical dimensions as M1, the transconductance of that transistor will also be tracking $\frac{1}{R}$. However, due to finite g_{ds}, this may not be true and any supply or process variations may directly affect the voltage at node y.

4.1.2 Improved Fixed g_m Bias Cell

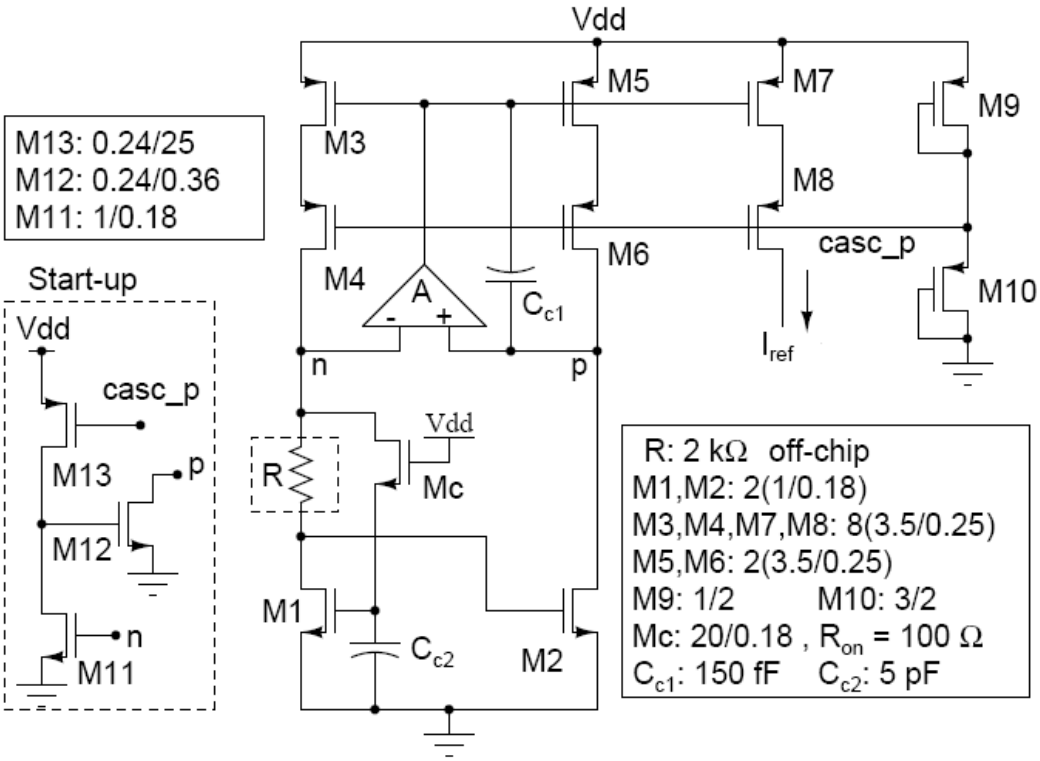


Figure 4.2: Schematic of the Improved Fixed g_m Bias Cell

This circuit has the following improvements:

- The PMOS current mirrors were cascoded to provide accurate current mirroring.

- To shield the drain of M2 against supply and process variations, an op-amp is connected between the nodes p and n and its output controls the gate of the top PMOS transistors. This means that any supply variation is approximately divided by the op-amp gain when it is felt at the drain of M2.

Op-amp Design

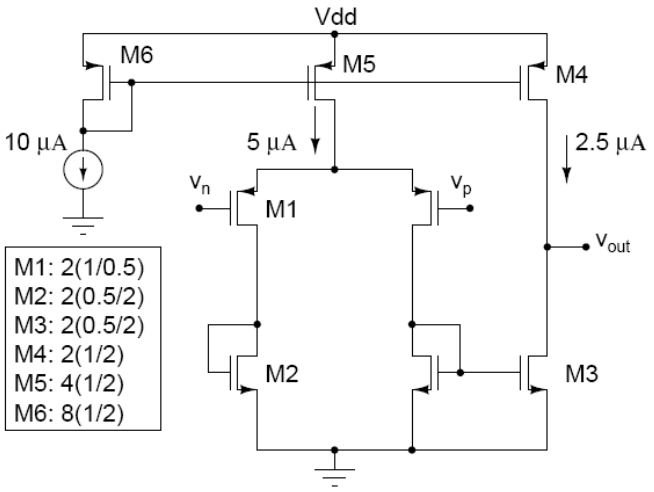


Figure 4.3: Schematic of the Op-amp used in Fixed g_m Bias Cell

The op-amp designed is a PMOS input current mirror based op-amp. This topology was selected since the input common mode level for the op-amp will be around 0.7 V and it has to drive the top PMOS gates of the bias cell. For a more detailed explanation of the circuit, refer to [4].

4.2 Programmable Frequency Divider

The frequency divider is implemented using a programmable divider chain which is programmable from 481 to 496 (16 channels with center frequencies from 2.405 GHz to 2.480 GHz). The architecture used, which is shown below, has become quite popular due to its modular nature.

The programming bits p_i control whether the cells divide by 2 or 3. F_{out} is the final output signal from the divider. If $p_i = 1$, then the i^{th} cell divides by 3 once every cycle of F_{out} i.e. the i^{th} cell adds one input period to its output for one period of F_{out} when

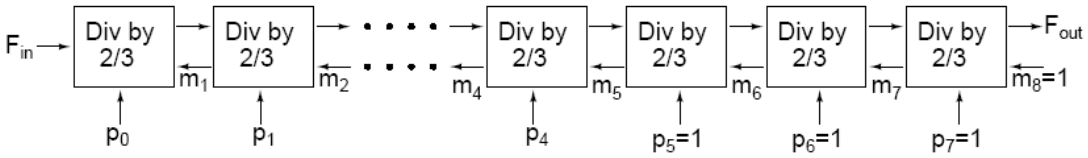


Figure 4.4: Programmable divider Implementation with N=481 to 496

$p_i = 1$. This functionality is achieved with the 'm' signal which makes the cells divide by three only once every cycle of F_{out}. The 'm' signal input to the last cell is set as '1'. So, the divide values range from 2^N to 2^{N+1} corresponding to P = 0 to $2^N - 1$.

For divide values from 481 to 496 atleast 8 cells are needed. The last 3 cells in the chain have their programming bits set to '1'. This restricts the programmability to N=480 to 511. If Q is the 4-bit channel select register, by adding 1 to it the 5-bit result can be used as programming bits, LSB through MSB go to the first five cells respectively.

4.2.1 Implementation of a 2/3 Divide Cell

Each 2/3 cell was implemented using four latches and three AND gates. Each latch can be implemented using CML logic with the AND gate embedded into the latch quite.

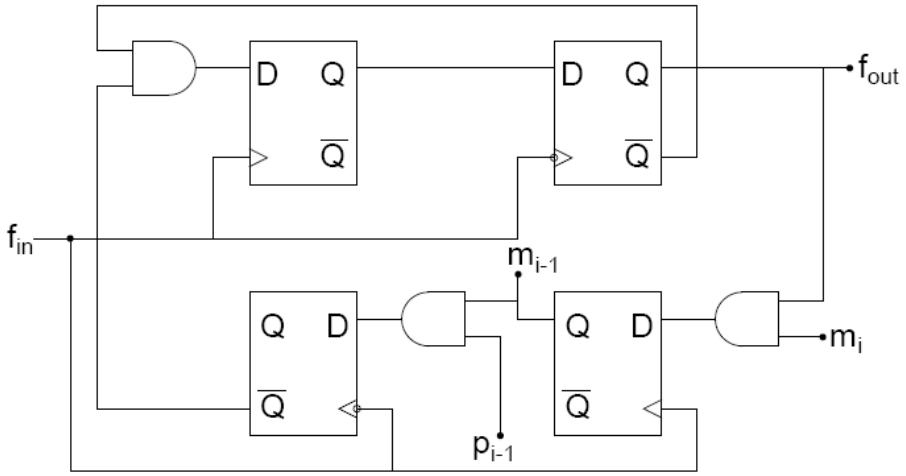


Figure 4.5: 2/3 Divide Cell Implementation

In the above circuit, m_{in} signal has only half a clock cycle to settle before the posi-

tive edge of the clock as the flip-flops are negative edge triggered. By taking f_{out} from the top left latch in the figure above the output changes during the positive cycle of the clock cycle. This leaves one full clock cycle for the latch to respond.

4.2.2 Implementation of the Divide Chain

An active inductor load was used for the first divider (working at 2.5GHz) and resistive loads for the others. Since each divide circuit operates at half the frequency as the previous one, all the device sizes and current were just be scaled by half while the load resistance was doubled. The 'latch with the AND gate embedded' used in the first divider in the chain (working at 2.5 GHz) is shown below:

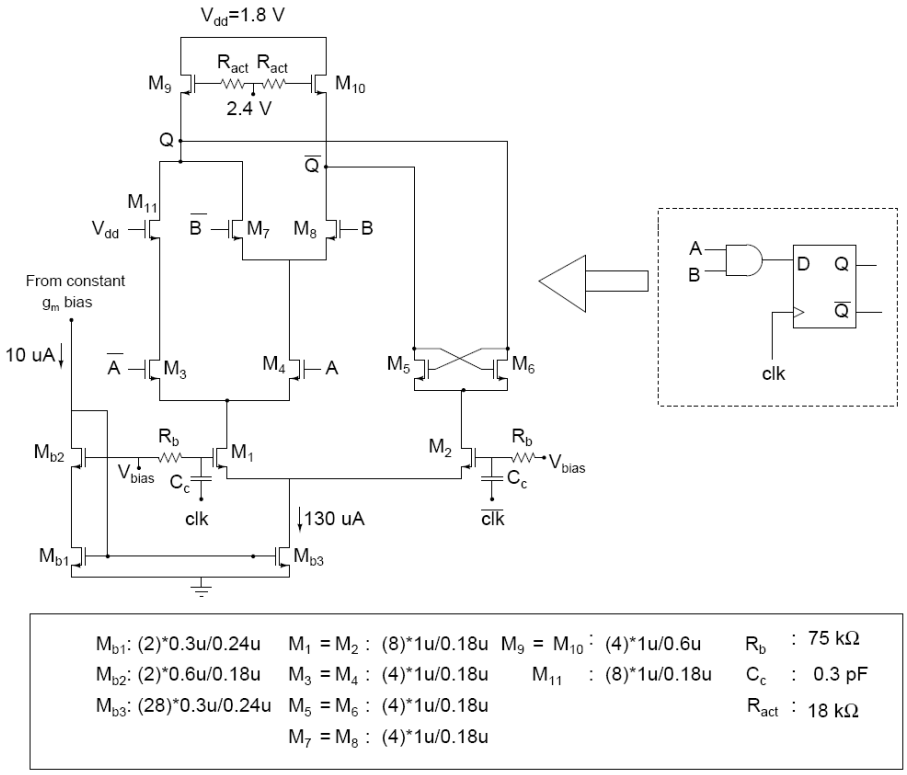


Figure 4.6: Schmatic of the CML Latch with an Embedded AND Gate used in the First Divider

Due to different DC operating points of the cells, the signals were AC coupled using a large capacitor and the DC bias was provided using a large resistor. For successive stages, the load resistor gets bigger and hence the DC coupling resistor needed is also bigger. Hence, the first four cells were coupled using R-C while the subsequent stages

used source follower circuits to shift down to the required DC level. For more details on the implementation and sizing of the stages, refer to [5].

4.3 Differential to Single-ended Converter

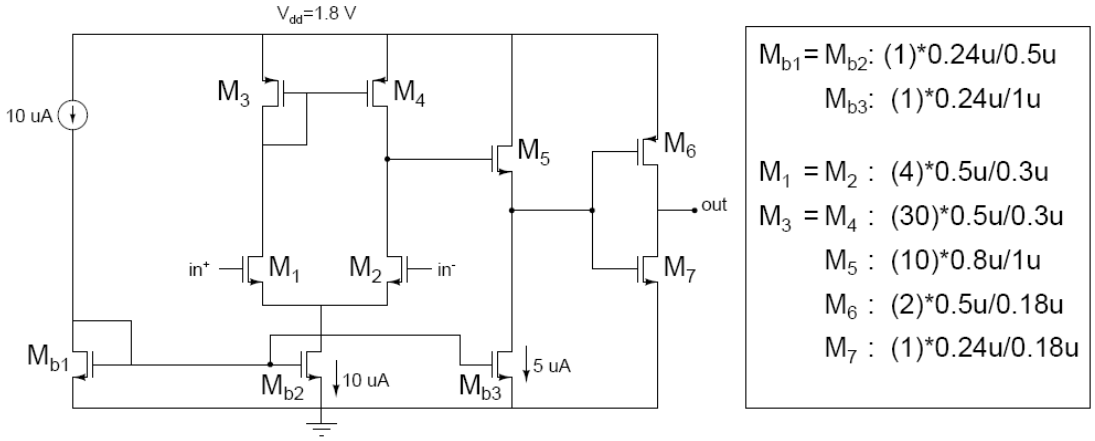


Figure 4.7: Schmatic of Differential to Single Ended Converter

The output of the frequency divider has to be converted to a single ended CMOS compatible form to be fed to the Phase Frequency Detector (PFD). This is done using a differential pair with a current mirror in the load which converts the differential signal to a single ended form. This was level converted using a source follower and fed to an inverter to convert the signal to a CMOS compatible form.

4.4 Phase Frequency Detector

The PFD measures the phase difference between the 5MHz refernce signal and the output of the frequency divider and drives the charge pump circuit. It can be easily implemented by using two flip-flops with asynchronous resets and an AND gate.

If A leads B, then UP stays at '1' from the positive clock edge of A till the positive clock edge of B. Then the AND gate output resets both the flip-flops. The same applies for DN when B leads A. Delays in the AND gate and flip-flop resets can lead to both

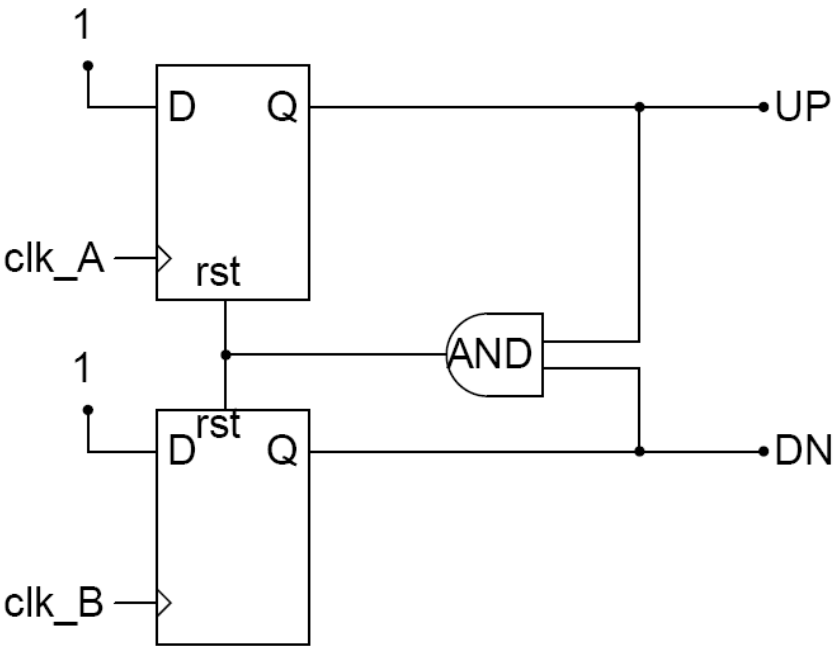


Figure 4.8: Block Diagram of the PFD

UP and DN being high for a short duration, but the charge pump has equal UP and DN currents and so no net current flows into the loop filter.

The flip-flops in the PFD are implemented using TSPC latches. More details on the implementation of the PFD can be found in [5].

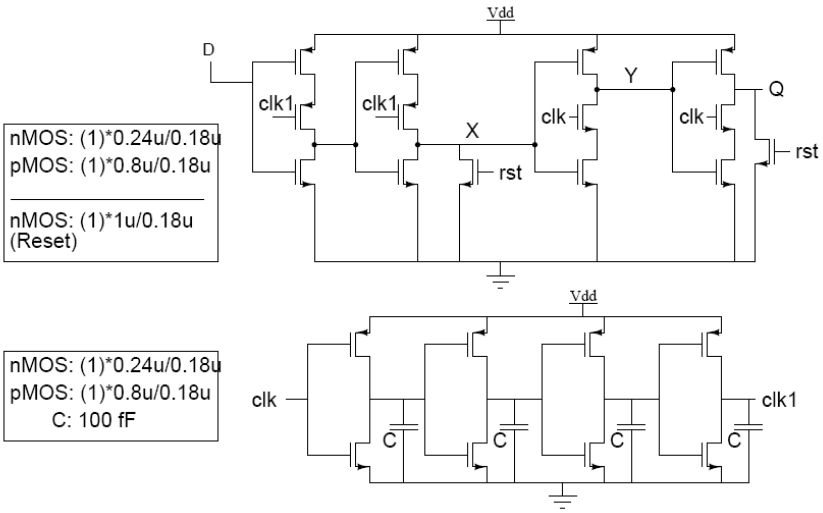


Figure 4.9: Schematic of the TSPC D flip-flop

4.5 Charge Pump

The charge pump converts the voltage corresponding to the phase difference between the two signals from the PFD to current which is passed through the loop filter. The basic requirements for a charge pump are two current sources for UP and DN currents which can be switched on or off on the outputs of the PFD.

The charge pump was implemented as a current steering CP. Current steering CPs don't switch off currents but just switch them to a dummy branch. Hence, the off-current is lower compared to non-current-steering CPs. The distortion at steady state is also slightly better. Since the MOS transistors stop conducting at voltages near the rails, the range of output tuning voltages is limited. This range is higher for current steering CPs. The schematic of the CP is shown below:

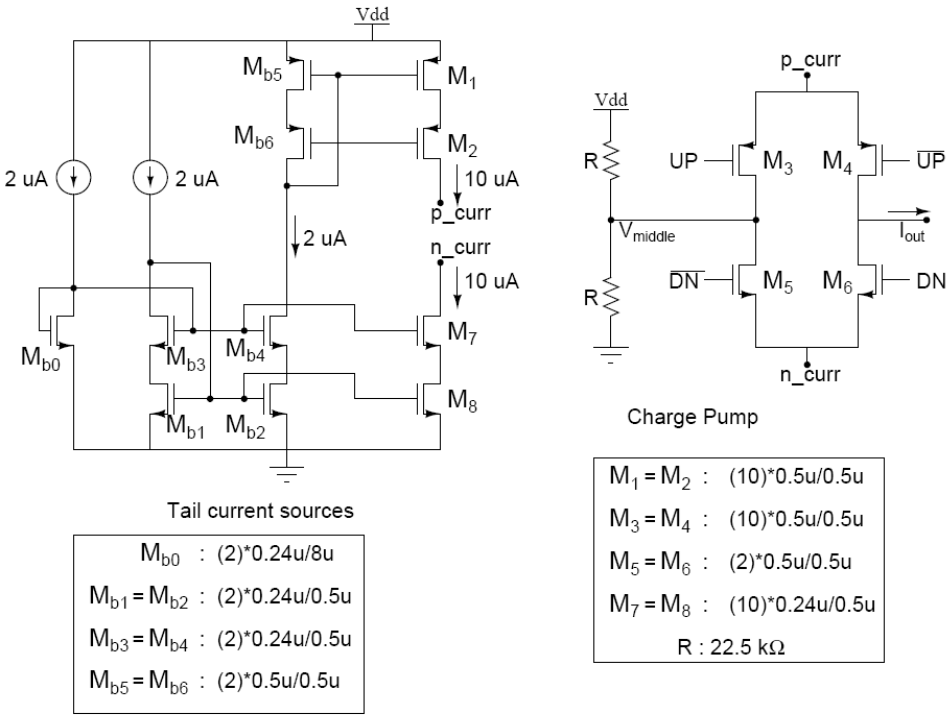


Figure 4.10: Schematic of the Current Steering Charge Pump

CHAPTER 5

PCB Design and IC Characterization

5.1 IC Characteristics

The IC designed in $0.18\mu m$ CMOS process was fabricated by Europractice foundry services. The layout of the chip is shown below:

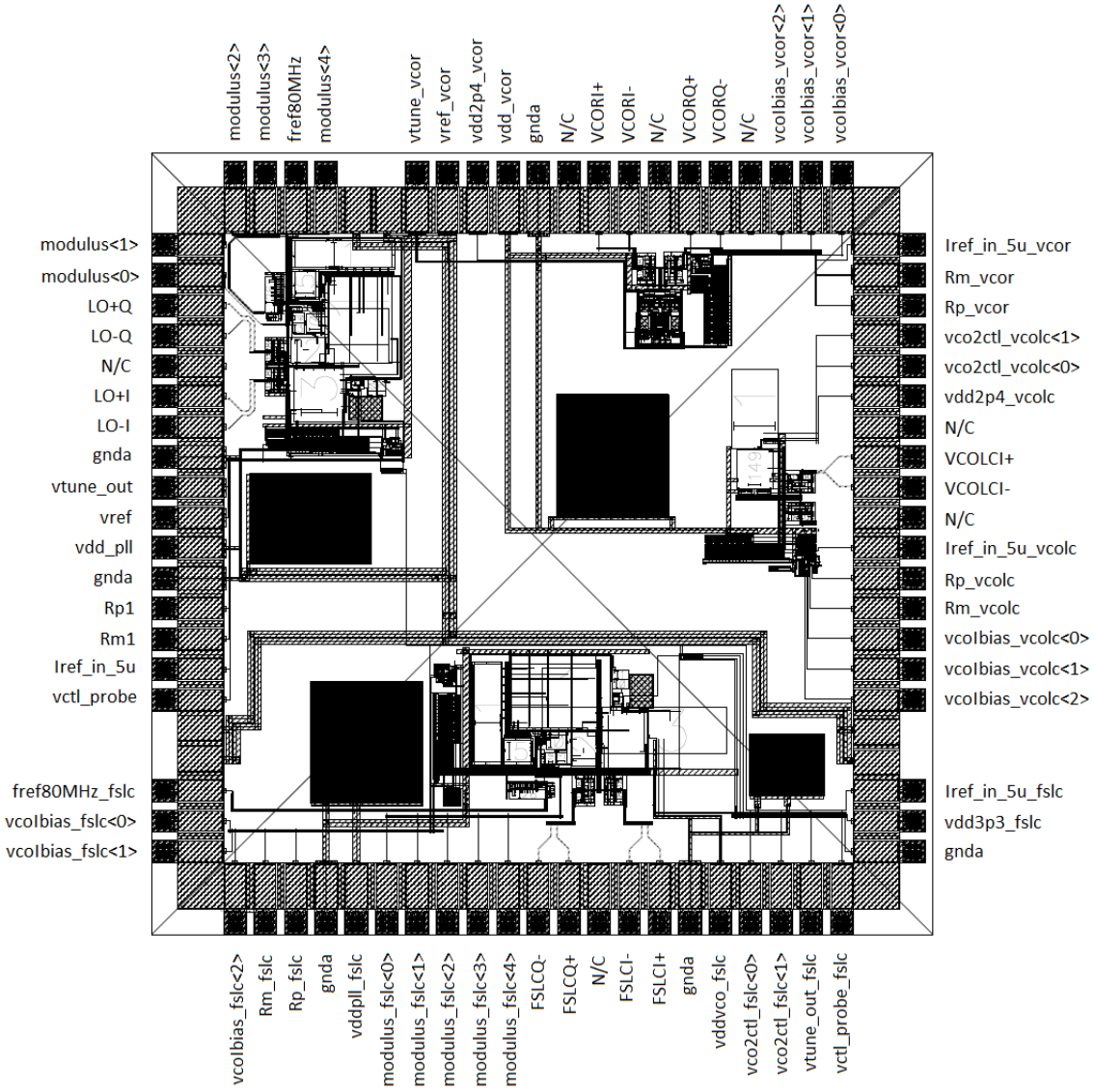


Figure 5.1: Layout of the Chip

The IC was obtained in a QFN80 package and consists of four seperate parts:

1. An externally tunable LC VCO.
2. An externally tunable ring VCO.
3. A ZigBee compliant frequency synthesizer with the LC VCO.
4. A ZigBee compliant frequency synthesizer with the ring VCO.

The major measurements required to characterize the IC are:

- The frequency and amplitude of oscillations for various tune voltages and modulus values.
- The phase noise of the frequency synthesizer.

All measurements were made using Rohde & Schwarz FSP Spectrum Analyzer. A screenshot of the output of the ring VCO on the display is shown below:

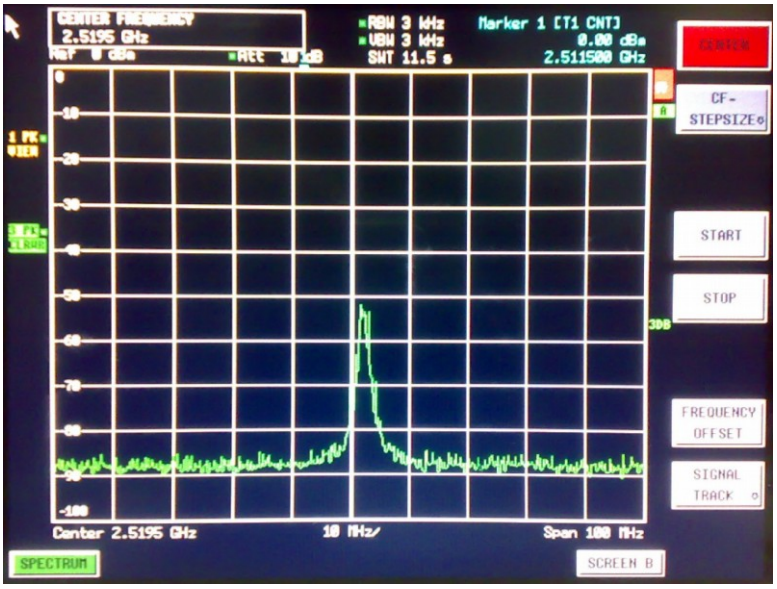


Figure 5.2: Measurement Screenshot

5.2 IC Measurements

5.2.1 VCO Measurements

The photograph of the PCB designed for measuring the properties of the VCOs is shown below. For the VCOs, the required bias voltages were 1.8V for V_{dd} and 2.4V for biasing

the active inductors. A current sink of $5\mu A$ is used as reference for generating bias currents in the circuits and can be fed from either one of the VCOs using jumpers. The only other input required is V_{tune} for the VCOs. The VCO output is measured only for its frequency and so only the positive I component is measured. Only the ring VCO characteristics could be measured due to problems mentioned later on in this chapter. Specific details of the PCB design are provided in the Appendix.

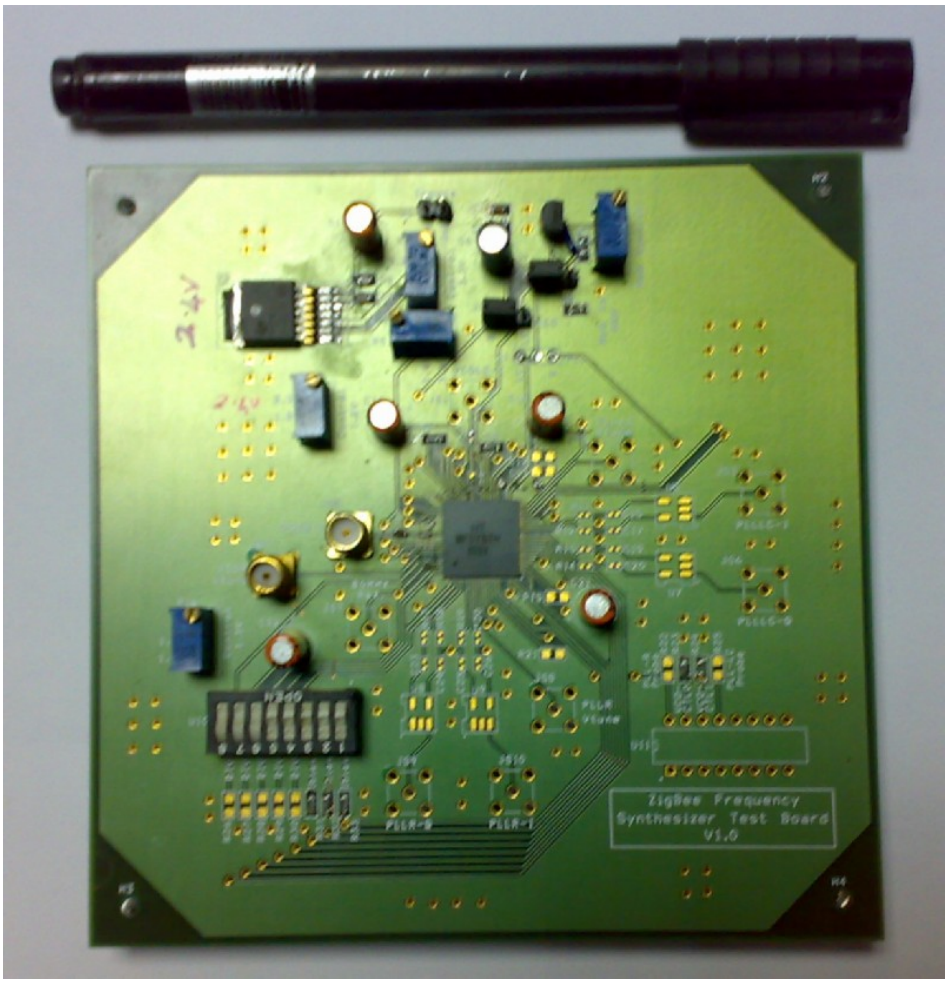


Figure 5.3: PCB for Testing the VCOs

The tuning characteristics of the VCO was measured for various values of V_{dd} and V_{ref}. It was observed that for a V_{dd} of above 1.88V, the tuning characteristics of the VCO changes abruptly and the phase noise also becomes much higher. This can be observed from the tuning curve for $V_{dd} = 1.9V$. This can be attributed to the fact that the transistors used for the active inductors go into the saturation region when their V_{gd} values is less than V_{Tn}. The measured tuning characteristics of the VCO are provided below:

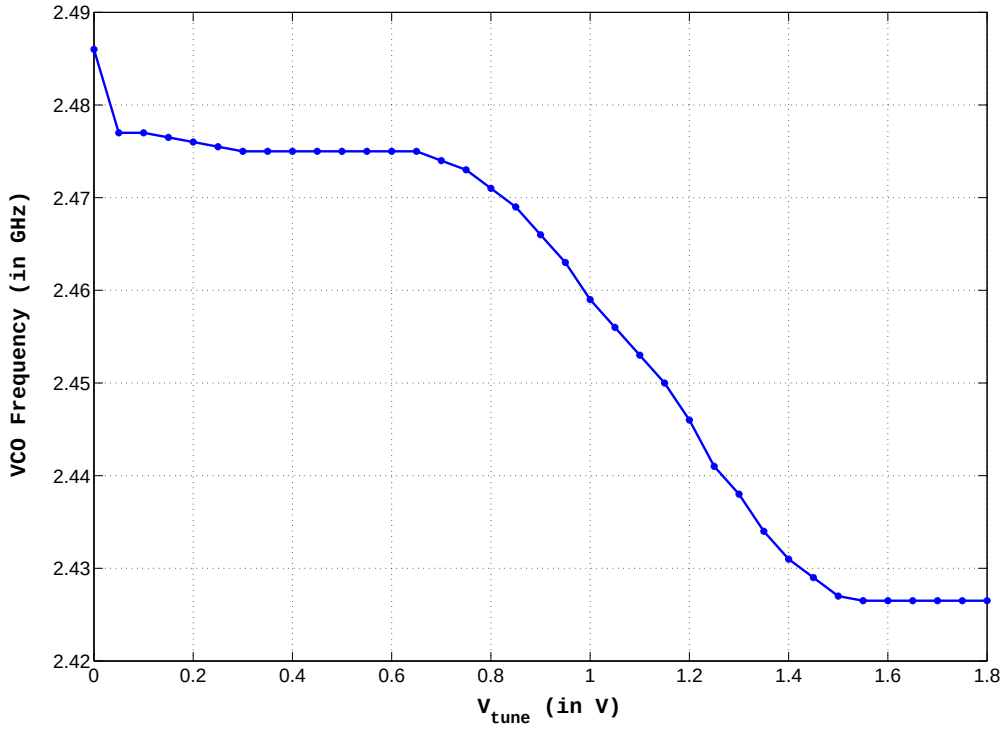


Figure 5.4: Measured Ring VCO Tuning Characteristics for V_{dd}=1.8V and V_{ref}=1.3V

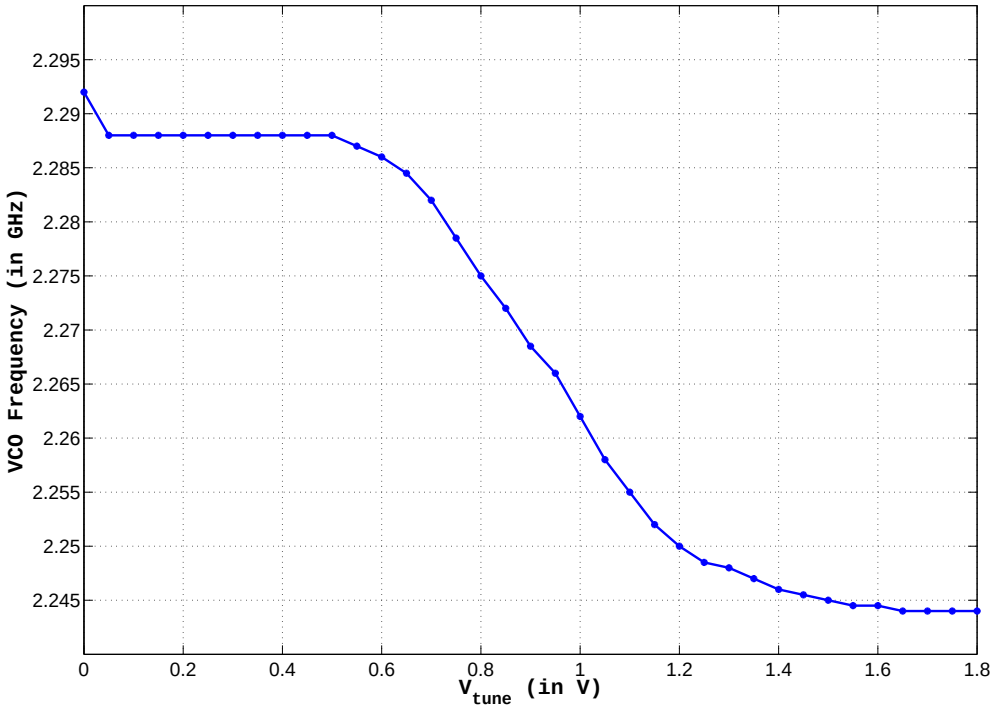


Figure 5.5: Measured Ring VCO Tuning Characteristics for V_{dd}=1.7V and V_{ref}=1.3V

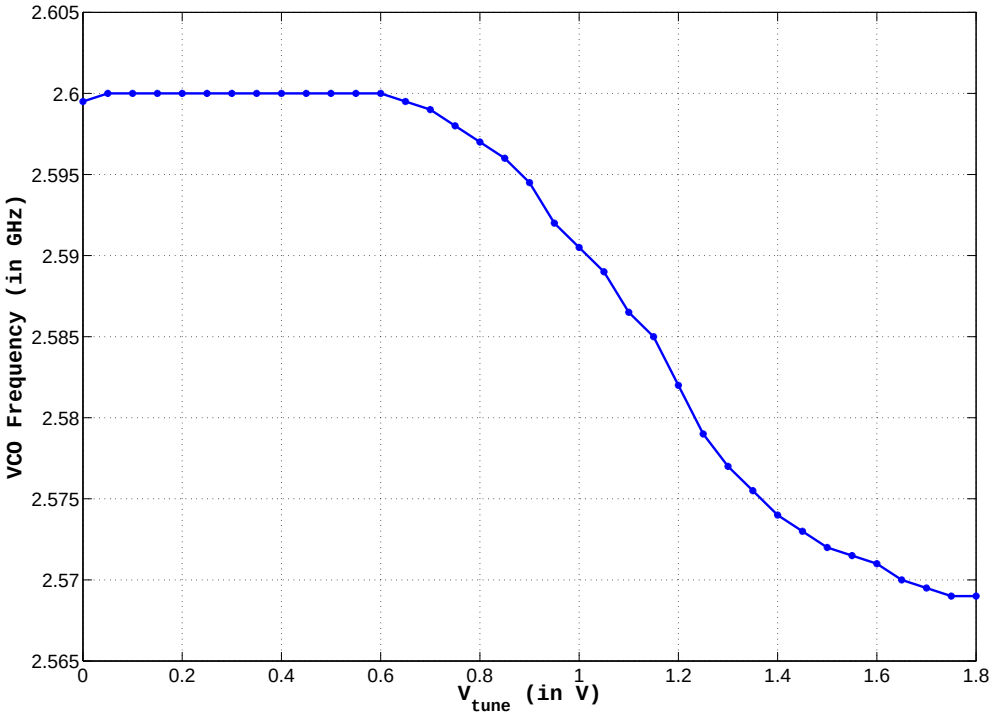


Figure 5.6: Measured Ring VCO Tuning Characteristics for V_{dd}=1.875V and V_{ref}=1.3V

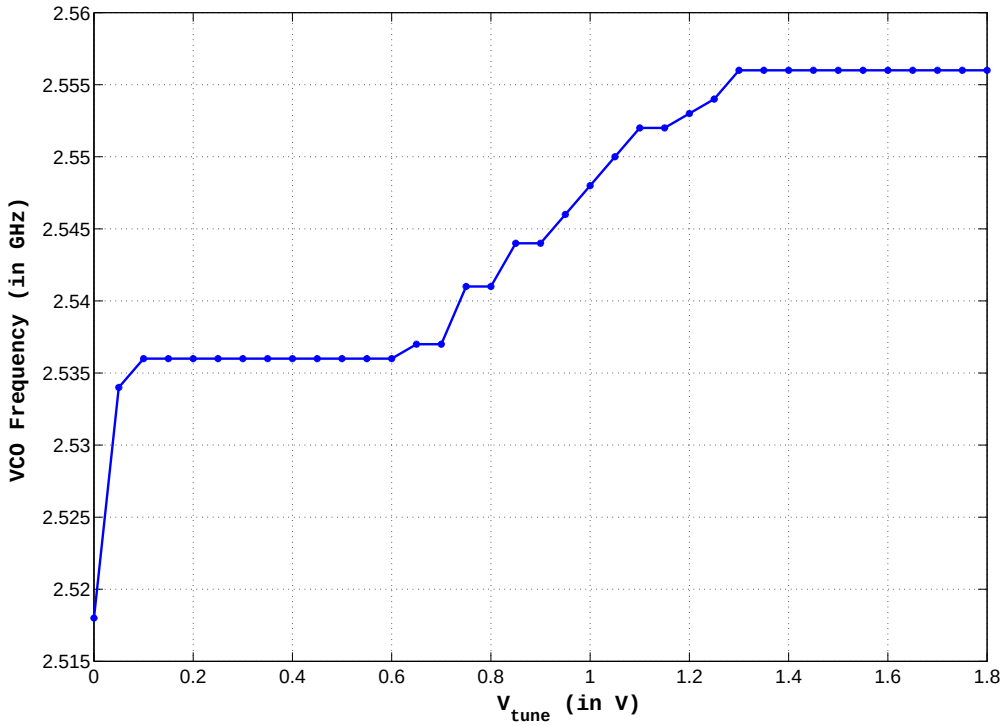


Figure 5.7: Measured Ring VCO Tuning Characteristics for V_{dd}=1.9V and V_{ref}=1.3V

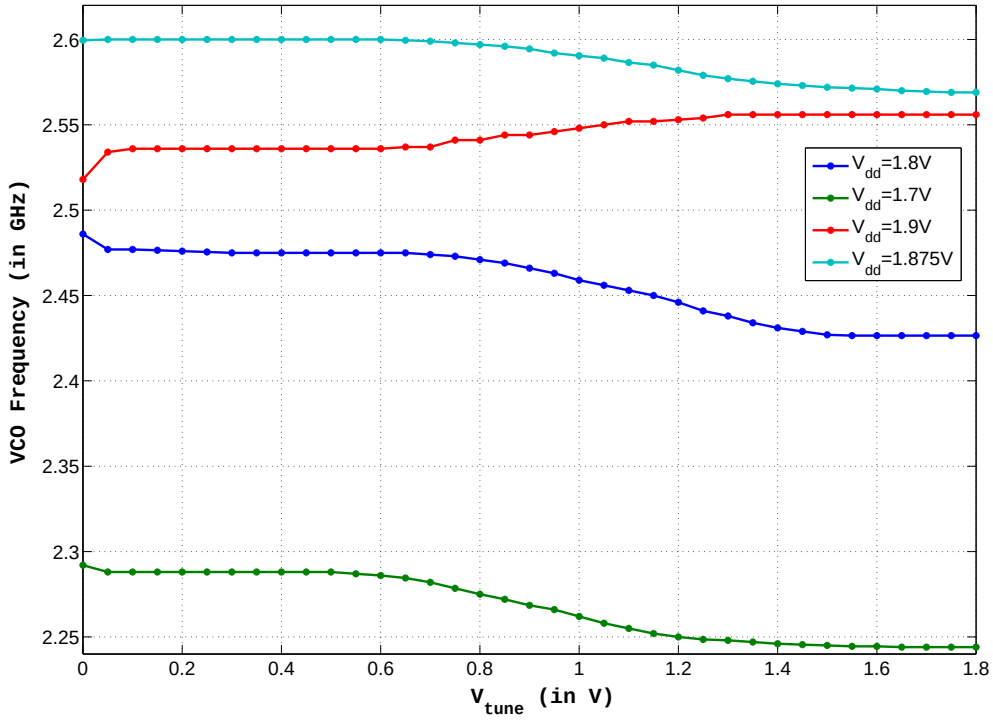


Figure 5.8: Ring VCO Tuning Characteristics for Various V_{dd} Values with V_{ref}=1.3V

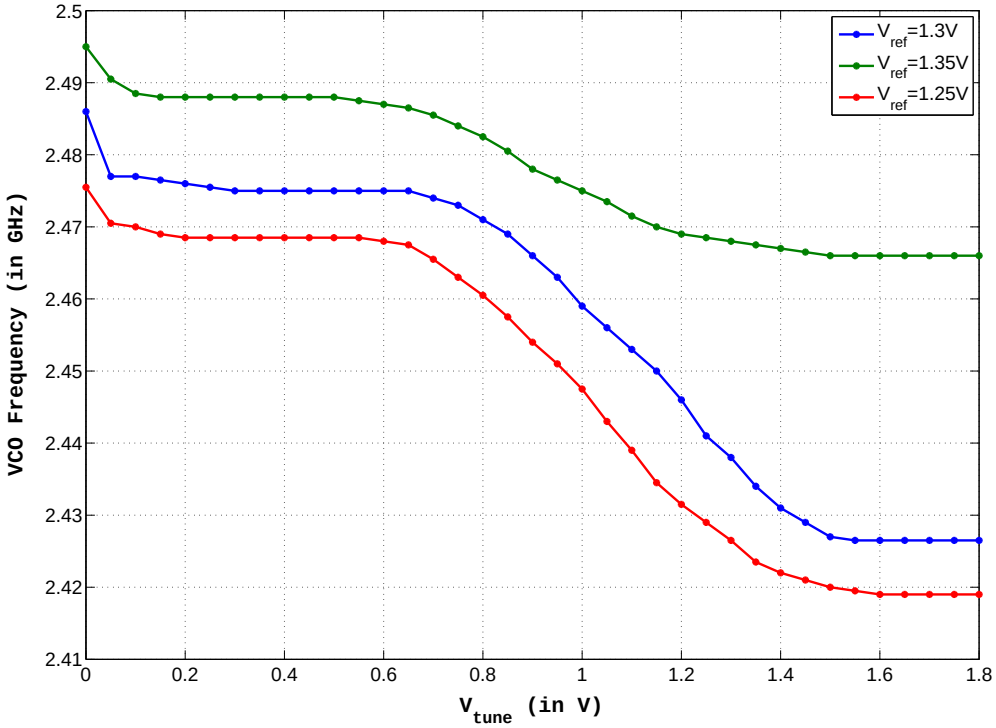


Figure 5.9: Ring VCO Tuning Characteristics for Various V_{ref} Values with V_{dd}=1.8V

Observations

The average k_{vco} values observed for the ring VCO in the high slope region of the tuning characteristics for various V_{dd} and V_{ref} values is recorded in the table below:

Table 5.1: Observed k_{vco} Values for Various V_{dd} and V_{ref} Values for the Ring VCO

V_{dd} (V)	V_{ref} (V)	k_{vco} (MHz/V)
1.8	1.3	-71.11
1.7	1.3	-66.67
1.9	1.3	27.27
1.875	1.3	-42.22
1.8	1.35	-34.44
1.8	1.25	-68.69

From the graphs and the table, it is clear that

- The tuning range reduces when V_{dd} or V_{ref} is increased beyond 1.8V and 1.3V respectively. The entire range also shifts to higher frequencies.
- The tuning range almost remains same for lower V_{dd} or V_{ref} values. However, the range shifts down to lower frequencies.

These observations can be explained using the following reasons:

- Increase in V_{dd} increases the current flowing through the PMOS transistors in the delay cells as their V_{sg} and V_{sd} increase. This increases the frequency of oscillations. The opposite happens when V_{dd} is reduced.
- Increaing V_{dd} beyond a certain range moves the transistors used for the active inductors into the saturation region when their V_{gd} values is less than V_{Tn} which reduces capacitances and increases g_m. This increasing noise and reduces the inductive characteristic.
- Increase in V_{ref} reduces the voltage swing at the output and increases oscillation frequency while decreasing V_{ref} results in the opposite.

5.2.2 PLL Measurements

The photograph of the PCB designed for measuring the properties of the frequency synthesizer with the ring VCO is shown below. Unfortunately, the measurements couldn't be made due to the problems mentioned later on in this chapter.

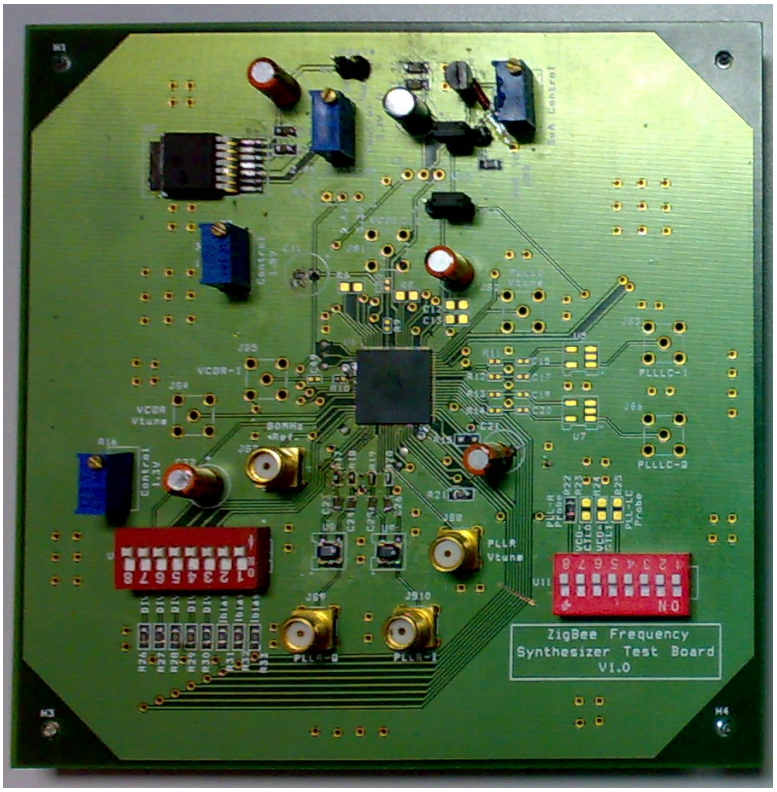


Figure 5.10: PCB for Testing the PLL with the Ring VCO

5.3 Problems Encountered

5.3.1 Problems with the Chip

There was a critical error in the layout of the chip related to the handling of the tuning voltage inputs (V_{tune}) to the varacters of the LC VCOs.

- In case of the standalone LC VCO, the V_{tune} input was unavailable as a pin in the chip and so the VCO couldn't be tuned externally.
- In case of the LC VCO based frequency synthesizer, V_{tune} input of the LC VCO was not connected to the output of loop filter and so the loop was incomplete.

These problems meant that the LC VCO and the synthesizer based on it couldn't be tested.

5.3.2 Problems with the PCB

There was a critical error in the layout of the PCB. The PCB layout used a QFN84 footprint for the chip while the the actual package was QFN80. This happened because the chip bonding diagram and package information were not available during the design of the PCB. The chip layout had 84 pads and so a QFN84 footprint was assumed.

Due to the arrangement of the pins, the PCBs were still usable if only one part of the chip and its associated components were soldered per PCB. Hence, two PCBs were required, one for the standalone ring VCO and another for the ring VCO based frequency synthesizer. However, soldering of the chip had to be done manually which was successful only in the case of the PCB for testing the VCOs.

5.4 Conclusion

This work involved designing PCBs for testing frequency synthesizers for the ZigBee standard based on LC and ring VCOs. Though the characterization of the ring VCO was done successfully, the characterization of the PLL based on it and the LC VCO and the PLL based on it couldn't be done due to layout errors in the chip and the PCB. Though the design for the PCB has already been rectified, the errors in the chip should be corrected to fully characterize the IC.

APPENDIX A

PCB Design

A.1 PCB Schematic

The schematic of the PCB is segmented into the following sub-schematics:

- Frequency Synthesizer Chip Schematic shown in A.1.
- Bias, References, Supply & Bypass Capacitors Schematic shown in A.2.
- Control Logic Schematic shown in A.3.
- Analog Inputs & Outputs Schematic shown in A.4.

A.1.1 Frequency Synthesizer Chip Schematic

The TOP and BOTTOM plane copper pour areas are connected to GND to ensure uniform GND across the PCB. The GND and the PWR planes are connected to the GND and 1.8V nodes respectively to provide low inductance paths for high frequency signals to flow. Multiple VIAS spread across the PCB are used to connect the TOP and BOTTOM GND planes. $2k\Omega$ resistors are used as PTAT references for the fixed g_m biasing circuits.

A.1.2 Bias, References, Supply & Bypass Capacitors Schematic

The chip requires 4 bias current sinks of $5\mu A$ each - for ring VCO, ring PLL, LC VCO and LC PLL. Only one needs to be connected at any given time. This is achieved using a series of jumpers. The current is generated using LM334 IC. The supply to LM334 IC is appropriately bypassed. Voltages requred in the circuit are 1.3V, 1.8V, 2.4V and 3.3V. The 3.3V reference is obtained using the TPS74401 LDO IC and the others are obtained using resistive dividers. Current is mainly drawn from the 1.8V supply and so

it is obtained using a 100Ω voltage divider while the rest use a $10k\Omega$ divider. At the supply inputs of the chip, a combination of a $10\mu F$ through-hole (TH) capacitor and $1\mu F$, 100 nF and 10nF surface mount (SM) capacitors are used for bypass capacitances. Supplies of 5V and -1.5V are required for the working of the TPS74401 and LM334 IC respectively.

A.1.3 Control Logic Schematic

Two 8 switch DIP ICs are used to set the various control pins to VDD/GND. When the switch is OFF, a pull down resistor is used to bring the control pin voltage back to GND. This is achieved by using $100k\Omega$ resistors for pull down. The control pins are used to set the modulus values for the frequency synthesizers, set the controls for the bias current generation block, enable varacter blocks in the LC VCO and enable V_{tune} outputs for measurement in case of the synthesizers.

A.1.4 Analog Inputs & Outputs Schematic

The chip requires various inputs such as the 80MHz reference clock, tune voltages for the VCOs, etc. The outputs are taken to be single ended in case of the output signals of VCOs and tune voltages of the PLLs and differential in case of the output signals of the PLLs. The transmission lines are impedence matched using resistors and the differential signals are converted to single ended using TC1113MG2 balun transformers.

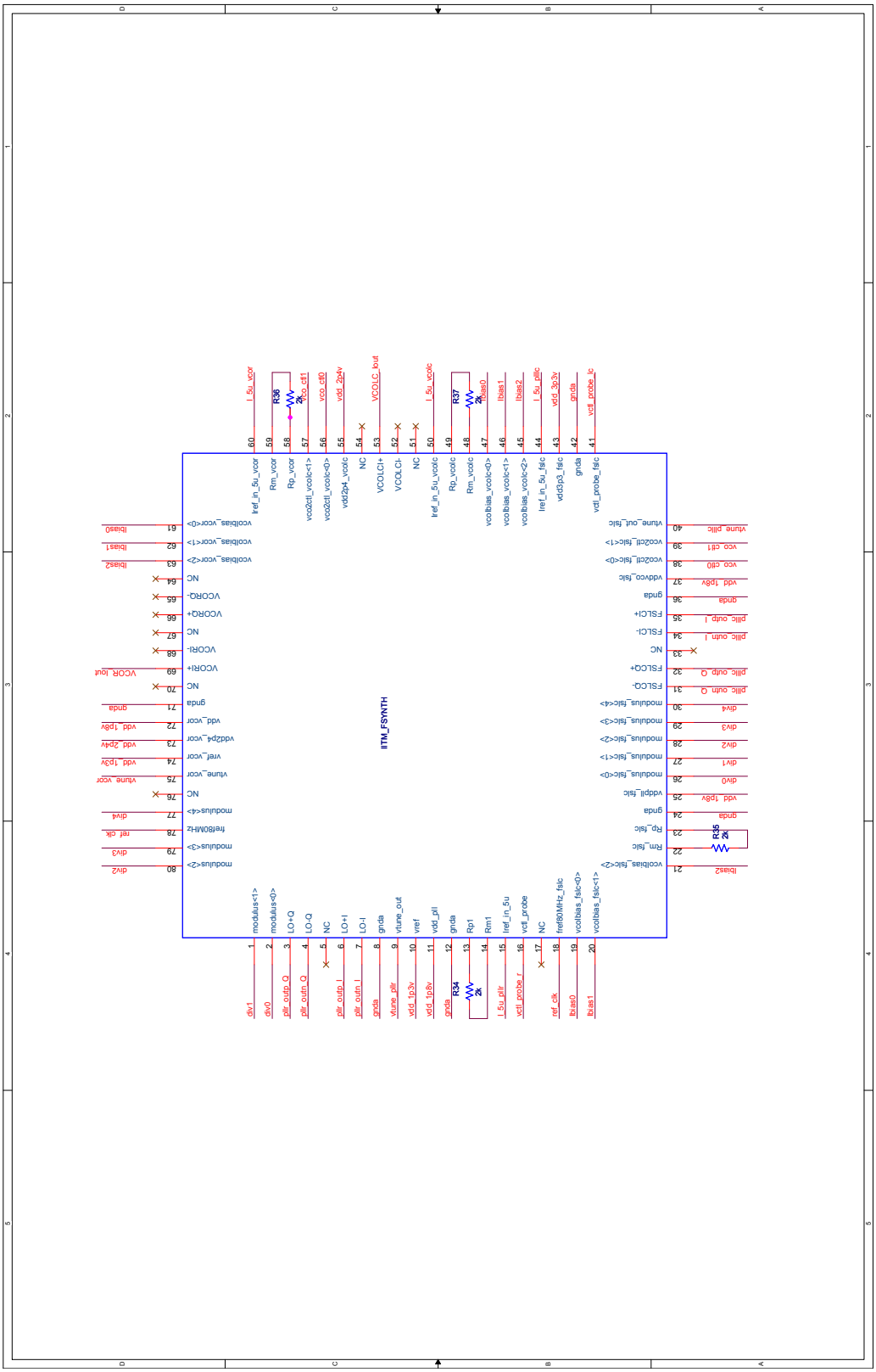


Figure A.1: Frequency Synthesizer Chip Schematic

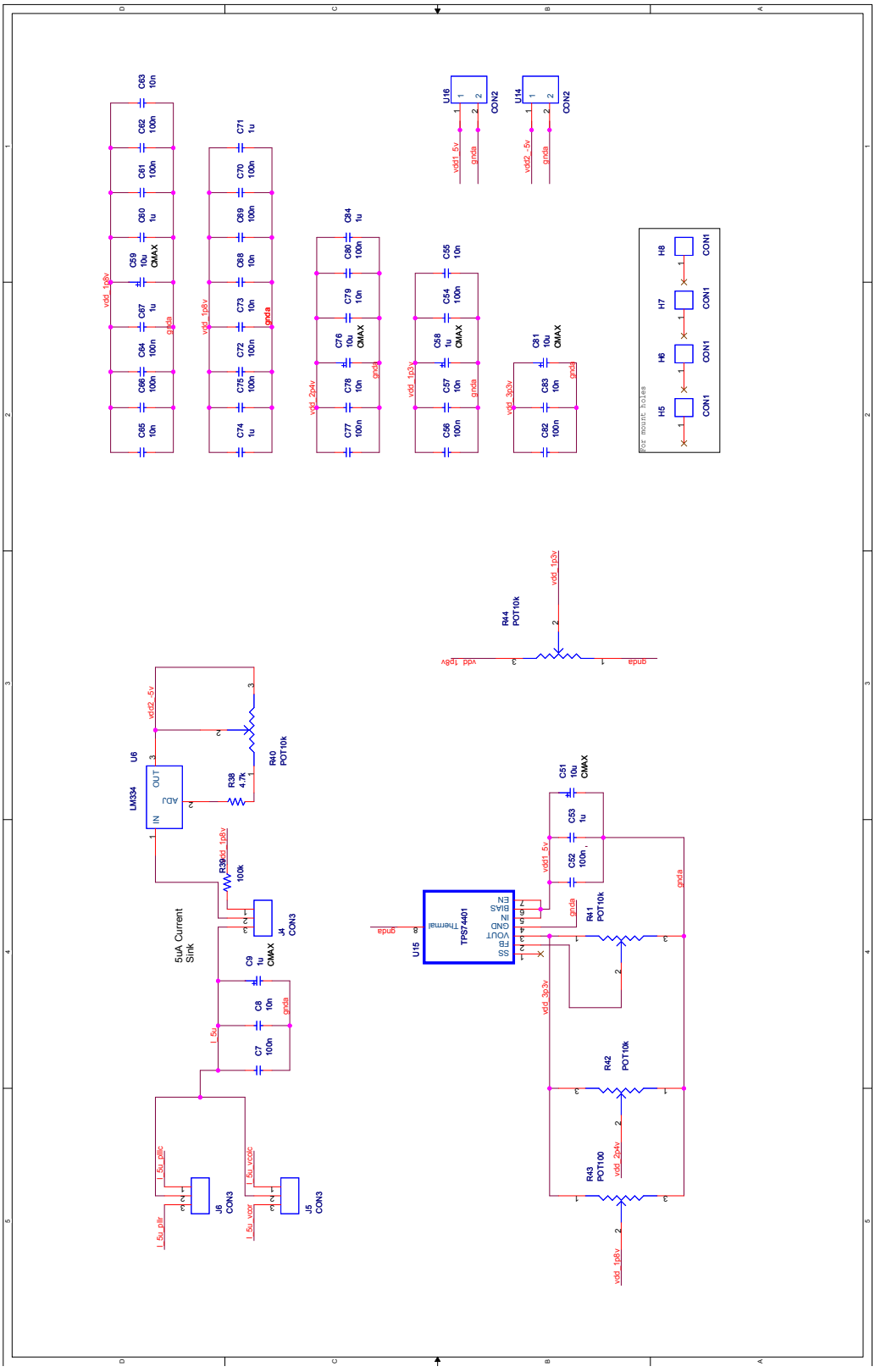


Figure A.2: Bias, References, Supply & Bypass Capacitors Schematic

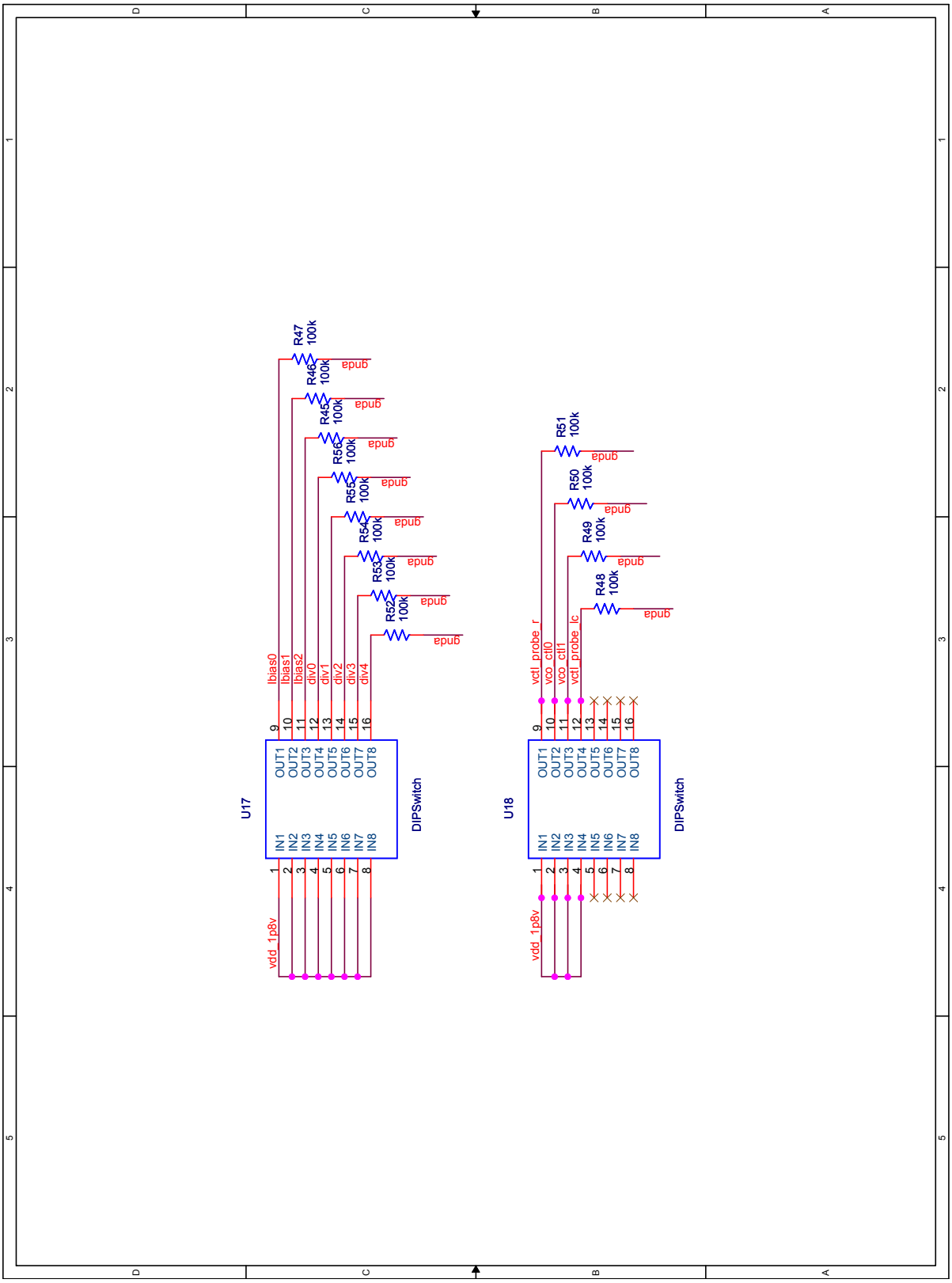


Figure A.3: Control Logic Schematic

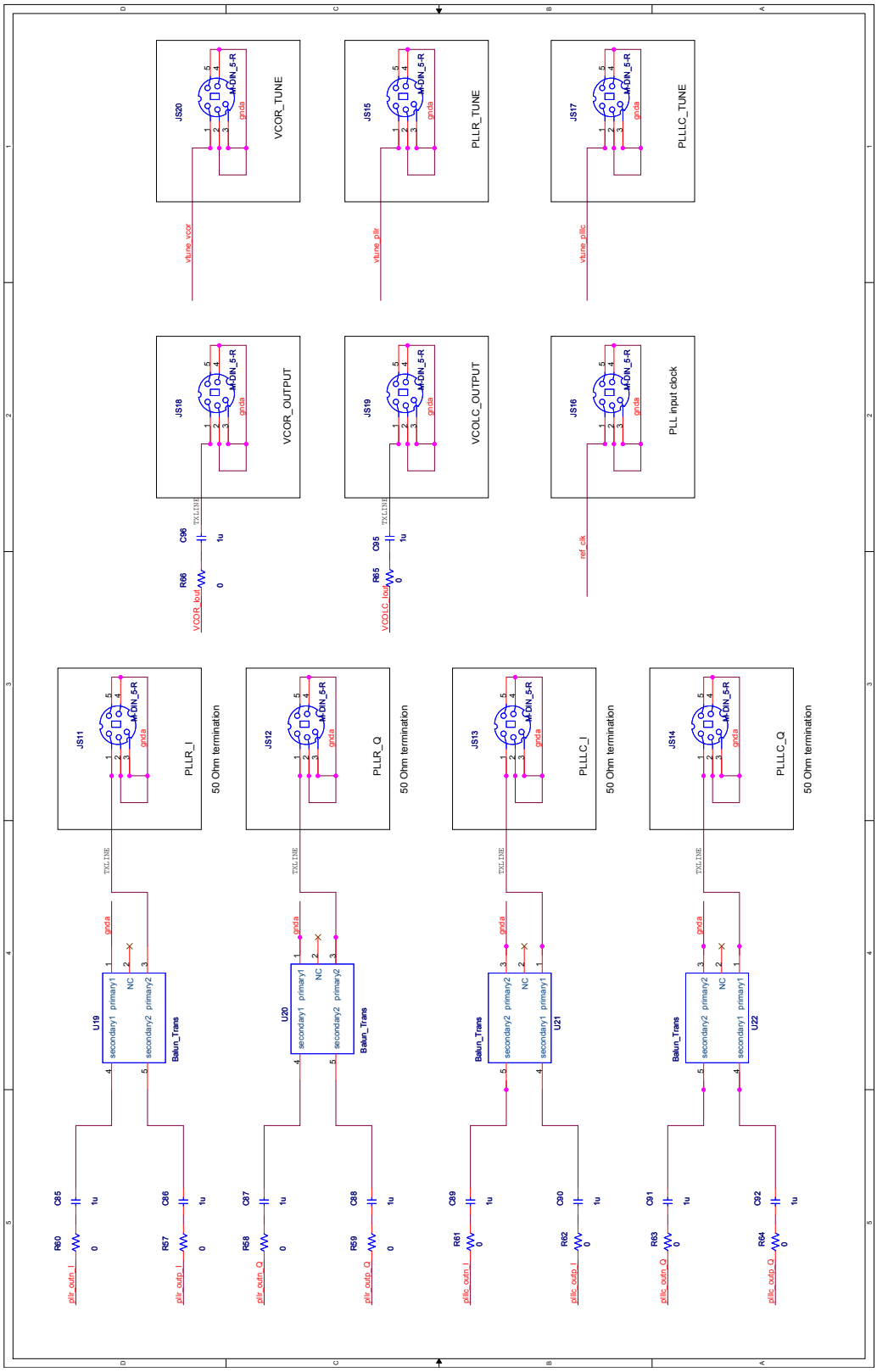


Figure A.4: Analog Inputs & Outputs Schematic

A.2 PCB Layout

The PCB used is a four layer board with TOP, BOTTOM, PWR and GND layers. The GND and the PWR layers are connected to the GND and 1.8V nodes respectively. The layout of the other two layers are shown below:

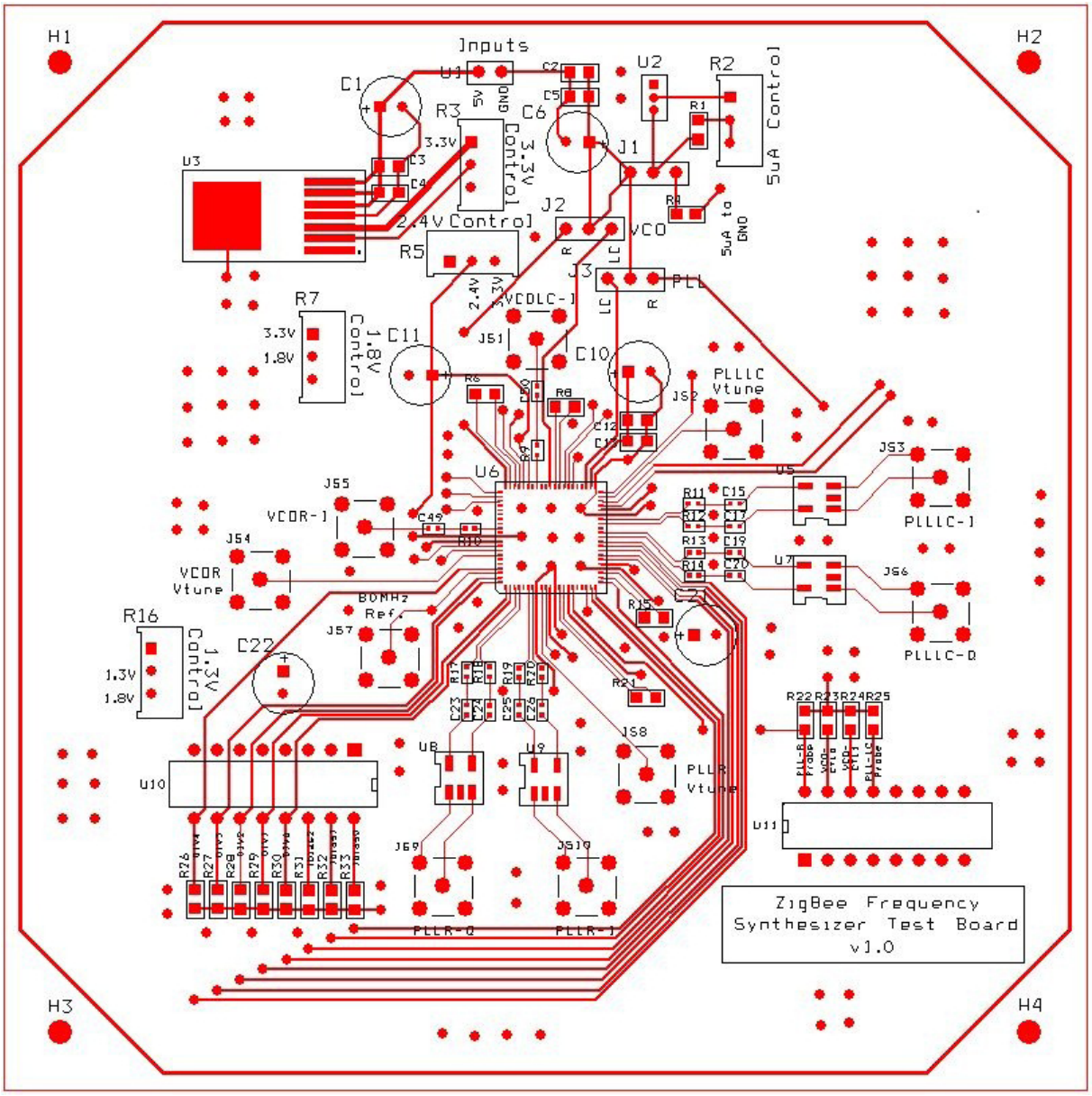


Figure A.5: Layout of the TOP Layer of the PCB

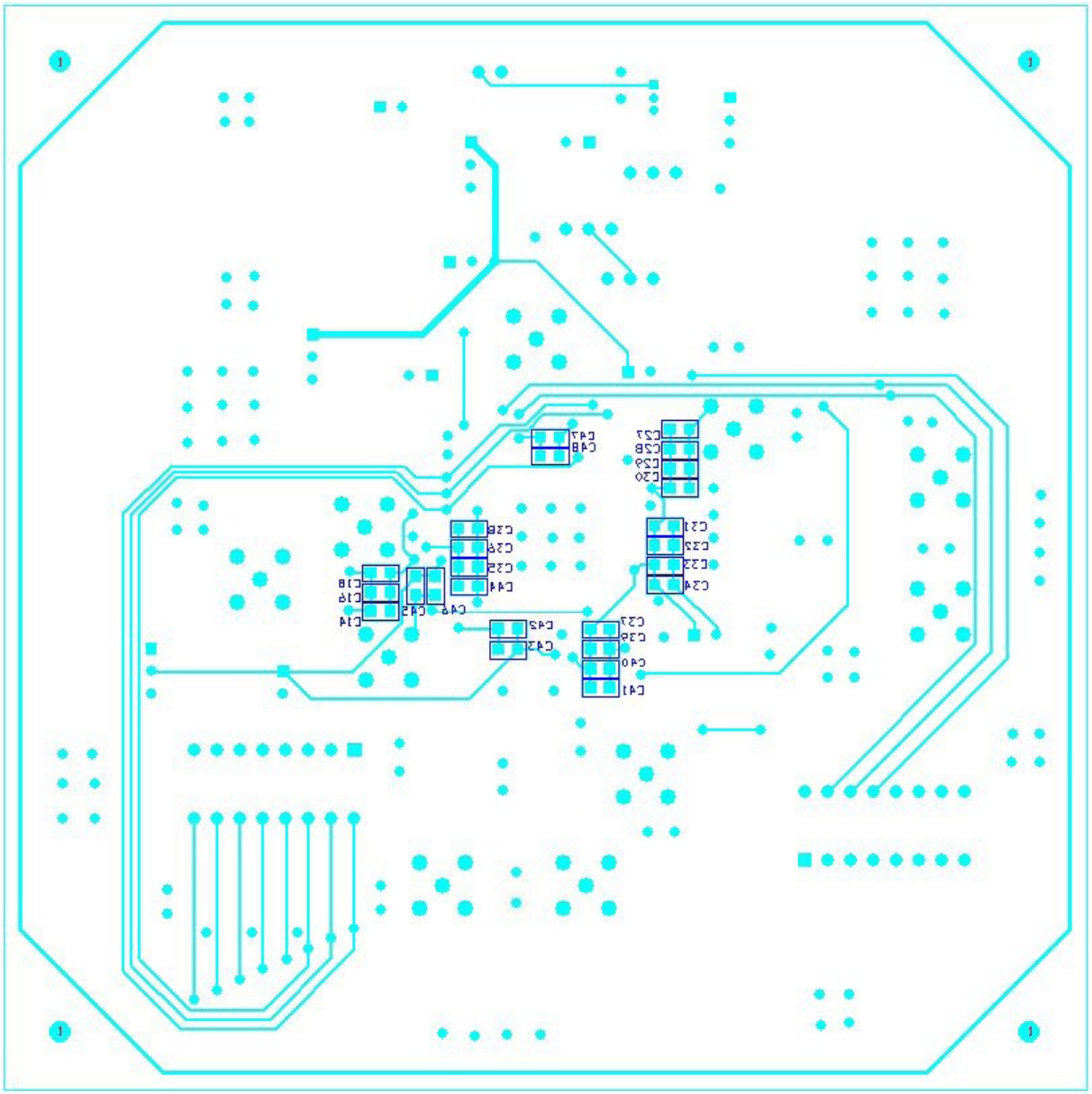


Figure A.6: Layout of the BOTTOM Layer of the PCB

REFERENCES

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.

[2] L. Manoj Kumar, A. Mohan, and N. Krishnapura, "A comparison of approaches to carrier generation for zigbee transceivers," in *22nd International Conference on VLSI Design*, 2009.

[3] L. M. Kumar, "Design of vco for frequency synthesizer in zigbee transceiver," Master's thesis, IIT Madras, July 2008.

[4] J. R. Prabhu, "Design of low power rf front-end blocks for a 2.4 ghz ieee 802.15.4 compliant zigbee transceiver," Master's thesis, IIT Madras, July 2007.

[5] A. Mohan, "Frequency synthesizer for a zigbee transceiver," Master's thesis, IIT Madras, May 2007.