Fully-Differential Opamp Design

Elyes Balti, *Student Member, IEEE*

***Abstract*—Operational amplifier is considered as the core of the analog building blocks. High performance opamp must exhibit high gain, wide bandwidth, low power consumption and rail-to-rail output swings. In this work, we propose to design a fully-differential opamp design to satisfy certain design requirements and specifications.**

***Index Terms*—Cascode, Class-AB, Dual Diff-Pair, CMFB, ICMR**

I. Design Specifications

A. Requirements

In this project, the opamp design must satisfy the following specifications given by Table 1.1.

TABLE I: Opamp Design Specifications

Parameter	Specified value
Technology	TSMC 180-nm
Supply voltage, V_{DD}	1.8 V
Common-mode voltage, V_{CM}	0.9 V
Typical load	100 kΩ, 1 pF
Unity gain frequency (f_{un})	$\geq$ 50 MHz
Open-loop gain (A_{OL})	$\geq$ 60 dB
Closed-loop gain (A_{CL})	6 dB
Closed-loop bandwidth ($f_{3dB,CL}$)	$\geq$ 20 MHz
Slew-rate (SR)	$\geq$ 100 $\frac{V}{\mu s}$
Phase margin (ϕ_M)	60 deg
Output swing	$\geq$ 1.5·V_{DD}
Power consumption	Minimum possible

To meet these requirements, the opamp design must include the following specifications:

- Two-stages: the first stage provides a high gain, while the second stage provides a high output swing (rail-to-rail) to drive a high load.
- The first stage does not necessarily provide high swing, but it has to provide high gain with minimum power consumption. The folded cascode amplifier is not suitable for the first stage since its gain is reduced 2 to 3 times compared to the telescopic and also the power consumption is higher, although it provides not only a wider ICMR and output swing, but also an excellent overlap of the ICMR and the output swing. Finally, the best candidate amplifier for the first stage is the cascode since it provides a high gain. The cascode also provides a higher bandwidth compared to the folded cascode since the last one has an additional pole due to the current summation at the node linking the bias source and the upper side of the cascode.
- The second stage is class-AB so that the output has a rail-to-rail swings (from 0 to V_{DD})
- Each stage has to be compensated separately, since this method is very robust compared to the method of using one compensation feedback loop for the two stages.
- Dual Diff-Pair CM Detector can be used in the first stage because it drives only small capacitive load and it does not affect the gain. However, it allows very limited output swings which is not required for the first stage.
- Since the second stage is class-AB, the practical CMFB method is the current injection.

Elyes Balti is with the Wireless Networking and Communications Group, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712 USA e-mail: ebalti@utexas.edu.

B. Bias circuit

In this project, a current of 20μA is biasing the first stage. To generate such current value, A BMR circuit is designed and used as a bias circuit to feed the first stage. The process of biasing should take place with a constant transconductance g_m. To generate a current of 20 μA for the process of 180 nm, I should determine first the corresponding size of the MOSFET given that V_{ov} is 90 mV. After the simulation and testing, I come up with the following MOSFET parameters' values so that to generate 20 μA.

TABLE II: Short-channel 180nm process MOSFET parameters

Parameter	NMOS	PMOS
V_{ov}	90 mV	90 mV
V_{THN} and V_{THP}	457 mV	463 mV
V_{GS} and V_{SG}	547 mV	553 mV
$V_{DS,sat}$ and $V_{SD,sat}$	60 mV	60 mV
Bias Current I_D	20 μA	20 μA
W/L	28/2	86/2
g_{mn} and g_{mp}	285 μA/V	260 μA/V
γ_{on} and γ_{op}	314 KΩ	437 KΩ

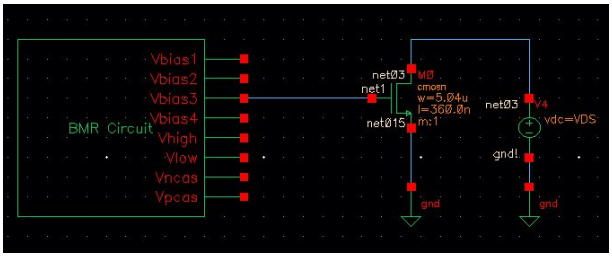

Fig. 1: NMOS testing for 20 μA

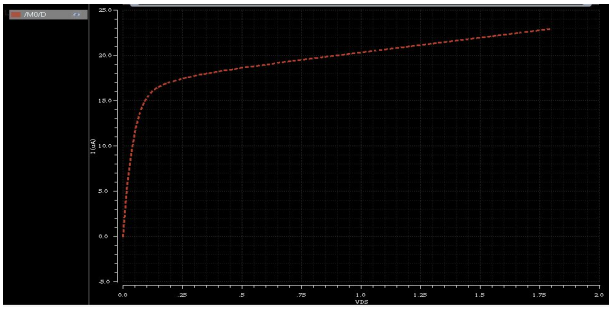

Fig. 2: NMOS bias current I_{D} = 20 μA

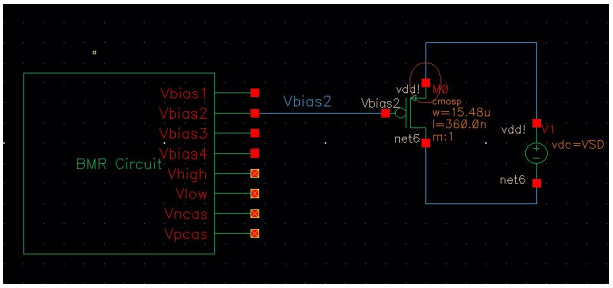

Fig. 3: PMOS testing for 20 μA

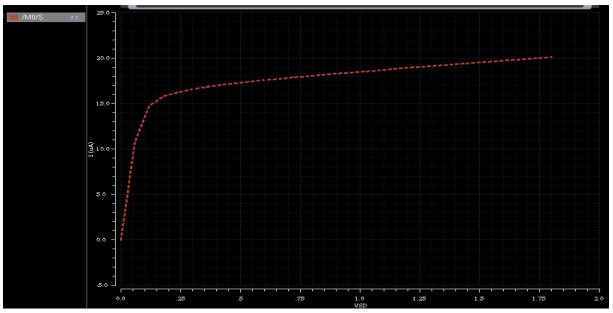

Fig. 4: PMOS bias current I_{D} = 20 μA

Each branch of the first stage is fed by 20μ A, to satisfy this condition, the total bias current of the first stage os 40μA. To achieve this value, the size of the NMOS must be doubled to be 56/2 and for the PMOS is 172/2. Note that Vbias 2 and 3 feed PMOS and NMOS, respectively.

II. First stage

A. Specifications

In this design, the first stage should provide a sufficient high gain. To satisfy this requirement, I suggest the cascode amplifier given by Fig. 2.1.

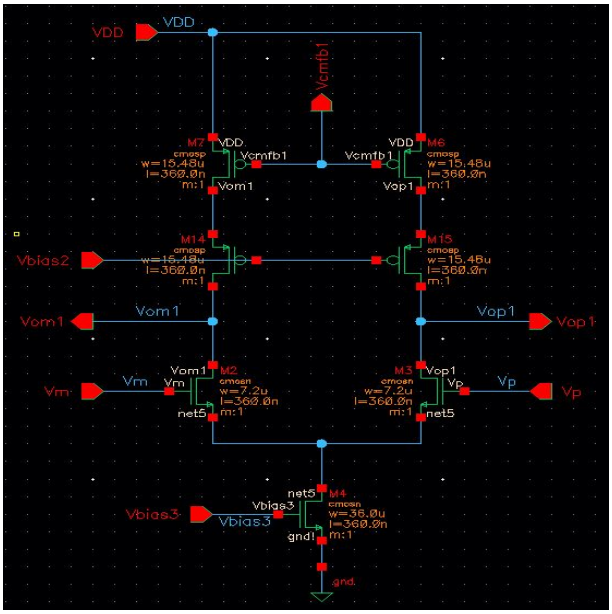

Fig. 5: First stage schematic

III. Common mode feedback loop

The first stage has to be compensated separately to be stable. The appropriate common mode feedback (CMFB) loop is the dual diff-pair (DDP). The topology of the DDP should include the Miller compensation cap $C_{\mathrm{c,CM1}}$. The schematic of the DDP CMFB is given by Fig. 2.3.

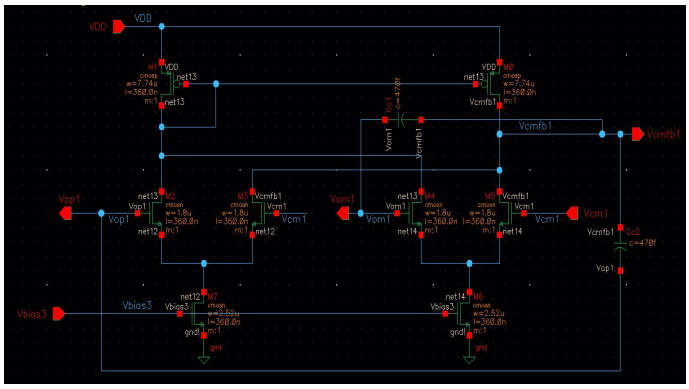

Fig. 6: DDP schematic

IV. Second Stage

A. Specifications

In order to provide sufficient rail to rail output swing, the best candidate is the class-AB stage. I also introduce the Miller cap C_{cDM} to compensate the differential path with the zero nulling R_z to push the RHP zero out to infinity. The schematic is given by Fig. 3.1.

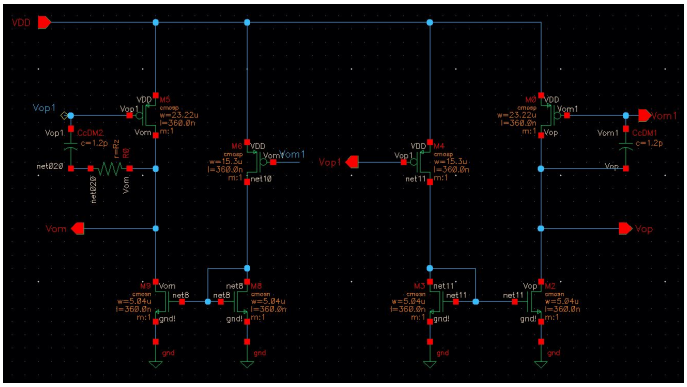

Fig. 7: Second stage schematic

B. Common mode feedback loop

The second stage has to be compensated separately to be stable. The appropriate common mode feedback (CMFB) loop is the current injection. The topology of the current injection should include the Miller compensation cap $C_{\mathtt{c,CM2}}$ and also the error amplifier to match the output common mode voltage with the voltage reference ($V_{\mathtt{CM2}}$ = 0.9 V).
The bias current and widths are scaled down to save power ($I_{\mathtt{c0}}$=I_0/n). Also both stages should have the same current density as follows:

$$\frac{I_0/2}{W_{\mathtt{pmos}}} = \frac{I_{\mathtt{c0}}/2}{W_{\mathtt{cpmos}}} \tag{1}$$

For the current injection CM detector, 1/4 of the current branch injects or removes the current into or from the outputnodes to control theri CM-level. Also 3 by 1 of the DC current split for the bias current of the second stage I_2 used to avoid the potential instability. The schematic of the error amplifier and the symbol are given by Fig. 3.3 and Fig. 3.4, respectively.

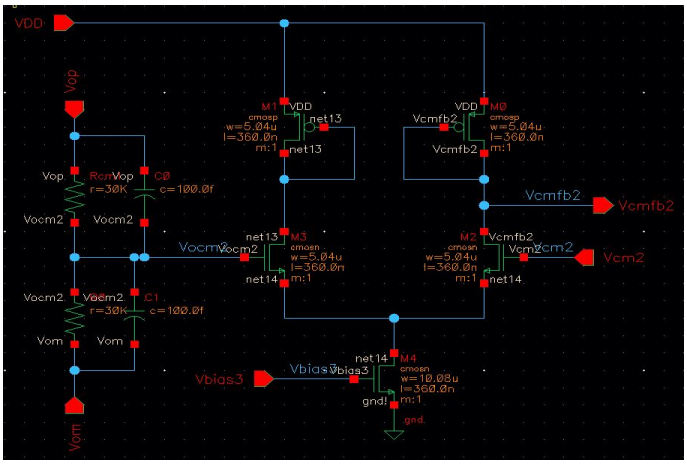

Fig. 8: Error amplifier schematic

The current injection and the relative symbol are given by Fig. 3.5 and Fig. 3.6, respectively.

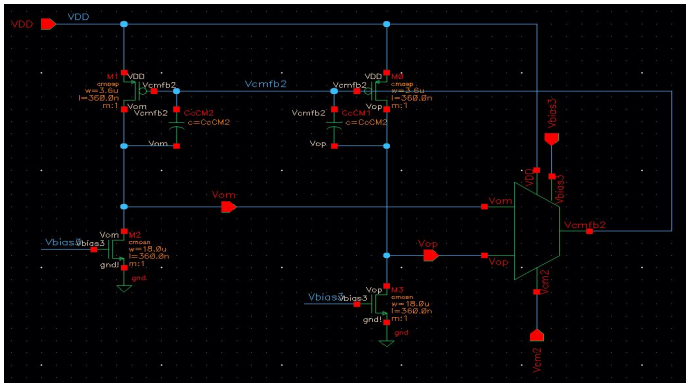

Fig. 9: Current injection schematic

V. Open-loop stability performance

The following table presents the design parameters that I come up with to achieve the opamp performance.

TABLE III: Design parameters

Parameter	Value
R_1	100K
R_2	200K
$R_{\mathtt{CM}}$	30K
$C_{\mathtt{cCM1}}$	0.94 pF
$C_{\mathtt{cCM2}}$	0.1 pF
$C_{\mathtt{cDM}}$	1.2 pF

The schematic of the two-stage opam with **CMDM** probes is given by the following figure.

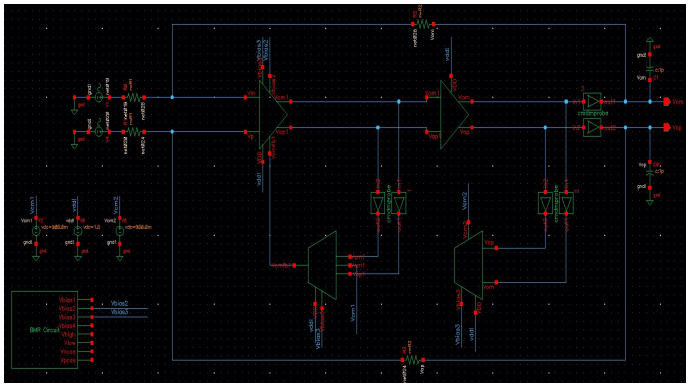

Fig. 10: Two-stage opamp

A. Differential open-loop gain

To measure the differential mode (DM) open-loop gain, I performed an **stb** analysis and I set the **CMDM 3** to -1. The simulation results show an agreement with the requirement detailed in the following table.

TABLE IV: DM open-loop gain results

Parameter	Value
$A_{\mathtt{v,DM}}$	64.84 dB
ϕ_M	63.025 deg
$f_{\mathtt{un}}$	59.408 MHz

The Bode plot of the magnitude and phase of the open-loop gain is given by the following figure.

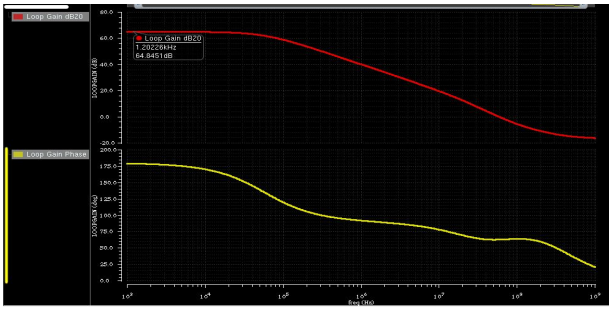

Fig. 11: DM open-loop gain Bode plot

B. First common mode open-loop gain

To evaluate the first CM open-loop gain, I performed an **stb** analysis and I set the **CMDM 1** to 1. The following table summarizes the main results.

TABLE V: First CM open-loop gain results

Parameter	Value
$A_{\mathrm{v,CM1}}$	62.57 dB
ϕ_M	60.077 deg
f_{un}	51.055 MHz

The Bode plot of the magnitude and phase of the open-loop gain is given by the following figure.

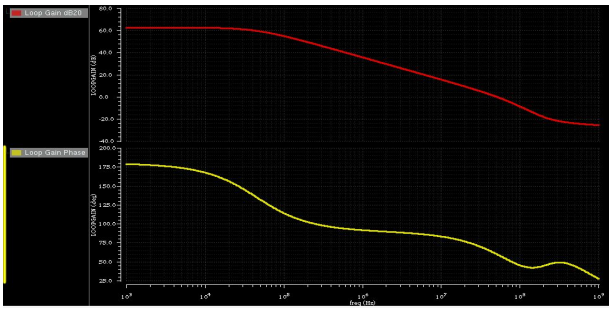

Fig. 12: First CM open-loop gain Bode plot

C. Second common mode open-loop gain

To evaluate the first CM open-loop gain, I performed an **stb** analysis and I set the **CMDM 2** to 1. The following table provides the main results of the open-loop gain of the second CM stage.

TABLE VI: Second CM open-loop gain results

Parameter	Value
$A_{\mathrm{v,CM2}}$	25.445 dB
ϕ_M	63.673 deg
f_{un}	65.94 MHz

The Bode plot of the magnitude and phase of the open-loop gain is given by the following figure.

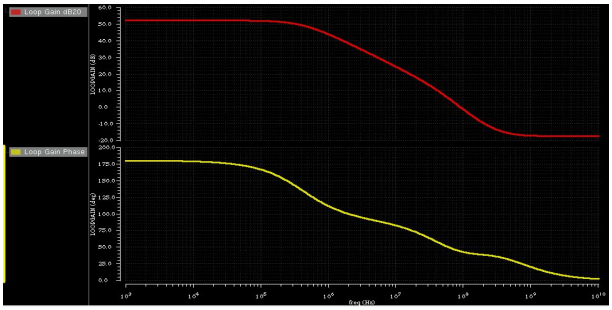

Fig. 13: Second CM open-loop gain Bode plot

VI. Closed-loop gain performance

To evaluate the closed-loop gain, the following steps must be achieved:

1) Remove all CMDM probes from the circuit.
2) For each loop (DM, CM1 and CM2), an AC voltage of 1V magnitude is introduced to the input.
3) Measure the output voltage of each loop.
4) Perform an **ac** analysis of each loop.

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A. Differential closed-loop gain

The main results are detailed in the following table.

TABLE VII: DM closed-loop gain results

Parameter	Value
$A_{\mathrm{v,DM}}$	6.013 dB
f_{3dB}	21.379 MHz

The Bode plot of the magnitude and phase of the closed-loop gain is given by the following figure.

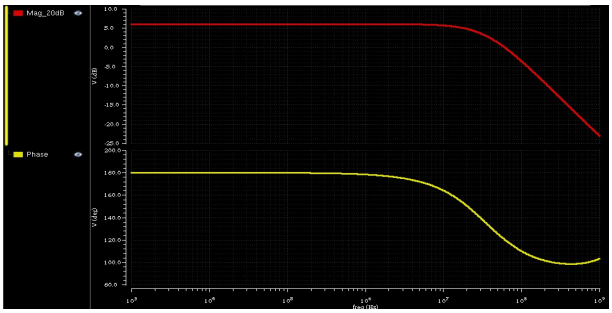

Fig. 14: DM closed-loop gain Bode plot

VII. First common mode closed-loop gain

The main results are detailed in the following table.

TABLE VIII: First CM closed-loop gain results

Parameter	Value
$A_{v,CM1}$	149.646 mdB
f_{3dB}	20.893 MHz

The Bode plot of the magnitude and phase of the closed-loop gain is given by the following figure.

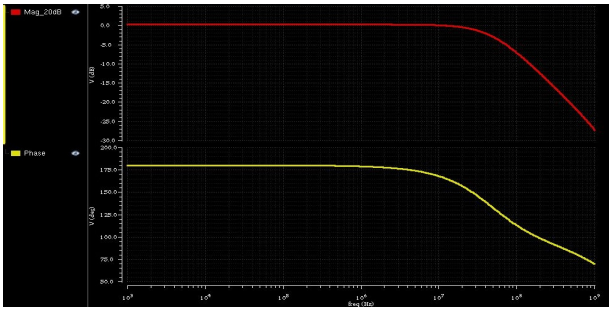

Fig. 15: First CM closed-loop gain Bode plot

VIII. Second common mode closed-loop gain

The main results are detailed in the following table.

TABLE IX: Second CM closed-loop gain results

Parameter	Value
$A_{v,CM2}$	213.508 mdB
f_{3dB}	22.9087 MHz

The Bode plot of the magnitude and phase of the closed-loop gain is given by the following figure.

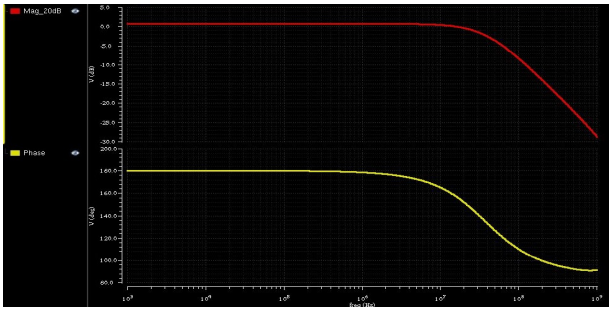

Fig. 16: Second CM closed-loop gain Bode plot

IX. Transient responses

A. Differential step response

To evaluate the differential step response, I introduce a differential step of the following characteristics:

TABLE X: Differential step input parameter

Parameter	Value
Amplitude	200 mV
rise	0.1 ns
fall	0.1 ns

The following figure shows the variations of the differential input and output voltages.

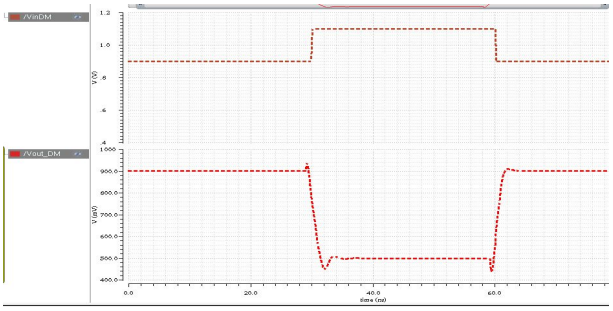

Fig. 17: DM transient response for input step = 200 mV

X. Common mode step response

The following table provides the parameters of the CM step input.

TABLE XI: CM step input parameter

Parameter	Value
Amplitude	100 mV
rise	0.1 ns
fall	0.1 ns

The following figure shows the variations of the common mode input and output voltages.

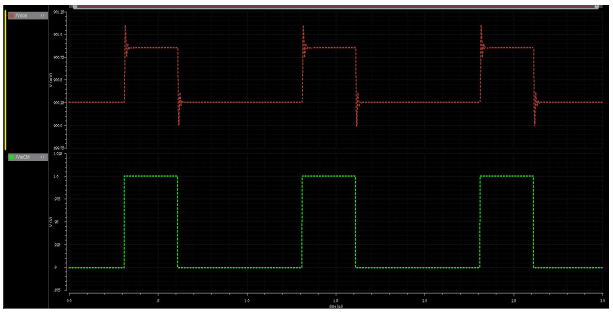

Fig. 18: CM transient response

A. Small and large step inputs

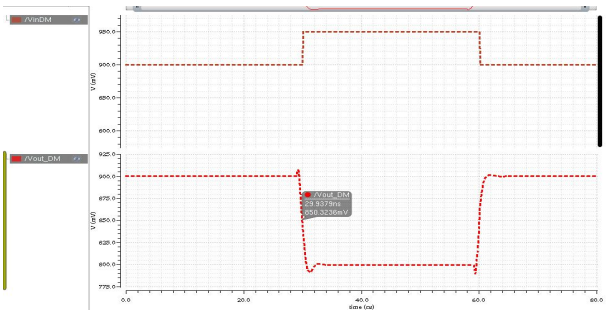

Fig. 19: Small input step = 50 mV

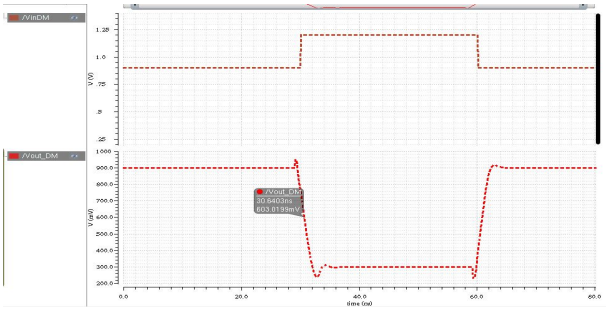

Fig. 20: Large input step = 300 mV

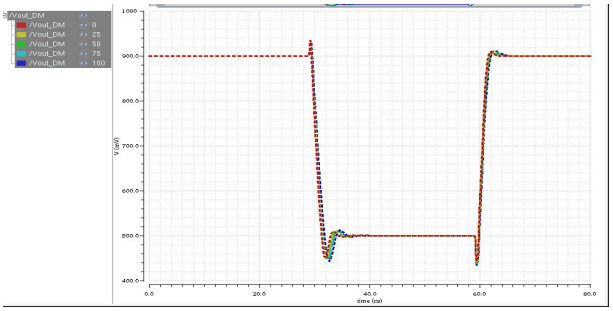

Fig. 21: Temperature variations vs transient DM output voltage

As the differential input step voltages increases, the slew-rate appears and varies. From the figures, as the differential step increases, I noted that the low-to-high settling times decrease while the high-to-low settling times increase. The table below summarizes the values of settling times (high-to-low and low-to-high) with respect to the differential input step voltage.

TABLE XII: DM input step voltage vs Settling times

DM input step	Settling times
50 mV	29.933 ns
300 mV	30.64 ns

XI. Metrics characterization

A. Slew rates

The following table summarizes the dependence of the slew-rates on the differential step input voltages

TABLE XIII: Slew-rates vs DM input step voltage

DM input step	$SR^{+}V/\mu s$	$SR^{-}V/\mu s$
50 mV	137.93	108.69
300 mV	301.51	265.01

B. CMRR

For fully-differential opamp, the CMRR metric is not defined. Thereby, CMRR is infinity. However, the CMRR makes sense for the case of single-ended differential opamp.

C. PSRR

For fully-differential opamp, the PSRR metric is not defined. Thereby, PSRR is infinity. However, the PSRR makes sense for the case of single-ended differential opamp.

XII. PVT characterization

A. Temperature variations

I run a temperature sweeping to control the transient response of the differential output voltage. The following figure illustrate the thermal impact.

I observe that the temperature variations affect the transient response of differential output voltage. In fact, this impact is negligeable for positive slew-rate while charging the capacitors. Nevertheless, as the temperature increases, the charging is longer, while the capacitor gets charged faster for lower temperature value. However, the thermal impact becomes pronounced for negative slew-rate (capacitors discharging). For higher values of temperature, the capacitors take so long for discharging, whereas, the discharching is faster for lower values of temperature.

XIII. Supply voltage variations

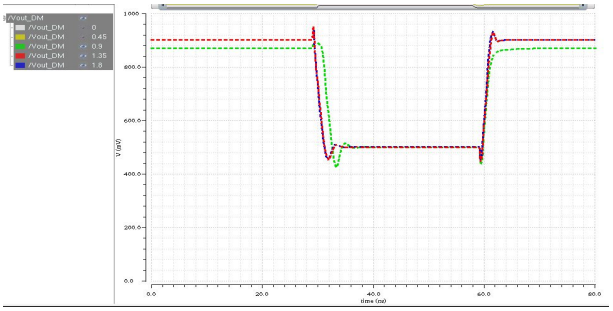

Fig. 22: Supply voltage variations vs transient DM output voltage

The figure above illustrates the dependence of the transient response against the supply voltage variations. For the case of no supply voltage (V_{DD} = 0 V), the MOSFETS are in cut-off region and the total opamp is in OFF-state, and the response is flat. For a supply voltage of 0.45 V, the response is very low, since the gain is deteriorated because many MOSFETs are still in cut-off or operating in triode region. As the supply voltage becomes higher than 900 mV, the two-stage opamp exhibits various response. The capacitors are charging and discharging faster for higher supply voltages. For lower supply voltages, the capacitors are slowly charging but they are discharging at a rate similar to the case of high supply voltages.

XIV. Conclusion

In this project, the design of the two-stage fully-differential opamp is achieved. The stability analysis of the open-loop gain for the two-stage common modes and the differential mode are studied. Based on the design parameters, the open-loops (CM1, 2 and DM) are stable and achieve a phase

margin greater than 60 deg. Also the first common and the differential modes loop-gain achieve sufficient gains greater than 60 dB. In addition, the differential closed-loop achieves a gain of 6 dB and cut-off frequencies higher than 20 MHz, while th CMFB closed-loop achieve gains closer to zeros which confirm the system stability against the common mode disturbance. Furthermore, the design shows slews-rates for various differential input steps higher than 100 $V/\mu s$. Based on those results, the proposed design met the requirements for an opamp of high performance. Furthermore, a framework analysis of the transient responses (common and differential modes) are provided and the opamp design is characterized based on various input steps, slew-rates and PVT variations.

REFERENCES

[1] The Designer's Guide to SPICE and Spectre: http://www.designersguide.org/books/dg-spice/

[2] Specter User Simulation Guide, pages 160-165: http://www.designersguide.org/Forum/YaBB.pl?num=1170321868

[3] https://secure.engr.oregonstate.edu/wiki/ams/index.php/Spectre/STB

[4] M. Tian, V. Viswanathan, J. Hangtan, K. Kundert, *Striving for Small-Signal Stability: Loop-based and Device-based Algorithms for Stability Analysis of Linear Analog Circuits in the Frequency Domain*, Circuits and Devices, Jan 2001. http://www.kenkundert.com/docs/cd2001-01.pdf