Optimizing switching performance of MOSFETs in half-bridge topology

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***Abstract*— This paper presents an empirical approach backed by LTspice simulation to optimize switching performance in half-bridge configuration. For a given layout effective value of RC network in gate drive loop, ways to avoid dV/dt induced false turn-on of MOSFET and remedial circuit for minimizing parasitic oscillation at switching nodes have been presented. Entire study has been validated using LTspice simulation as it's not possible to build a hardware board which can cover all the design aspects authors wanted to cover. Idea is to present a systematic approach which a practicing engineer can adopt for optimizing switching of MOSFET in a given PCB layout.**

***Keywords*– MOSFET, false turn-on, 3-phase inverter, parasitic oscillations, automotive electronics, low voltage electronics.**

I. INTRODUCTION

Designing a power electronic converter is a daunting task. For a given voltage and current rating, several MOSFET may be available in market from different manufacturer. Each manufacture define their datasheet parameters at different test condition. If a universal test condition is adopted by all manufacturer for their datasheet, then, one can just pick MOSFET by comparing parameters in datasheets available from manufacturer, but this is not the case in reality. Therefore, for selection of MOSFETs relying just on datasheet is not a good idea. Best way for selecting MOSFET for a given application is to test the shortlisted MOSFET in the given layout to check their switching behavior. Almost every power electronics converter employs inductive switching, therefore, double pulse test (DPT) is commonly used for accessing switching performance. By performing a DPT, information such as rise time/fall time of voltage and current, dV/dt information, dI/dt information, overshoot of current and voltage, switching losses and presence of gate oscillation, amplitude of miller pulse on the off device due to dV/dt induced gate voltage can be accessed [1]-[2]. Having this information on hand can be useful for determining parasitic elements of circuit layout and apply corrective actions to optimize the circuit the best one could.

Fig. 1 shows a typical DPT circuit and switching waveform obtained using the test setup. First pulse is a wide pulse which is used to build the current to the magnitude which is of interest. This is usually equal to maximum RMS value of load current in the converter topology. Second pulse is a short pulse for measurement purposes and is kept as short as possible [3]-[4]. The DPT are supplied at a very low frequency to allow measurement at constant device temperature and to allow the load to discharge completely between two DPT. By adjusting time T1, T2 and T3, the run-on and turn-off waveforms of the device under test (DUT) can be controlled and measured over the full range of operating conditions. T2 and T3 usually corresponds to minimum duty cycle used in the actual converter. V_{DC} is the DC link voltage.

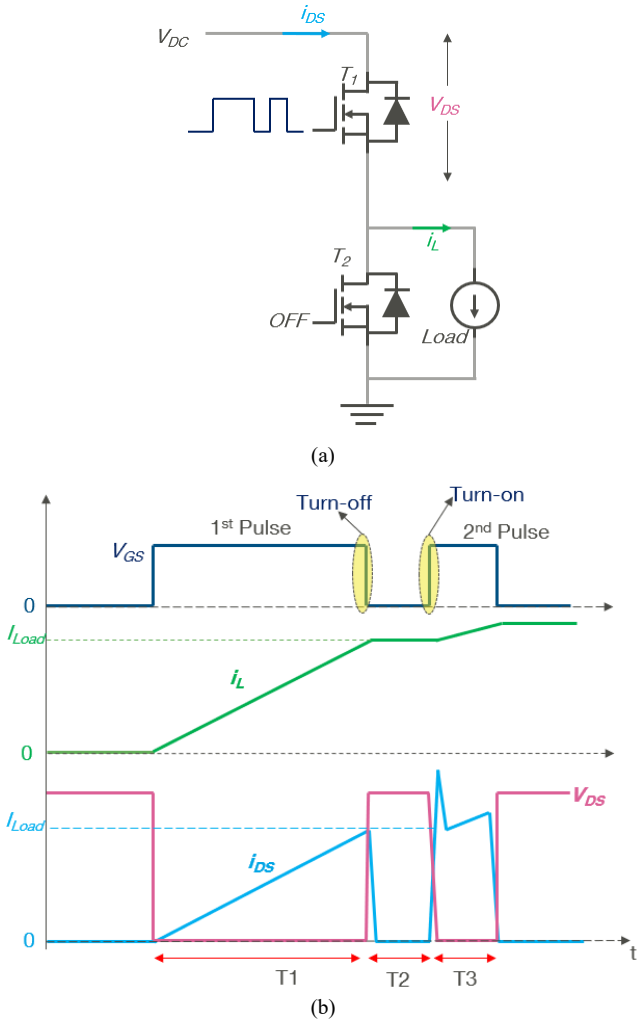

Fig. 1. (a) Double pulse test (DPT) circuit (b) Switching waveform in DPT

It is worth noting that complementary MOSFET T_2 can also be switched with dead time for synchronous operation for observing the effect of dead-time interval on switching performance. Beauty of this circuit is that it effectively represents switching in any converter topology employing

similar switching pole structure, e.g. buck converter, boost converter, half-bridge inverter, full-bridge inverter, 3-phase inverter, multilevel inverter etc. This test allows to optimize the switching behavior of the power frame of the converter without using the actual controller and load. For example, to optimize the power frame of 3-phase inverter for motor drive application, one may not have to use the actual controller and motor load to test and finalize the power frame layout. This in turn allows the hardware engineer working on PCB layout and power frame design to work independently with the firmware engineer working on controller design and vice versa.

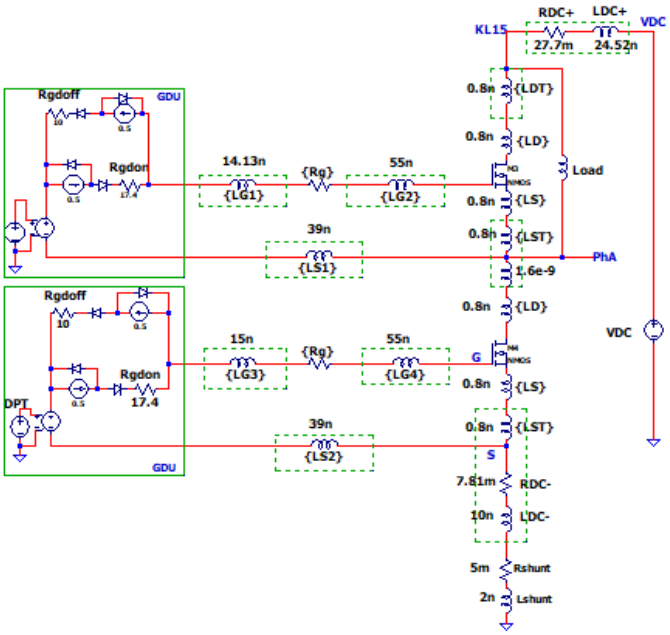

Fig. 2. Half bridge circuit with parasitic elements of PCB layout

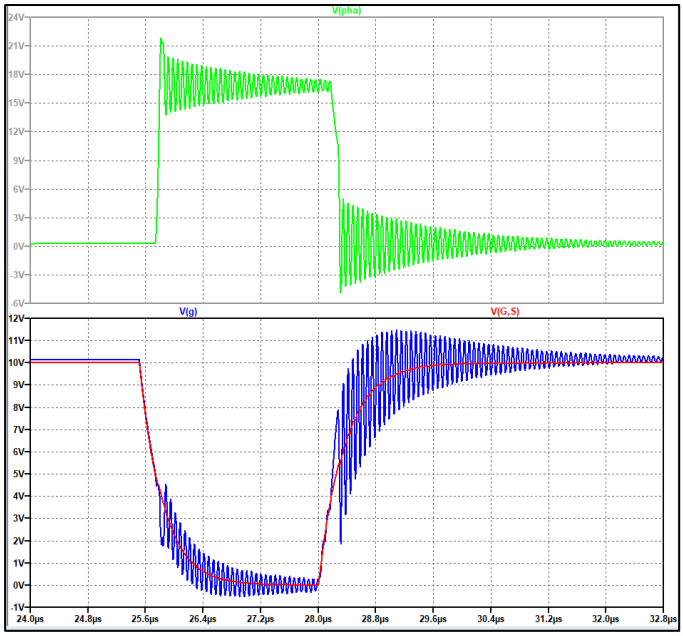

Fig. 3. Ringing on phase voltage (PhA) and gate pin of MOSFET in circuit shown in Fig. 2

Fig. 2 shows the half-bridge circuit which will be used to present the optimization process. Resistance and inductance in dotted box represents the parasitic of the PCB traces. In addition, LD and LS represent the lead inductance of the MOSFET T1 and T2. T1 and T2 is STL64DN4F7AG dual channel automotive grade 40V MOSFET from STMicroelectronics [5]. Targeted application is electronic purge pumps (BLDC motor pumps) used in gasoline vehicles with 12V battery pack. Circuit inside solid green box represents gate driver unit with current limit and different turn-on (R_{GDON})and turn-off (R_{GDOFF}) resistance. Load inductor is fixed to achieve load current of 10A in 25µs assuming switching frequency of 20kHz. Due to parasitic elements of PCB layout and MOSFET package (lead inductances, input/output capacitance) oscillation could be observed on switching nodes (gate, source and drain) of MOSFET as shown in Fig. 3.

Optimization process involves appropriate sizing of gate resistor R_G to meet desired dV/dt rate, selection of external capacitance $C_{GS,Ext}$ connected between gate a-source pin of MOSFET to avoid false turn-on of the MOSFET and snubbers to damp ringing on drain of MOSFET. However, gate resistor not only affect dV/dt rate and overall switching time, but it also influence false turn-on in MOSFET, similarly external capacitance, if not sized properly, will make the switching time longer than desired and will therefore generate loss. Therefore, a systematic approach is needed as switching variables are interlinked to each other and has been discussed in coming sections.

II. Sizing Gate Resistor, R_G

Selection of gate resistor R_G depends on three factors:

(a) Gate driver current limit:

Gate resistor should be high enough that sourcing and sinking current doesn't hit the limit set in GDU. To meet this rule, value of gate resistor is given as:

$$R_{G,tot} \geq \frac{VDD(max)}{I_{limit}} \qquad (1)$$

In eq.(1) VDD(max) is the maximum supply voltage of gate driver unit (GDU). I_{limit} is the peak sourcing and sinking current capability of GDU. $R_{G,tot}$ is the sum of resistance offered by internal circuitry of GDU, internal gate resistance of MOSFET and external gate resistor R_G. In this paper author wants to limit the current drawn from GDU to 250mA to avoid stressing GDU. Using eq. (1), $R_{G,tot}$ is calculated to be 48 Ω for VDD(max) of 12V.

(b) Rate of change of voltage across MOSFET

Rate of change of voltage across MOSFET, i.e., dV/dt rate is inversely proportional to $R_{G,tot}$ and is given by:

$$\frac{dV_{DS}}{dt} = \frac{V_{DD}-V_{GP}}{R_{G,tot}C_{GD}} = \frac{V_{DS}(V_{DD}-V_{GP})}{R_{G,tot}Q_{GD}} \qquad (2)$$

In eq. (2) V_{DS} is voltage across FET, V_{GP} is miller plateau voltage of the FET, Q_{GD} is total gate-drain charge moved during voltage changing across the FET. V_{GP} and Q_{GD} are obtained from the datasheet of STL64DN4F7AG and are equal to 5.5V

and 2.48nC respectively. In automotive application operating voltage range of electronics product is usually 9V to 16V. Switching frequency of purge pump which is essentially a 3-phase inverter driving a BLDC motor is 20kHz. Factors behind selection of dV/dt rate depends upon desired switching speed, EMI performance and factors such as device capability. Detail discussion over choice of dV/dt rate is out of scope of current paper. In this paper, assuming minimum rise time of 50ns for 16V, i.e. dV/dt rate of 0.32V/ns is used for presenting the optimization process. Using eq. (2) value of $R_{G,tot}$ is calculated to be 131 Ω. Fig. (4) shows the effect of gate resistance on dV/dt rate of FET T2. For $R_{G,tot}$ of 131 Ω, rise of approximately 50ns is obtained as can be seen from the time base.

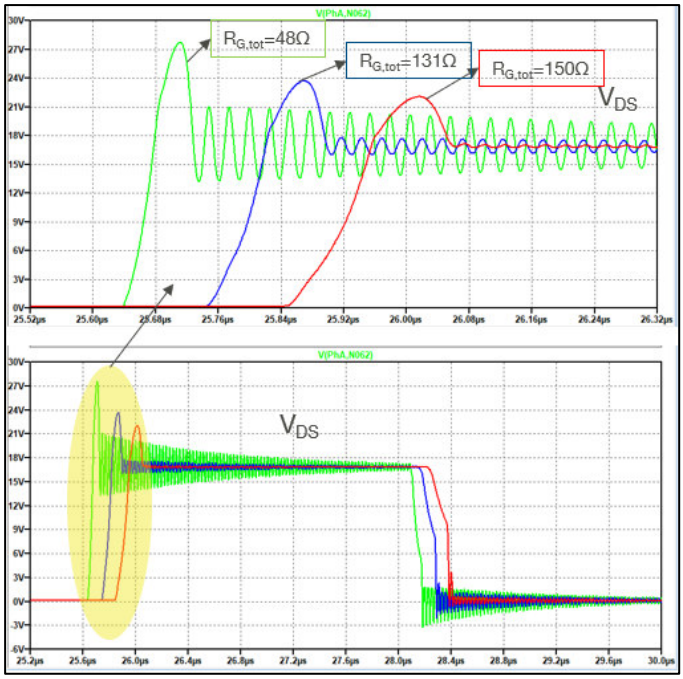

Fig. 4. Simulation result showing slope of drain-source voltage of T2 for different value of R_G

(c) Oscillation in gate drive loop

Oscillation on gate signal is due to two reasons: (i) parasitic components in the gate drive loop (ii) any voltage transients on drain is coupled to the gate due to the presence of miller capacitor C_{GD} between drain and gate of FET.

To illustrate this point, a circuit was created as shown in Fig. 5. Simulation results obtained from the circuit, presented in Fig. 6, shows the oscillation on gate pin of FET. Low frequency oscillation is due to parasitic components in gate drive loop High frequency oscillation is due to oscillation on drain pin which is induced on the gate pin by miller cap C_{GD}. Frequency of induced oscillation is same as frequency of ringing on drain node of MOSFET. Low frequency oscillation on gate pin is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{par}C_{par}}} \qquad (3)$$

In eq. (3) L_{par} is total inductance in gate drive loop. This includes inductance due to PCB traces, MOSFET packaging and GDU inductance in Gate drive loop. C_{par} is total capacitance in gate drive loop. This includes stray capacitances due to PCB layout as well as MOSFET gate source capacitance.

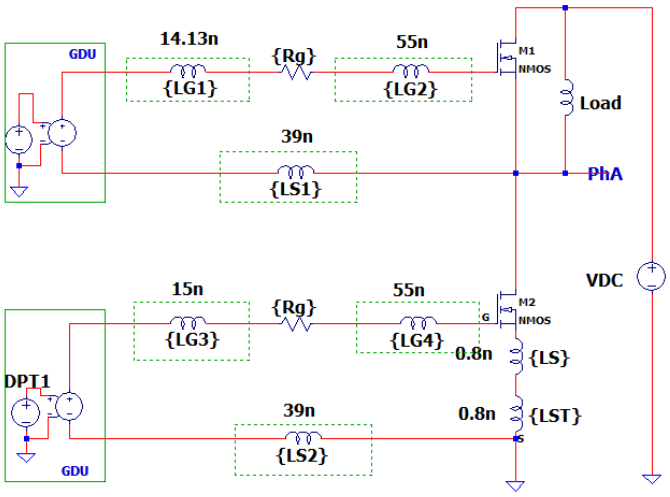

Fig. 5. Simulation circuit used to show oscillations on gate of FET

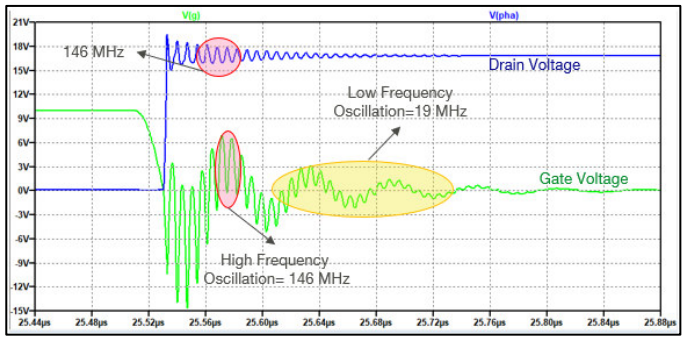

Fig. 6. Simulation result showing oscillation on gate pin of MOSFET M2

Neglecting effect of stray capacitance due to PCB traces, C_{par} is essentially equal to C_{GS} of the FET and can be obtained from the datasheet of the device By measuring the frequency of oscillation f_{osc} using CRO, value of L_{par} can then be easily be calculated using eq. (3). However, for more accuracy C_{par} and L_{par} should be determined experimentally and procedure for determining the parasitic elements has been discussed in later section of this paper. Once f_{osc} and L_{par} is known, value of gate resistance to damp the oscillation is given by:

$$R_{G,tot} = 4\pi\zeta f_{osc}L_{par} \qquad (4)$$

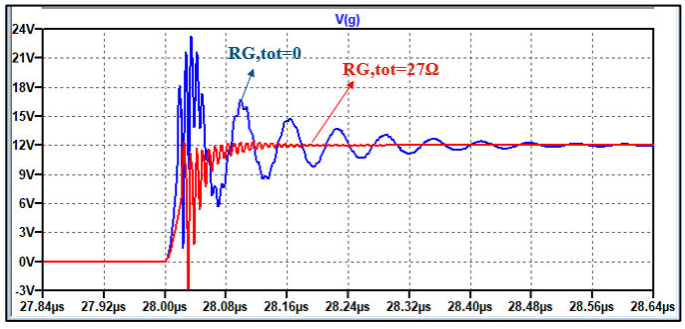

Fig. 7. Effect of gate resistor on oscillation on gate voltage

In Fig. 5, Lpar is 110.6nH and f_{osc} is measured to be 19MHz in Fig. 6. For damping factor ζ equal to 1, $R_{G,tot}$ is calculated to be 27.38 Ω using eq. (4). Fig.7 shows the effect of $R_{G,tot}$ of 27 Ω on gate oscillation. One can observe that low frequency oscillation is completely damped however high frequency induced oscillation remains. A common mistake is to try to damp high frequency oscillation by increasing gate resistor value. Technically high frequency oscillation can also be eliminated by using corresponding value of gate resistor but for damping of 146MHz one would need a resistor of 202Ω. Using such a high value of gate resistor will make the rise time of voltage very slow. One should also realize that for a given layout it's possible that induced oscillation is similar to gate oscillation, in that case a single value of gate resistor can solve the problem of oscillation on gate as well as drain node. If that's not the case, one should always identify the type of oscillation first and then apply appropriate corrective action as described above.

Final value of gate resistor should satisfy all three cases discussed above, therefore, $R_{G,tot}$ should be 131 Ω. Finally, value of R_G is calculated to be: (131-1.3-17.4) Ω = 112.3 Ω. Here 1.3 Ω is internal gate resistor of STL64DN4F7AG and 17.4 Ω is the resistance of the GDU. Nearest standard value of 110 Ω will be used as R_G in this paper.

III. Avoid False Turn-On of Complementary MOSFET

Using Fig. 8 one can understand, if T1 turn-on suddenly, then rate of change of voltage at node U will cause displacement current through Miller capacitor C_{GD} of T2. This current causes voltage drop $V_{GS,off}$ across turn-off resistor of T2. If $V_{GS,off}$ is greater than threshold voltage $V_{GS(th)}$ of T2 it will turn on and will cause direct short circuit across the DC supply.

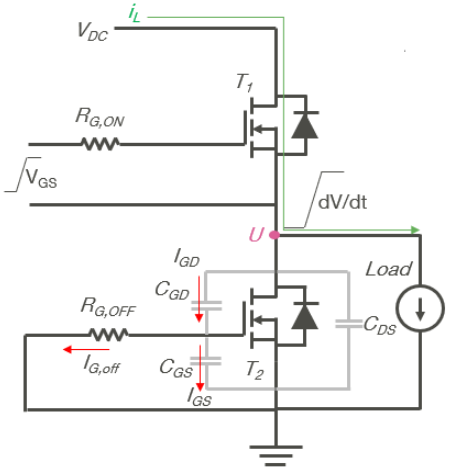

Fig. 8. Circuit showing self-turn-on phenomenon

Using Fig. 8, one can write:

$$I_{GD} = I_{GS} + I_{G,off} = C_{GS}\frac{dV_{GS}}{dt} + \frac{V_{GS,off} - V_{drv}}{R_{G,off}} \quad (5)$$

$$V_{DS} = V_{DG} + V_{GS} \quad (6)$$

In eq. (5), V_{drv} is initial voltage on gate of T2 during start of dV/dt. Using (1) and (2), one can derive the $V_{GS,off}$ as in eq. (7).

$$V_{GS,off} = R_{G,off}C_{GD}\frac{dV_{DS}}{dt}\left[1 - e^{-t/R_{G,off}(C_{GS}+C_{GD})}\right] \quad (7)$$

From (7), $V_{GS,off}$ is rising exponentially with time-constant of $\tau = R_{G,off}(C_{GS}+C_{GD})$ and its peak value is equal to $R_{G,off}C_{GD}\frac{dV_{DS}}{dt}$. To avoid false turn-on one can either reduce the peak value of $V_{GS,off}$ below $V_{GS(th)}$ of T2 or can increase the time constant τ of $V_{GS,off}$.

To reduce the peak value, only option is to reduce $R_{G,off}$, i.e. to use a separate gate resistor for turn-on and turn-off interval. Usually, its common practice to bypass the turn-on resistor R_G using a Schottky diode to limit the voltage generated on gate pin of FET due to dV/dt. However, this method is not very effective in synchronous rectification operation as it also increase the dV/dt rate and resulting current will cause voltage drop across R_{GDON} which is still present. Therefore, overall peak value of $V_{GS,off}$ remains almost the same.

Most effective way to avoid false turn-on is to increase the time constant τ of $V_{GS,off}$ so that it doesn't reach its peak value during dV/dt time period, t. This is achieved effectively by adding an external capacitor $C_{GS,Ext}$ between gate-source pin of FET. If τ>>t then, using Maclaurin expansion e^x=1+x, eq. (7) can be re-written as:

$$V_{GS,off} = \frac{C_{GD}}{C_{GD}+C_{GS}}V_{DS} \quad (8)$$

This essentially means that C_{GD} and C_{GS} behaves like a capacitive divider. If induced voltage becomes greater than V_{th} of the FET, it will turn-on. Therefore, in order to have a low sensitivity to parasitic turn-on, selecting MOSFETs with a high $V_{GS(th)}$ and a large C_{GS}/C_{GD} ratio is of prime importance. Adding external $C_{GS,Ext}$ further increases the C_{GS}/C_{GD} ratio. Note, however, that the gate-source capacitor affects the switching speed of the MOSFET as well as size of bootstrap capacitor will also increase, therefore an optimum value must be selected for a circuit.

To verify eq. (7), an approximate small signal model of MOSFET was simulated as shown in Fig. 9. In the circuit, $R_{G,OFF}$ is 10Ω C_{GS} is 611pF and C_{GD} is 26pF, therefore τ is 6.37ns. Supply of 16V is being turned-on and off in 50ns to have dV/dt of 0.32V/ns.

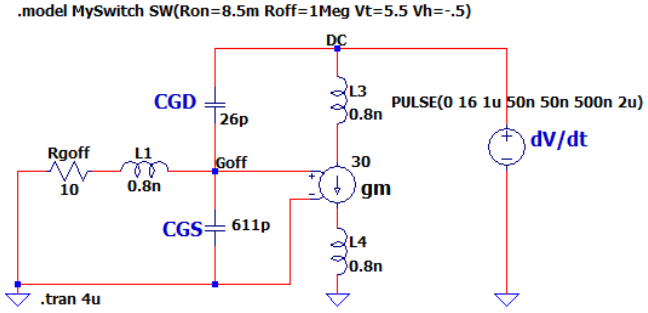

Fig. 9. Circuit for verifying dV/dt induced voltage

Since, in Fig. 9, τ<dV/dt period, $V_{GS,off}$ reaches its peak value of :

$V_{GS,off} = R_{G,off} C_{GD} \frac{dV_{DS}}{dt}$=10*26pF*0.32V/ns=0.0832V

If $R_{G,off}$ is increased to 120Ω, τ increases to 76ns which is greater than dV/dt period. In such a circuit, $V_{GS,off}$ is given by eq. (8) and is calculated to be 0.653V. Fig.10 and Fig. 11 shows the simulation result for both cases, i.e. for τ<dV/dt period and τ>dV/dt period respectively. I_{GD} can also be calculated as:

$$I_{GD} = C_{GD} \frac{dV_{GD}}{dt} = 26pF * .32V/ns = 8.32mA$$

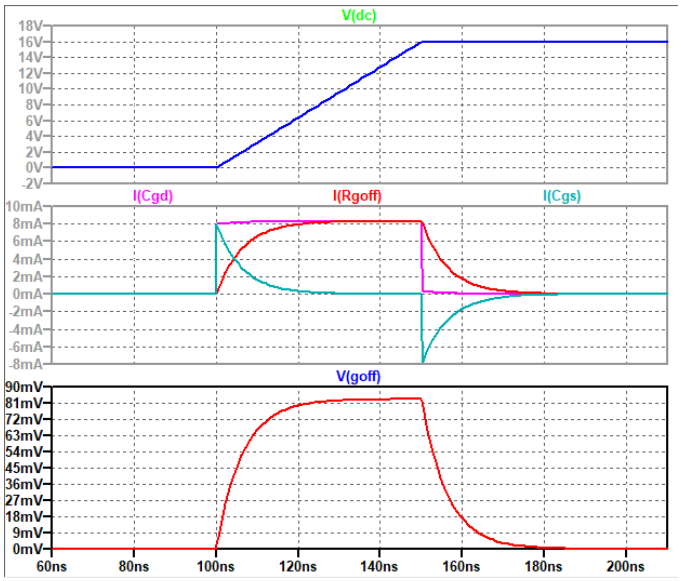

Fig. 10. Simulation Result for τ<dV/dt period

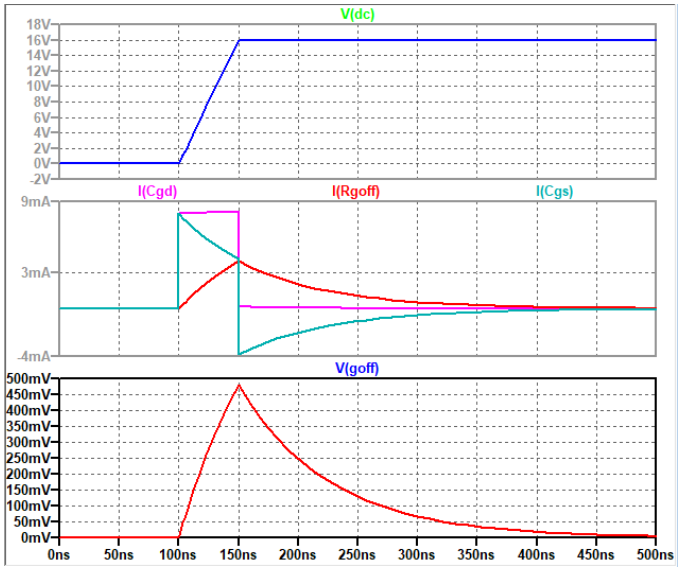

Fig. 11. Simulation Result for τ>dV/dt period

In Fig. 10, one can see that the $V_{GS,off}$ reaches its peak value of 83mV during dV/dt period. In Fig. 11 since τ>dV/dt $V_{GS,off}$ couldn't reach its peak value and start dropping once dV/dt period is over. I_{GD} in each case is independent of $R_{G,off}$ and is equal to 8.32mA.This essentially verifies the concept of dV/dt induced gate voltage on MOSFET.

For the original circuit shown in Fig. 2, $C_{GS,ext}$ is calculated for dV/dt of 0.32V/ns. Considering inductive spike to be 100% of V_{DC}, maximum voltage across the MOSFET will be 32V. For STL64DN4F7AG, minimum value of $V_{GS(th)}$ is 2V, C_{GD} is 26pF and C_{GS} is 611pF. Minimum value of $C_{GS,Ext}$ needed to keep induced voltage at maximum 0.5V is calculated as:

$$C_{GD,Ext} = C_{GD} \frac{V_{DS}}{V_{GS(off)}} - C_{GS} - C_{GD} = 1027 \text{ pF}$$

To provide some design margin, a value of 2.2nF is selected considering non-linear nature of C_{GD} capacitor. Fig. 12 shows the effect of adding $C_{GS,Ext}$ on gate voltage and $V_{GS,off}$ in Fig. 2.

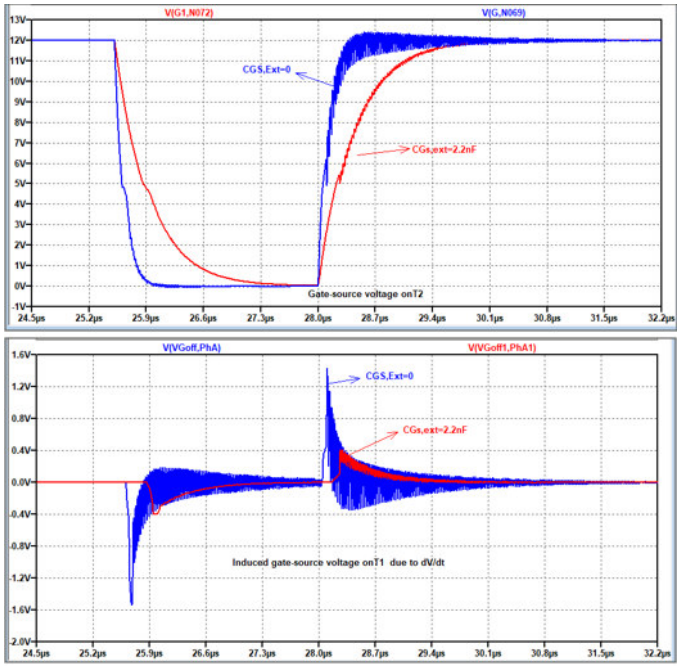

Fig. 12. Simulation result showing effect of adding $C_{GS,Ext}$ in DPT circuit

IV. Minimizing Ringing on Switching Node

Fig. 13 shows the ringing on voltage across MOSFET T1 and T2, of the circuit shown in Fig. 2, during their turn-off instant. For Fig. 13, simulation was done with $C_{GS,Ext}$ of 2.2nF. Reason of ringing has been explained in several literatures [7]. Essentially, during turn-off process, the body-diode of FET draws a peak reverse recovery current and then abruptly snaps off. Since there is a small but finite parasitic inductance in the circuit, the reverse recovery current will circulate through the circuit until it dies down. This will result in voltage overshoot and oscillation at the drain node of FET as observed in Fig. 13.

Fig. 14 shows the leakage current path in the DPT circuit during turn-off of T1 and T2. Frequency of ringing at drain of T1 during its turn-off instant is given as:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{llk} C_{DS1}}} \quad (9)$$

Here, L_{lkg} is total leakage inductance in leakage current path, i.e., $L_{lkg}=L_{lkg1}+ L_{lkg2}+ L_{lkg3}+ L_{lkg4}+ L_{lkg5}+ L_{lkg6}$ and C_{DS1} is equivalent output capacitance of T1. This includes MOSFET drain-source cap C_{DS}, any external capacitance connected

across FET, freewheeling diode capacitance as well as any stray capacitance due to PCB layout.

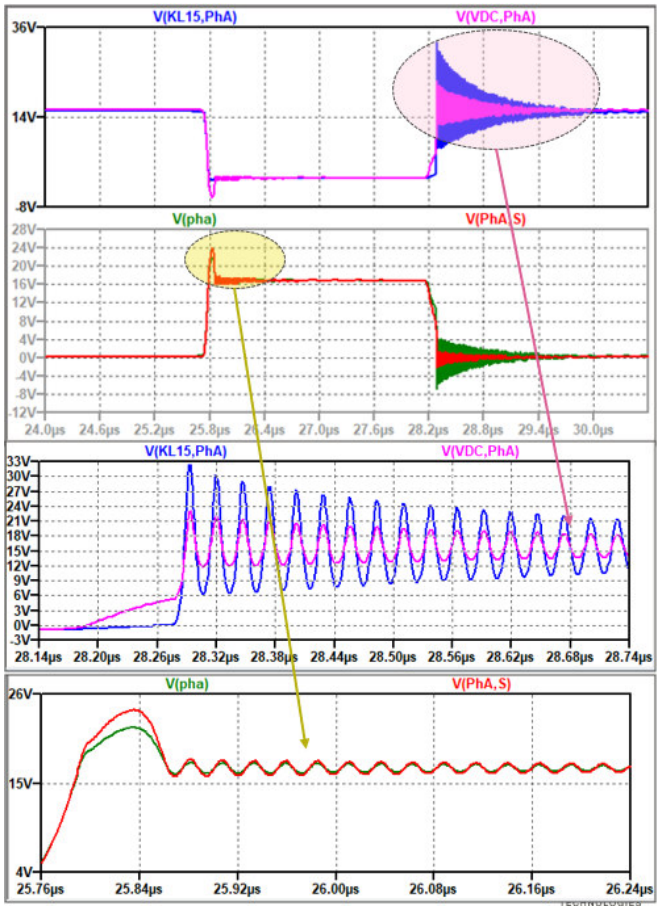

Fig. 13. Ringing at switching node of T1 and T2 MOSFET.

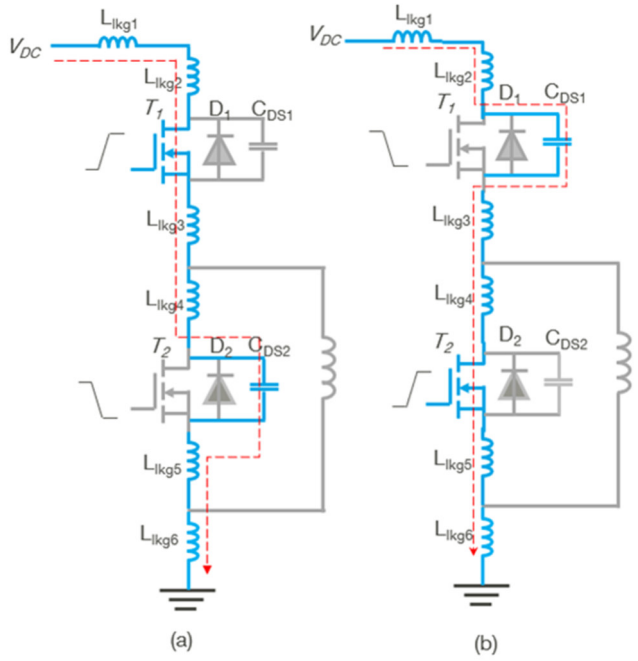

Fig. 14. Circuit showing leakage current path during turn-on and turn-off instant of switches in DPT

f_{osc} doesn't depend upon location of L_{lkg} but only on its total net value which makes it very easy to determine experimentally. Note, however, location of L_{lkg} will affect the magnitude and phase of the ringing though as is evident from the Fig. 13. To determine the f_{osc} experimentally steps described as below could be used:

a) Measure the frequency of oscillation (f_{osc}) on Phase voltage during it fall from V_{DC} to GND level as shown in Fig. 15.
b) Connect a capacitor ($C_{DS,Ext}$) of known value across High Side FET T1 and measure the new frequency of oscillation (fosc1) on phase voltage during its fall from V_{DC} to GND potential as shown in Fig. 16.
c) Calculate the ratio of two frequency: $x= (f_{osc})/(f_{osc1})=2.5$
d) Calculate circuit parasitic capacitance: $C_{DS}= C_{DS,ext}/(x^2-1)=$ 419pF
e) Calculate parasitic inductance of circuit: $L_{lkg}= 1/(4\pi^2 C_{DS} f^2_{osc})=44.2nH$

Total L_{lkg} in simulation circuit is 43.72nH. Therefore, this method gives a very accurate estimate of total parasitic inductance in leakage current path

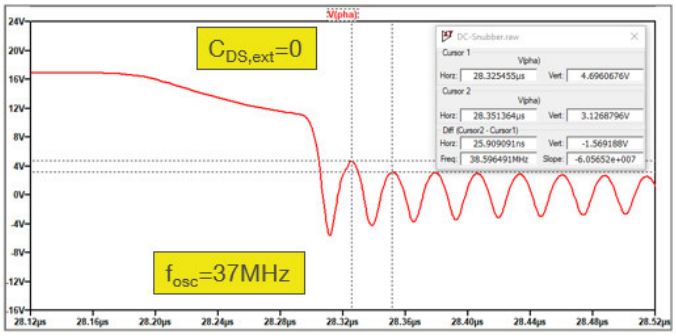

Fig. 15. Phase voltage without any external capacitor across T1

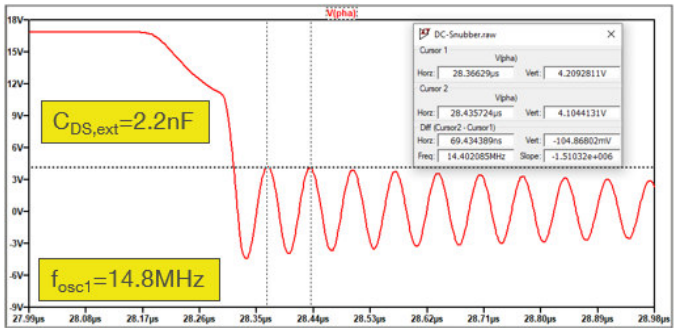

Fig. 16. Phase voltage with external capacitor of 2.2nF across T1

Once L_{lkg} and C_{DS} is determined, a snubber circuit could be designed to minizine the ringing on switching node. There are various snubber topology used for this purpose, such as [7]-[10]: RCD snubber, regenerative snubber, bus side RCD snubber, over-voltage snubber etc. Each have its own merit and demerits, discussion over which is out of scope of this paper. For a low power and low voltage circuit, a simple RC snubber is a good compromise between complexity, cost and available real estate on PCB and therefore will be used in this paper. Fig. 17 shows the equivalent circuit used for RC snubber design.

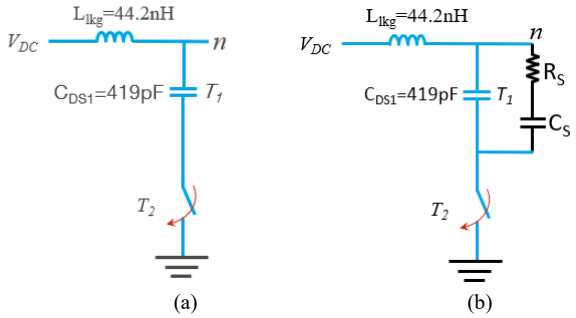

Fig. 17. Equivalent circuit during turn-off of FET in switching pole (a) Without snubber (b) with RC snubber

Neglecting Cs, transfer function of Fig. 17(b) is given as:

$$T(S) = \frac{\omega_{osc}^2}{S^2+S2\zeta\omega_{osc}+\omega_{osc}^2} \quad (10)$$

Here, $\omega_{osc} = \frac{1}{\sqrt{L_{Lkg}C_{DS}}}$ and $2\zeta\omega_n = \frac{1}{R_S C_{DS}}$

Value of Resistance, R_S which snubs the circuit is given as:

$$R_S = \frac{1}{2\zeta\omega_n C_{DS}} = \frac{1}{2\zeta}\sqrt{\frac{L_{lkg}}{C_{DS}}} \quad (11)$$

In half-bridge circuit, one cannot just have a resistor mounted directly across FET as it will permanently short that FET. Therefore, a capacitor Cs is put in series with R_S to RC snubber. Reasonable damping occur at ζ=0.5, therefore,

$$R_S = \sqrt{\frac{L_{lkg}}{C_{DS}}} = \sqrt{\frac{44.2nH}{419pF}} = 10.27\Omega$$

Snubber capacitor is selected so that ringing frequency is easily passed but all lower frequency and DC are blocked. For convenience it is nice to choose a frequency that 2π times lower the RC cut-off frequency [11]. Therefore,

$$C_S = \frac{3}{R_S f_{osc}} = 1/(10.27\Omega * 37MHz) = 7.89nF$$

Using a higher value of capacitor will provide overdamping but will also increase loss in R_S [11]. Time constant of RC snubber should be small compared to the shortest expected on-time of the FET. Fig. 18 shows the simulation of Fig.17 with and without RC snubber.

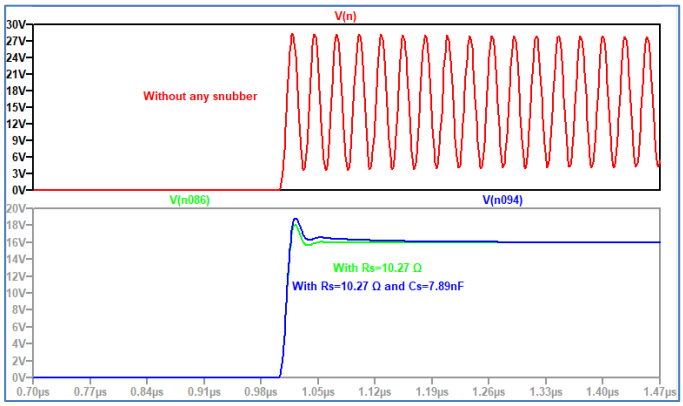

Fig. 18. Effect of using RC snubber on voltage at node 'n'

Once RC snubber is calculated, optimisation process is complete. In final circuit a practical value of Rs=10Ω and Cs=10nF was used. Fig. 27 shows the final circuit with calculated R_G, $C_{GS,Ext}$ and RC snubber.

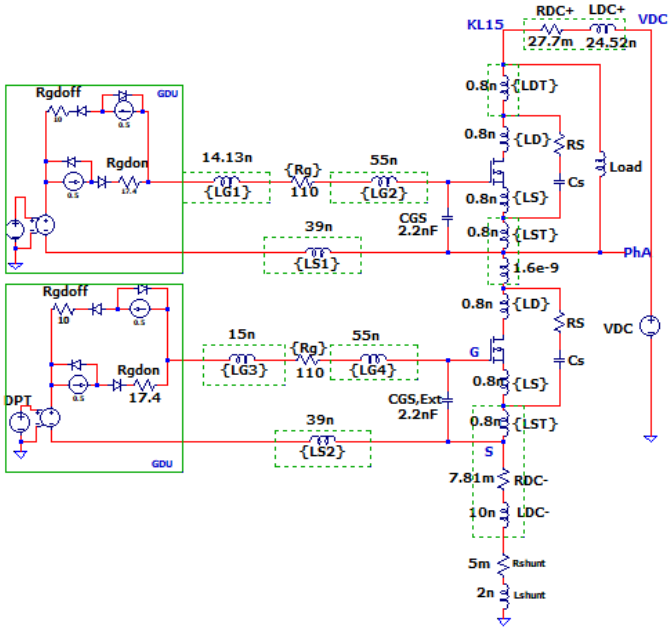

Fig. 19. Final optimised circuit.

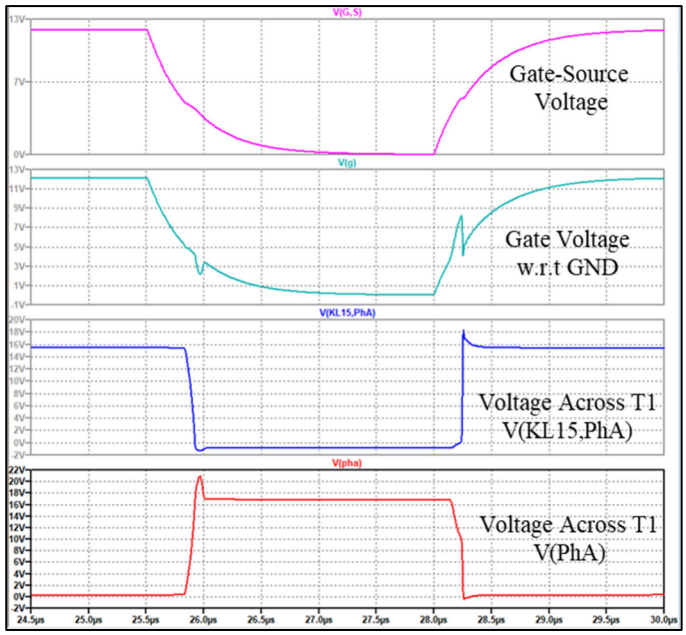

Fig. 20. Simulation result showing switching node voltage for optimised circuit.

In Fig. 20 one can see that ringing on gate, drain and source pin of MOSFET is damped. A dV/dt rate of 0.18V/ns is achieved. Due to addition of snubber rise time of phase voltage increases from 50ns to 87ns which is within the design requirement of achieving minimum rise time of 50ns.

V. CONCLUSIONS

This paper presents an analytical design methodology backed by LTspice simulation for optimising switching performance in half-bridge MOSFET circuit. In such a half-bridge circuit, design variables are depended on each other. For example, gate resistor value not only affect the oscillation in the gate drive loop but also affect the switching rate of the MOSFET. It is shown in this paper that oscillations on the gate pin of MOSFET is due to parasitic elements in gate-drive loop as well as due to the induced oscillation which is coupled to the gate from drain through Miller cap. This paper showed the difference between both type of oscillations and corrective action needed to minimize both type of oscillation. Gate resistor value is calculated to damp the oscillation due to parasitic elements in gate-source loop. Since gate resistor also affect the dV/dt rate, its important to not oversize it. Paper also showed the rational behind selecting proper value of external gate-source capacitance used in circuit for avoiding false turn-on of the MOSFET. Finally, dV/dt induced oscillation as well as oscillation on drain of MOSFET is damped using snubber circuit. Following the design methodology presented in this paper any half-bridge circuit can be optimised to meet the design goal.

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