Junction temperature of CMOS electronics cooled by a regenerative cryocooler

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Abstract

The optimal operation of cryo-CMOS electronics requires accurate knowledge of the junction temperature, which may be derived from the design parameters of the mechanical cryocooler and cryospace. Research on the subject has been mostly restricted to limited examples of coupled cryocooler-cryocomputer operation with little quantitative analysis. Here, we develop and experimentally validate an analytical relation between the junction temperature and the parameters of the cryogenic system for the steady-state. For validation, a printed circuit board was placed into the cryospace and cooled to 173 K using a regenerative cryocooler based on the reversed Stirling cycle. The junction temperature was measured in five experiments as a function of five different input clock frequencies. The analytical relation for the junction temperature showed good accuracy with the coefficient of variance of ±2%, the mean biased error of –2%, and the determination coefficient of 0.92. The result of this work permits determining accurately the steady-state junction temperature of a cryo-CMOS electronics in a wide range of cryogenic temperatures for different types of cryocoolers.

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I Introduction

The scaling of silicon transistors below 5 nm to increase computer performance is an arduous task, and it is yet unclear whether this nanoscale technology will entail radically different applications or will merely be used in a conventional fashion. According to Khan *et al.* (2018), "*the semiconductor industry is on the verge of entering uncharted territory for the first time in more than 50 years*", but Kuzmicz (2017) states that silicon-based electronics "*will remain the key technology for logic gates for the next decade or two*". The matter has important implications in the burgeoning sector of quantum computing, and particularly for the application of cryogenic complementary metal–oxide–semiconductor (cryo-CMOS) electronics (Xue *et al.*, 2021). However, fundamental problems still preclude the complete control of qubits-based technologies that would enable the full development of quantum computers (Dyakonov, 2020).

Another approach worth considering is the operation of silicon-based semiconductors or technology under cryogenic temperatures below 77K (Krane *et al.*, 1988; Carlson *et al.*, 1989; Clark *et al.*, 1992; Rose *et al.*, 1999). The empirical findings conclusively showed positive improvements in the operation of CMOS electronics, such as a nine-fold reduction of resistivity, a two-fold or larger increase in clock rate, increased time before first DRAM charge retention failures from several seconds to several hours. The results also suggested the improvement circuit reliability by a factor of 10^{15} against processes activated by higher temperatures, such as diffusion, electromigration, and chemical reactions that follow an Arrhenius law. High-temperature superconductor materials can improve the performance further (Holmes *et al.*, 2013).

Technology feasibility studies of IBM in the early 1990s concluded that no fundamental technical problems existed for cryogenic computing, and the best choice for cooling was the Stirling cycle heat pump. This technology recycles (regenerates) part of the produced cold back

into the process and does not rely on greenhouse refrigerants for its operation (Chu, 1999). However, at that time, the conventional transistor scaling and ambient operation were understandably cheaper than using cryocomputers. The latter implied additional cooling cost, system reliability, and "*the need to redesign the technology for optimized low-temperature operation*" (Isaac, 2000). The advent of cryo-CMOS electronics as a natural choice for semiconductor-based qubits (Giustino, 2021), physical limits to miniaturize transistors, and a limited number of feasible alternatives for computing technologies (Adamatzky, 2014) motivate to resume experimental work in cryocomputing (Ungerer & Carpenter, 2018, p. 59). The work conducted in the 1980s and 1990s was primarily focused on the fundamental properties of cryo-CMOS electronics using liquid nitrogen. Therefore, the literature is scant with empirical analysis of joint CMOS and cryocooler (cryogen-free) operation and data about designs, materials and performance. The present work provides critical insights into the operation of a joint system "CMOS electronics—cryospace—electricity-based mechanical cryocooler". Here, *cryospace*, means the space or thermal chamber isolated from the external environment and cooled by a cryocooler. An object of cooling would be located inside this chamber.

This paper aims to find the answer to the question, *what is the fundamental relationship between the junction temperature of the semiconductor electronics and the known and controllable parameters of the cryospace?* Answering this question will help:

1) design and control cryospaces using electrical cryocoolers for advanced products in electronics and biomedicine, which require cryogenic temperatures;
2) increase the calculation power of computers using traditional CMOS technology;
3) design and control the coupled operation of cryospaces and cryo-CMOS electronics for quantum computing.

This work contributes to finding the solution to the research question by developing and experimentally validating an analytical equation between the semiconductor junction temperature and design and operational parameters of the cryospace cooled by a regenerative cryocooler. The article is organized as follows. The following section describes the object of analysis, derives the analytical equation for predicting the junction temperature and discusses the methodology for the validation experiment. Section III shows the experimental results. Section IV discusses the results, limitations and future work. Section V concludes on the findings.

II Methodology

II.1 Object of analysis

The object of analysis is the thermo-mechanical system "Stirling cryocooler—Thermal chamber—CMOS printed circuit board (PCB)" ("the system"), shown in Fig. 1a. In the figure, T_{atm} is the atmospheric temperature (K), T_c is the cryocooler temperature (K), $T_g^{st.s}$ is the steady-state gas temperature in the thermal chamber ("TC") (K), T_s is the surface temperature of the heat source, the CMOS integrated circuit (K) ("IC"), and T_j is the junction temperature of the IC semiconductor (K). An electromotor drives the Stirling cryocooler ("SC"). The latter converts mechanical work into cooling capacity and cools the gas in the TC. The heat transfer is mostly due to forced convection initiated by the gas (air), circulated in the chamber by the electrical fan.

Figure 1b depicts the thermo-electrical analogy of the system. We used this analogy to model thermal balance in the chamber. In Fig. 1b, q_c is the cooling capacity of the SC (W), q_L is the sum of all parasite heat leaks from the atmospheric environment (W), q_s is the heat flow from
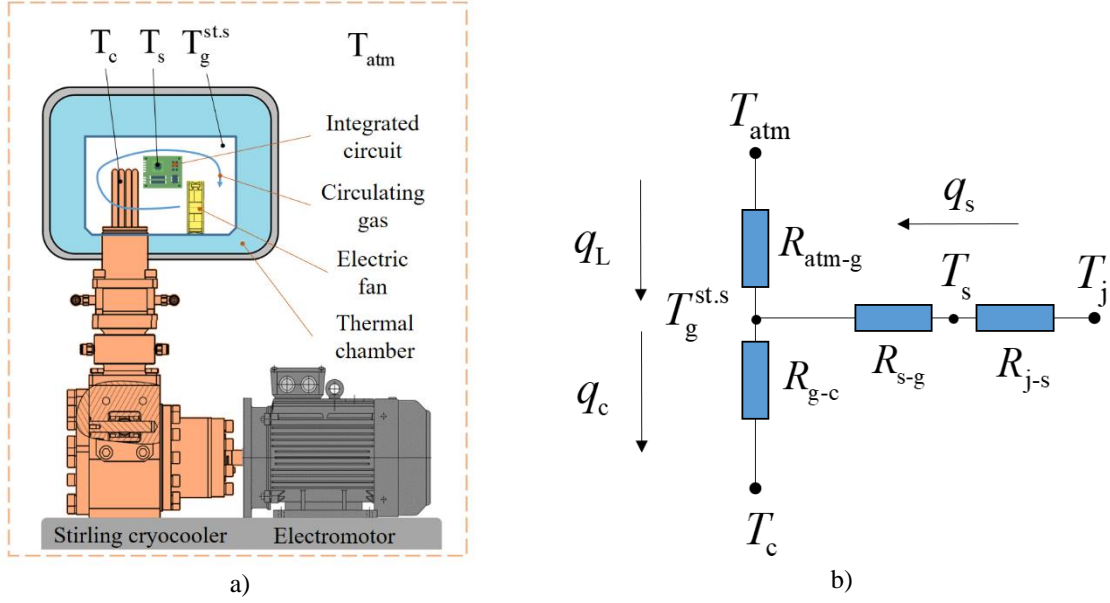
Fig. 1. The system "Stirling cryocooler—Thermal chamber—CMOS printed circuit board": a) principal diagram with key elements, b) Thermal-electrical analogy.

Table 1. Characteristics of the system's key elements.

Stirling cryocooler	
Charge pressure, p	1.4 MPa
Shaft frequency, f	9.1 Hz
Radiator temperature, T_r	287 K
Design constant, S_c	90.2
Otaka number for given p and f, Θ	0.078
Working fluid	Helium
Width × height × depth	262 × 474 × 205 mm
Thermal chamber	
Circulating gas	Air
External width × height ×depth	330 × 250 × 425 mm
Internal width × height ×depth	225 × 135 × 275 mm
External surface area	0.724 m^2
Internal surface area	0.259 m^2
Heat conductance of the wall	0.040 W·m^{-1}·K^{-1}
Room temperature, T_{atm}	297 K
Integrated circuit	
IC type	CD4049UBE
Number of ICs on the PCB	3
Width × height ×depth	20 × 5 × 7 mm
Effective heat transfer area of IC	0.0033 m^2
Junction-to-case (top) thermal resistance, R_{j-s}	36.8 K·W^{-1}

an internal source (W) (in this case—an IC), $R_{\text{atm-g}}$ is the total thermal resistance of the system "atmosphere-gas" ($\text{K} \cdot \text{W}^{-1}$), $R_{\text{g-R}}$ is the thermal resistance of the system "gas-SC" ($\text{K} \cdot \text{W}^{-1}$), $R_{\text{s-g}}$ is the thermal resistance of the system "heat source-gas" ($\text{K} \cdot \text{W}^{-1}$), and $R_{\text{j-s}}$ is the thermal resistance of the system "semiconductor juncture-heat source surface" ($\text{K} \cdot \text{W}^{-1}$). Table 1 lists essential operational, geometrical and thermal parameters of the integrated circuit and the Stirling cryocooler test rig (Smirnov *et al.*, 2019).

II.2 Predicting the junction temperature of the CMOS IC

We first derive an analytical expression for the steady-state temperature of the gas in the chamber as a function of cryocooler control parameters and environment conditions. In a previous work (Smirnov & Ouerdane, 2021), we found and experimentally validated the relation for the steady-state gas temperature in the thermal chamber T_{g} :

$$T_{\text{g}}^{\text{st.s}} = \frac{R_{\text{g-c}} \cdot T_{\text{atm}}}{R_{\text{atm-g}} + R_{\text{g-c}} - \dfrac{R_{\text{atm-g}}}{R_{\text{g-c}} \cdot S_{\text{c}} \cdot \Theta \cdot f \cdot p \cdot \dfrac{1}{T_{\text{r}}} + 1}} = \frac{R_{\text{g-c}} \cdot T_{\text{atm}}}{R_{\text{atm-g}} + R_{\text{g-c}} - \dfrac{R_{\text{atm-g}}}{R_{\text{g-c}} \cdot C + 1}} = \gamma \cdot T_{\text{atm}} \tag{1}$$

where the constant S_{c} characterizes the Stirling cryocooler design structure $\left(\text{cm}^3\right)$, Θ is the Otaka number that describes the cryocooler performance (Otaka, 2002), f is the frequency of the cryocooler cycle (Hz), p is the charge pressure (MPa), and T_{r} is the temperature of the cryocooler's radiator (K). The frequency and charge pressure were not changed during the experiments; therefore, the value of the cryocooler operational complex C is constant and can be calculated from the values in Table 1. Thermal resistances were constant for the system studied in this work and equal to $R_{\text{atm-g}} = 2.687 \, \text{K} \cdot \text{W}^{-1}$ and $R_{\text{g-c}} = 0.771 \, \text{K} \cdot \text{W}^{-1}$ correspondingly. We call the

parameter γ in Eq. 1 a *cryospace modifier*, which is equal to 0.563. This parameter will become

relevant in the derivations below.

Our objective is to find an analytical relation between the steady-state junction temperature

and other *controllable* parameters in the system. Let us first find the expression for the temperature

of the gas inside the thermal chamber as a function of heat source and heat sink parameters. Heat

sources include heat leaks from the atmosphere q_L and heat generated inside the chamber by the

heat source q_s (IC). The heat sink is the heat q_c flowing to the cryocooler. For the steady-state

conditions, the relation for the heat conservation reads:

$$q_c = q_L + q_s \tag{2}$$

$$q_c = S_c \cdot \Theta \cdot f \cdot p \cdot \frac{T_c}{T_r} \tag{3}$$

$$q_c = \frac{T_g - T_c}{R_{g\text{-}c}} \tag{4}$$

$$q_L = \frac{T_{atm} - T_g}{R_{atm\text{-}g}} . \tag{5}$$

Equation 3 is the Otaka equation for the cryocooler cooling capacity. Equations 4 and 5

follow from the thermal-electrical circuits analogy. Using equations from 2 to 5, we find the

steady-state gas temperature in the chamber as a function of thermal properties, cryocooler

parameters, and the heat source power:

$$T_g = \frac{R_{g\text{-}c}\left(\dfrac{T_{atm}}{R_{atm\text{-}g}} + q_s\right)}{1 + \dfrac{R_{g\text{-}c}}{R_{atm\text{-}g}} - \dfrac{1}{R_{g\text{-}c} \cdot C + 1}} = q_s \cdot \gamma \cdot R_{atm\text{-}g} + \gamma \cdot T_{atm} . \tag{6}$$

Now, let us derive the relation for the junction temperature T_j. Heat dissipated from the IC into the environment of the gas chamber can be characterized by two relations:

$$q_s = h_{s\text{-}g} \cdot A_s \cdot \left(T_s - T_g \right) \tag{7}$$

where $h_{s\text{-}g}$ is the heat transfer coefficient between the heat source wall and the flow of cold gas ($W \cdot m^{-2} \cdot K^{-1}$) and A_s is the heat transfer area (m^2). The second relation reads:

$$q_s = \frac{T_j - T_s}{R_{j\text{-}s}} \tag{8}$$

where $R_{j\text{-}s}$ is the thermal resistance of the IC ($K \cdot W^{-1}$). This value is provided by the IC manufacturer (Table 1). Using equations 6, 7 and 8, the relation for the junction temperature T_j as a function of controllable parameters of the system reads:

$$T_j = q_s \left(R_{j\text{-}s} + \frac{1}{h_{s\text{-}g} \cdot A_s} + \frac{R_{g\text{-}c} \cdot R_{atm\text{-}g}}{R_{atm\text{-}g} + R_{g\text{-}c} - \dfrac{R_{atm\text{-}g}}{R_{g\text{-}c} \cdot C + 1}} \right) + \frac{R_{g\text{-}c} \cdot T_{atm}}{R_{atm\text{-}g} + R_{g\text{-}c} - \dfrac{R_{atm\text{-}g}}{R_{g\text{-}c} \cdot C + 1}} . \tag{9}$$

The estimation of the heat transfer coefficient $h_{s\text{-}g}$ was carried out using the classical empirical relation for the Nusselt number around a hot plate for the characteristic length L in the laminar flow with thermal conductivity k:

$$Nu = \frac{h_{s\text{-}g} L}{k} = 0.664 \cdot Re^{\frac{1}{2}} \cdot Pr^{\frac{1}{3}} . \tag{10}$$

The gas main flow speed was $1 \ m \cdot s^{-1}$, air thermal properties were selected using standard tables for the temperature $T_g = 173 \ K$. The characteristic length L was assumed as the wetted contour of the IC parallel to the flow, 17 mm. The effective heat transfer surface was assumed as

one third of the total area of the PCB, where the three ICs were mounted with a fin coefficient of 1.1 to account for the influence of a thermocouple and other electronics and structural elements, 0.0033 m^2.

Simplifying the Eq. 9 using $R_{\text{s-g}} = 1/(h_{\text{s-g}} \cdot A_{\text{s}})$ and the notion of the cryocooler modifier γ (Eq. 1), we find:

$$T_{\text{j}} = q_{\text{s}} \cdot \left(R_{\text{j-s}} + R_{\text{s-g}} + \gamma \cdot R_{\text{atm-g}} \right) + \gamma \cdot T_{\text{atm}} \tag{11}$$

$$\gamma = \frac{R_{\text{g-c}}}{R_{\text{atm-g}} + R_{\text{g-c}} - \dfrac{R_{\text{atm-g}}}{R_{\text{g-c}} \cdot S_{\text{c}} \cdot \Theta \cdot f \cdot p \cdot \dfrac{1}{T_{\text{r}}} + 1}} . \tag{12}$$

Equation 11 shows the relation of the junction temperature to known and controllable parameters of the cryocooler and the cryospace. The summation in brackets represents the total thermal resistance that dissipates the heat generated by the IC in the cryospace with the ambient temperature $T_{\text{g}} = \gamma T_{\text{atm}}$. Equation 11 can be utilized to control the junction temperature of cryogenic CMOS electronics. Before we move to the experiment, let us analyze the properties of the cryospace modifier.

We first would like to analyze a possible range of values that γ might take and, at the same time, make a preliminary verification of the model results. Four limit cases are noteworthy and described in Table 2 below. Detailed calculations of the limits are in the Appendix. The solution for Case 1 implies that if there is no heat flow between the cryospace and the room, the heat from the IC flows directly to the cryocooler. There is no cooling in Case 2 and 3 because the cryocooler is not working or is effectively isolated. The thermal path goes from the IC to the room environment through the resistances of the thermal chamber. Case 4 is less pronounced than the

previous three. It represents the situation of an ideal contact between the cryocooler and the gas in the cryospace.

Table 2. Analysis of limit cases for the junction temperature equation (Eq. 11)

Limit case	Case 1 Perfect isolation between the cryospace and environment	Case 2 The cryocooler is non-functional	Case 3 The cryocooler is perfectly isolated from the cryospace	Case 4 Perfect heat transfer between the cryocooler and the cryospace
	$R_{\text{atm-g}} \to \infty$	$C = S_c \cdot \Theta \cdot f \cdot p \cdot \dfrac{1}{T_r} = 0$	$R_{\text{g-c}} \to \infty$	$R_{\text{g-c}} \to 0$
Solu-tion	$\gamma = 0$ $q_s = \dfrac{T_j - T_c}{\left(R_{\text{j-s}} + R_{\text{s-g}} + R_{\text{g-c}} \right)}$	$\gamma = 1$ $q_s = \dfrac{T_j - T_{\text{atm}}}{\left(R_{\text{j-s}} + R_{\text{s-g}} + R_{\text{g-atm}} \right)}$	$\gamma = 1$ $q_s = \dfrac{T_j - T_{\text{atm}}}{\left(R_{\text{j-s}} + R_{\text{s-g}} + R_{\text{g-atm}} \right)}$	$\gamma = \dfrac{1}{R_{\text{atm-g}} \cdot C + 1} = \dfrac{R_c}{R_{\text{atm-g}} + R_c}$ $q_s = \dfrac{T_j - T_{\text{atm}} \cdot \dfrac{R_c}{R_{\text{atm-g}} + R_c}}{\left(R_{\text{j-s}} + R_{\text{s-g}} + \dfrac{R_{\text{atm-g}} \cdot R_c}{R_{\text{atm-g}} + R_c} \right)}$

To understand the meaning of this result, let us first assume that the cryocooler operational complex C ($\text{W} \cdot \text{K}^{-1}$) represents the heat flow conductance of an additional element in the thermal circuit represented by the cryocooler. The physical meaning of parameter C follows from the cryocooler operational principle. Inside a cryocooler there is an internal temperature $T_c^{\text{in}} < T_c$, which is reached using the gas expansion effect. This effect is proportional to the cryocooler gas volume and design S_c , gas average pressure p , cycle frequency f , temperature of the radiator T_r , and cooling efficiency Θ . Let us call the inverse of C, the cryocooler resistance $R_c = 1/C$

($\text{K} \cdot \text{W}^{-1}$). Then Case 4 represents a classical solution in electrical circuits for the two-loop circuit. Sources of the two loops for the heat current are the atmosphere and the heat source inside the chamber. In the two-loop circuit, the solution is derived using the Thévenin theorem, whereby the term $\left(R_{\text{atm-g}} \cdot R_c \right) / \left(R_{\text{atm-g}} + R_c \right)$ represents the Thévenin resistance, and the term

$(T_{atm} \cdot R_c)/(R_{atm\text{-}g} + R_c)$ is similar to the Thévenin voltage. With this notable result, let us rewrite Eq. 12 utilizing the notion of the cryocooler thermal resistance R_c for the final form of the cryospace modifier:

$$\gamma = \frac{R_{g\text{-}c} + R_c}{R_{atm\text{-}g} + R_{g\text{-}c} + R_c}. \tag{13}$$

Equations 11 and 13 are solution-neutral, which means that different types of cryosystems could be analyzed with these equations. Let us now discuss the methodology to validate the model using the real experiment.

II.3 Experimental measurements of the junction steady-state temperature

The increase of IC clock frequency leads to the growth of the junction temperature. This section describes the method that finds the IC junction temperature at each value of clock frequency. Figure 2 depicts an external view of the test setup with the CMOS PCB. The circuit consisted of three ICs (Fig. 2a) for the reliability of measurements. Each IC was a CMOS Hex inverting logic-level buffer and converter CD4049UBE. The ICs were integrated into a whole circuit, which represented a physical model for a simple computational CMOS electronics device. The latter was installed in the thermal chamber (TC) to conduct measurements for three different cooling methods (different from cases discussed in Table 2): 1) cooling by natural convection (Method 1, TC is open), 2) cooling by forced convection with the air fan (Method 2, TC is open), and cooling by forced convection with an air fan and cryocooler (Method 3, TC is closed). The cryocooler test rig is shown in Fig. 2b. The input signal generator, the output signal reader, and the power supply for the circuit were located outside TC.

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Four main parameters were controlled during the tests: the IC clock signal frequency, f_{IC} (MHz), the power supply voltage, U (V), the cryocooler shaft speed, f (rpm), and the cryocooler charge pressure, p (MPa). Only the parameter f_{IC} was changed during the test. For
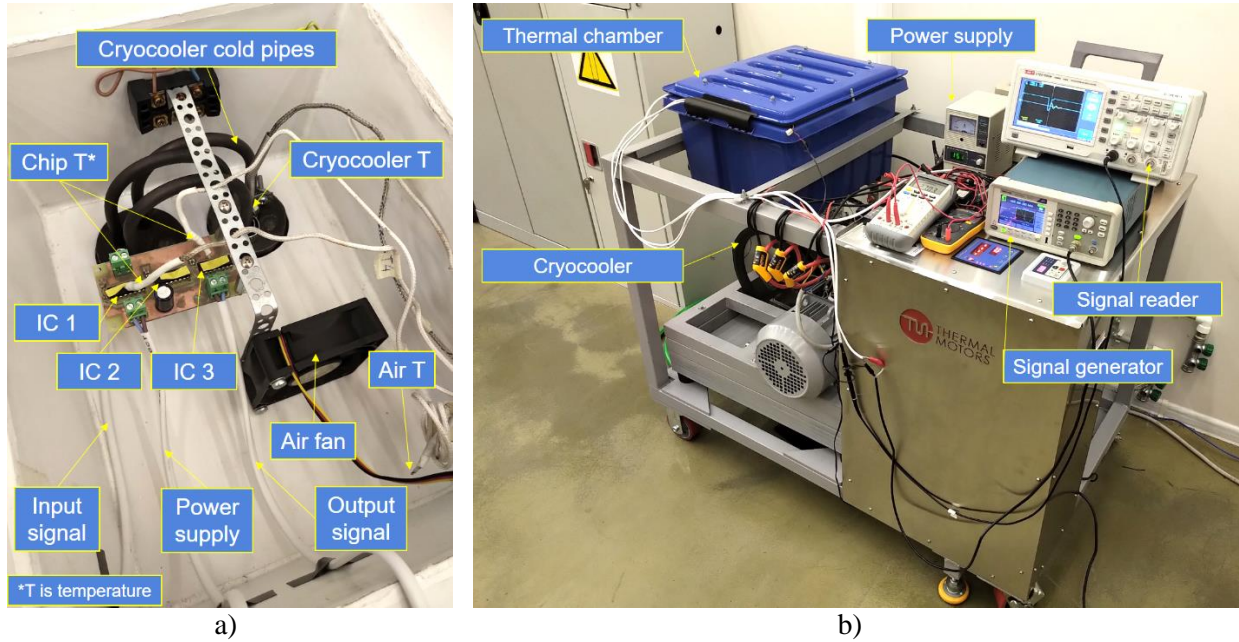

Fig. 2. The test setup: a) the internal view of the thermal chamber with the CMOS PCB, b) the external view of the thermal chamber with the cryocooler test rig.

each mode of cooling, the following values of f_{IC} were used: 1, 5, 10, 15, 20, and 25 MHz. The upper value of $f_{IC} = 25$ MHz was determined by the frequency limit of available equipment. Power supply voltage was kept at 15 V. Other controlled parameters were kept at constant values according to Table 1.

Four main parameters were measured during tests: circuit current, I (A), temperature of IC surface, T_s (°C), temperature of circulating gas (air) in the chamber, T_g (°C), temperature of cryocooler cold pipes, T_c (°C). Table 2 depicts instrument accuracies according to manufacturers.

It was convenient to use one IC for measurements. We conducted preliminary tests to understand the systematic error caused by imperfections in different manufactured ICs of the same type. For 36 observations of T_s for IC 1, 2 and 3 at different frequencies, the standard deviation of the measured temperature from the average between IC was ±2°C.

Table 3. Instrument accuracy for measured and controlled parameters.

Measured parameter	Accuracy
Circuit current, I, A	±0.4%
Temperatures, T_s, T_a, T_c, T_r °C	±0.25%
Power supply voltage, U, V	±0.5%
Shaft frequency, f, rpm	±0.05%
Charge pressure, p, MPa	±2.5%

The main measurements were conducted using one IC for convenience; however, the systematic error of ±2°C was used to evaluate the total measurement error of T_s. Average power dissipation q_s over one IC was calculated using Eq. 14:

$$q_s = \frac{I \cdot U}{3}.$$ (14)

II.4 Evaluation of model accuracy

We selected three metrics to analyze model accuracy: the coefficient of variance, mean biased error, and coefficient of determination. The formulas read:

$$CV = \frac{\sqrt{\frac{1}{n-1}\sum_{i=1}^{n}\left(x_i - \hat{x}_i\right)^2}}{\overline{x}_i} \cdot 100$$ (15)

$$MBE = \frac{1}{n-1} \cdot \frac{\sum_{i=1}^{n}\left(x_i - \hat{x}_i\right)}{\overline{x}_i} \cdot 100$$ (16)

$$R^2 = 1 - \frac{\sum_{i=1}^{n}\left(x_i - \hat{x}_i\right)^2}{\sum_{i=1}^{n}\left(x_i - \overline{x}_i\right)^2}$$ (17)

where n is the number of experiments, x_i is the measured value, $\hat{x}_i$ the predicted value, and $\bar{x}_i$ the mean measured value. In this work, x_i takes values of the junction temperature T_j . For acceptable accuracy, the values of CV and $|\text{MBE}|$ should not exceed 5% and be less than 0.95 for R^2 . Smirnov & Ouerdane (2021) discuss these formulas in more detail.

III Results

Table 3 aggregates the measurements for three cooling methods, and Fig. 3 visualizes the data graphically and depicts that with the growth of the clock frequency the junction temperature increases.

Table 3. Results of experiments with different methods of cooling

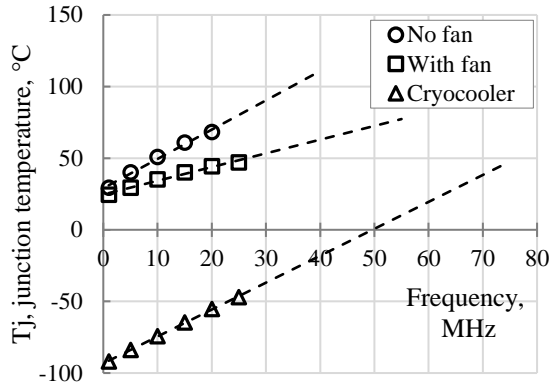| f_{IC} , MHz	I , mA	U , V	$q_s/3$, W Calculated, Eq. 11	T_s , °C	T_a , °C	T_j , °C Calculated, Eq. 8
Method 1: cooling the integrated circuit with natural convection						
1	23	15.1	0.11	28	22	32
5	62	15.1	0.31	36	22	48
10	104	15.0	0.52	45	22	64
15	143	15.0	0.72	52	22	78
20	179	15.1	0.90	57	22	90
25	No data was collected to prevent overheating of the integrated circuit					
Method 2: cooling the integrated circuit with forced convection, air fan						
1	23	15.1	0.11	23	22	27
5	62	15.0	0.31	26	22	37
10	105	15.0	0.53	29	22	48
15	145	15.0	0.73	31	22	58
20	180	15.0	0.90	33	22	67
25	204	15.0	1.03	35	22	72
Method 3: cooling the integrated circuit with forced convection, air fan and cryocooler						
1	27	15.1	0.14	-97	-101	-92
5	66	15.1	0.33	-96	-101	-84
10	107	15.1	0.54	-94	-101	-74
15	148	15.1	0.75	-92	-101	-65
20	187	15.1	0.94	-90	-101	-55
25	216	15.1	1.09	-87	-100	-47

Fig. 3. Measured junction temperature from input clock frequency for different methods of cooling
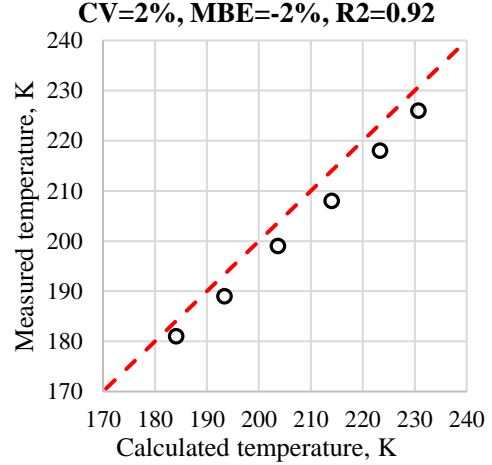

Fig. 4. Measured and calculated junction temperatures

III.1 Model accuracy

Fig. 4 depicts the comparison of predicted (Eq.11) and measured values of the junction temperature. The coefficient of variance of the model is $\pm 2\%$, the mean biased error is -2%, and the coefficient of determination is 0.92. The model predicts with good accuracy when compared with measured values. However, it is also essential to evaluate the accuracy of the measurements. Because there was only one experiment at each IC clock frequency, the estimation of a random measurement error was not possible. However, systematic errors from the instruments and IC property variations were known. The expression for indirect measurements of the junction temperature reads:

$$T_j = T_s + R_{j\text{-}s} \cdot \frac{I \cdot U}{3} \,. \tag{18}$$

From Eq. 18, Table 3, and measured error of different IC σ_{IC}, the systematic measurement error for T_j is $\sigma_{T_j} = \sqrt{\sigma_{\mathrm{IC}}^2 + \sigma_{T_s}^2 + \sigma_I^2 + \sigma_U^2}$. It follows that the total systematic error caused by the variation of IC properties, ammeter, voltmeter, and thermocouple is $\pm 2.1\%$. The error for the model-predicted value is $\pm 2\%$, which puts the prediction *within the observational error range*.

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From Fig. 4, it is evident that the model systematically predicts higher values with the mean biased error of –2%. Possible sources of this systematic error include inaccuracies in calculating resistances and the cryospace modifier in Eq. 12.

IV Discussion

It can be inferred from Fig. 3 that for the selected junction temperature $T_j = 50°C$, the computational performance of a CMOS IC operated inside the cryospace has an improvement performance potential with the factor of 3 compared with simple fan cooling. This result does not come as a surprise. Previous experimental studies, albeit limited, demonstrated similar improvements of the computational frequency with the factor that ranged between 1.5 and 2.3, depending on the study (Chu, 1999; Clark *et al.*, 1992; Carlson et *al.*, 1989). However, little was known about the exact operating conditions and design parameters of the system. This study fills this crucial gap by deriving and experimentally validating an analytical relation (Eq. 19) between the junction temperature and cryospace operational and design parameters. This formula would be helpful to analyze cryo-CMOS electronics of a wide range of designs parameters and cooling temperatures, provided that the thermal resistances are estimated accurately.

$$T_j = q_s \cdot \left(R_{j\text{-}s} + R_{s\text{-}g} + \frac{R_{g\text{-}c} + R_c}{R_{atm\text{-}g} + R_{g\text{-}c} + R_c} \cdot R_{atm\text{-}g} \right) + \frac{R_{g\text{-}c} + R_c}{R_{atm\text{-}g} + R_{g\text{-}c} + R_c} \cdot T_{atm}. \tag{19}$$

Previously (Smirnov & Ouerdane, 2021), we discussed the urgent need to better describe the cryospace operation as a function of an electricity-based cryocooler's known design and operation parameters. This conceptualization is most important as more advanced products and technologies need cryogenic temperatures for the operation. The computational performance potential demonstrated a notable improvement just by cooling the integrated circuit to a very low

temperature. With more research on computing using superconductive materials, cryocomputing could demonstrate even better performance. Therefore, the development of relation for temperatures inside the cryospace for internal heating sources is essential for analytical and design purposes. Equation 6 describes a validated analytical relation for the cryospace gas temperature and internal heat sources, and Equation 19 characterizes the core temperature of the heat source operated in the cryospace. Experiment measurements demonstrated that the coefficient of variance (±2%), mean biased error (–2%) and the coefficient of determination (0.92) of predictions are at an acceptable accuracy level. We additionally calculated the systematic observational error in the experiment (±2.1%). The prediction error of the model (±2%) is within the range of the measurement error. We implied from these results that our model makes predictions accurately enough within the uncertainty of the experimental validation. These formulas will be helpful to advance the field in the future.

The cryocooler creates an organized sink of dissipated heat to the external environment through the cryocooler. Dissipated heat produced during the computation could be pumped to a particular system for heat recovery. This approach evokes a closer look at the coupling of the cryospace with a heating source and the external environment. In this work, the amount of dissipated heat in the cryospace was negligible (Table 3). More significant amounts of heat can be dissipated using two basic approaches. The same IC can be operated at higher clock frequencies. Alternatively, more ICs can be located in the cryospace. Tradeoffs between these approaches would depend on the functionality expected from the cryocomputer and the limitations of the heat transfer from ICs.

Coupling the cryocooler to the system for heat recovery is another interesting problem. In principle, this approach can recover most of cryocooler's energy input and the pumped heat from

the cryospace (Smirnov, 2021). However, the heat recovery technology has a minimum input temperature, which is higher than a typical temperature of the cryocooler's heat sink. For example, absorption chillers for space cooling need a minimum temperature of around 350 K to operate (Amiri *et al.*, 2021), and the cryocooler in this work had the heat sink temperature of 293 K. This means that the operational and design parameters of the cryocooler would need to be changed to accommodate a hotter heat sink requirements. On the other hand, the change of boundary conditions would also affect the cryospace temperatures. Coupling effects change the entire thermal state of the system. The effect of changing boundary conditions on cooling devices was studied previously by Apertet *et al.* (2018), and future work could explore the effects of coupling using expressions 6 and 19.

IV.1 Limitations

Because of equipment limitations, we were unable to measure the temperature of the IC at clock frequencies f_{IC} exceeding 25 MHz. Although the dependence is linear in the range between 0 and 25 MHz (Fig. 3), a different relation is possible at higher frequencies.

Another limitation is that we carried out only one experiment for each IC frequency. We partially addressed this limitation by measuring temperature differences between three identical ICs for the same operational conditions. The standard deviation of temperatures was ±2%. However, more experiments would help to account for the influence of other random factors. They include different room conditions, changing temperature of the cooling water, variation of frequency in the electrical grid that powered the electromotor, changing operation of the air fan in the cryospace, or changing thermal properties of materials under cryogenic conditions. From our experience of operating the cryocooler within the range between 108 K and 200 K, these

differences would not influence the result significantly. However, the operation at cryogenic temperatures lower than that range would result in the presence of random factors, which are unique for ultra-low temperatures.

Our model calculates the heat transfer coefficient using an empirical relation of the Nusselt number for the laminar flow around the plate (Eq. 10). The IC in our experiment (Fig. 2a) can be characterized as a plate but with some reservations. Measuring the exact heat transfer surface area of the IC was problematic. As a heat source, the IC is not isolated from the circuit board, which does not produce any heat. However, some heat flows to the board through the thermal conduction because of the connection between the IC and the board and dissipates in chamber environment through the thermal convection. As a result, the effective heat transfer surface is not isothermal and has a temperature gradient, with the IC having the highest temperature. The thermocouple, which measured the surface temperature, directly contacted the IC, thus increasing the effective heat transfer area. In addition, it created local vortices that changed the heat transfer conditions near the IC. Moreover, the surface of the IC and the printed circuit board included structural elements that increased the effective surface area. It was challenging to measure these surface variations accurately. The effective surface area of the heat exchange, in this case, was larger than the wetted surface area of the IC. Therefore, we used one-third of the total printed circuit board surface area with a coefficient of 1.1 to account for additional elements on the surface of the circuit. We later validated this assumption using experimental data by calculating the product of $h_{\text{s-g}} \cdot A_{\text{s}}$ (Eq. 7), 11.87 $\text{W} \cdot \text{K}^{-1}$, and comparing it to the model calculation, 10.12 $\text{W} \cdot \text{K}^{-1}$. Future studies should pay more attention to selecting the empirical relation for the Nusselt number and estimation methods for the heat transfer coefficient from the IC.

Another assumption is the constancy of the heat transfer coefficient near the wall of the IC where the temperature T_s was measured. This assumption was introduced to develop a tractable hence physically transparent model. Thermal properties of air were used for the temperature of 173 K. However, in reality, the heat transfer coefficient changed with increased input signal frequency and temperature of the surface (Fig. 5).
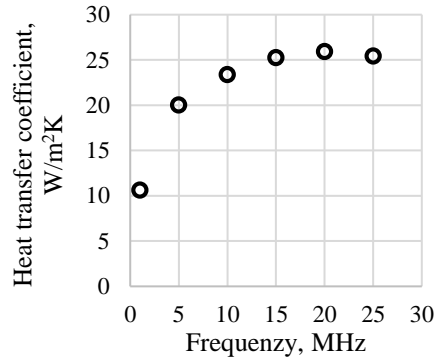

Fig. 5. Heat transfer coefficient calculated from the measurements

Equation 9 provides a great deal of explanation of how operational and design parameters of the system influence the junction temperature T_j; however, the formula says nothing about the design parameters of the IC. One would need to optimize electronics to work at cryogenic temperatures (Isaak, 2000; Chu, 1999). A dedicated study of the relation between cryogenic temperatures and architectural, structural, material and operational design decisions of the cryo-CMOS electronics would offer valuable insights and would help to design optimal cryocomputers and electronics. Some experimental and conceptual works related to cryo-CMOS electronics have been published recently (Xue *et al.*, 2021; Pauka *et al.*, 2021). Nevertheless, they primarily focused on the electronics design but not on the coupled design and operation of electronics and cryospace.

The energy to run a cryocooler is several times larger than the energy consumption of advanced computer processors. For example, the cryocooler power consumption in this study to

cool a space with a shoebox-size to 173 K was 850 W. At the same time, the heat dissipation of a commercial computer processors is around 200 W. In other words, to increase the computational performance with the factor of 3—assuming that the processor is optimized for low temperatures—one needs to use an extra 850 W of energy just to cool a processor to cryogenic temperatures. However, when the frequency would be actually increased, the power dissipation would also increase, effectively heating the cooling gas in the cryospace. In order to pump more heat out of the cryospace and keep the temperature of the gas at a set constant level, the cryocooler would need additional energy from the grid. Extra energy cost might not be justified because the efforts to reduce watts needed per million instructions per second using conventional approaches were successful in the past (Roser and Ritchie, 2013) and finding novel approaches (such as cryocooling) might not be urgent. And yet, jamming more transistors on the circuit becomes an increasingly challenging task, and the increase of computational performance through this approach might not have substantial grounds any longer. Perhaps, another way to put the question of extra energy cost is to ask, how to make computers faster and waste less energy? We discussed above that a joint operation of the cryocomputers with a heat recovery system for space cooling or other applications might be an exciting avenue for future research. In addition to future trends and the possibility for heat recovery that might justify extra energy cost to run a cryocooler, there are several advantages of cryo-CMOS device discussed in the introductory section. Could the increased energy cost be offset by the benefits of a substantial decrease of the electrical resistivity, increased DRAM storage time by several orders of magnitude, and improved device and circuit reliability (Clark *et al.*, 1992)? Could these properties be more beneficial in designing computers for specific applications, for example artificial intelligence of crypto-mining? How could the application of superconductor materials enhance cryocomputing? The answers to these questions

would help to better understand whether it is necessary to pay extra energy cost for the cryogenic cooling of CMOS electronics.

Another side of the problem is the performance of the cryocooler itself. At present, the knowledge of how to build efficient high-capacity cryocoolers is inadequate. The efficiency of a cryogen-free cryocoolers operated at 4 K is around 10% of the ideal Carnot cryocooler (Strobridge, 1974) and has not improved significantly over the last 50 years (Martin *et al.*, 2021). Many questions related to design, material choice and reliability of these complex thermal machines are still not answered. Furthermore, there is always the question of the coupled operation of the cryocooler and cryoprocessor. Taken together, the answers to these questions would help to reduce the energy cost and might offset it with other benefits.

An important implication of this work is the knowledge to operate cryo-CMOS electronics for quantum computing. Recent work in this area focused on the design and operation of cryoelectronics. However, much is to be learned about modifying the parameters of the cryospace for these types of devices. The operational temperatures currently discussed in the literature are at the level of several kelvins. The present work discusses the operation of electronics in the cryospace with a temperature of 173 K. This is a significant difference and a limitation to generalizing the results to lower temperature ranges. Although the empirical base is limited, the analytical model, at least in theory, is independent of the cryocooler choice and the temperature range (Eq. 19) because it is derived using the thermal-electrical analogy. This relation could be utilized to model cryospaces with different cryocooling technologies described by thermal resistances R_c, R_{atm-g}, R_{g-c}, and R_{s-g}, provided that the latter take into account the change of material properties at the temperature level of several kelvins.

IV.2 Future work

Two interesting research directions could be pursued based on the results of this work:

1) Analytical and experimental analysis of a coupled cryo-CMOS electronics and regenerative cryocooler operated at the temperature of low-temperature heat recovery applications.
2) Optimization of design and operational parameters of the cryo-CMOS electronics and cryospaces for their joined operation.

V Conclusions

This work aimed to derive an effective analytical relationship between the junction temperature of the Si-based semiconductor integrated circuit and the known and controllable parameters of the cryospace. We developed a model to predict the steady-state junction temperature of the integrated circuit operated in the cryospace using the thermal-electrical analogy. Our experimental validation demonstrated that the prediction accuracy of the model is ±2%. Our results showed the increase of possible clock frequencies through cryogenic cooling of a simple CMOS integrated circuit by the factor of 3. Our findings can be applied to analyze the coupling of cryo-CMOS electronics and cryocoolers over a wide range of cryogenic temperatures for the design and control of cryo-CMOS devices.

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Appendix

Calculation of limits in Table 2.

Case 1) $R_{\text{atm-g}} \to \infty$, $R_{\text{atm-g}} = x$, $R_{\text{g-c}} = b : \lim\limits_{x\to\infty} \gamma = 0$

$$\gamma = \frac{b}{b+x-\dfrac{x}{b\cdot C+1}} = \frac{b}{\dfrac{b(b\cdot C+1)+xb\cdot C+x-x}{b\cdot C+1}} = \frac{b\cdot C+1}{x\cdot C+b\cdot C+1} \Rightarrow \lim\limits_{x\to\infty}\gamma = 0$$

$$R_{\text{atm-g}}\gamma = \frac{x(b\cdot C+1)}{x\cdot C+b\cdot C+1} = \frac{b\cdot C+1}{\dfrac{b\cdot C}{x}+\dfrac{1}{x}+C} \Rightarrow \lim\limits_{R_{\text{atm-g}}\to\infty} R_{\text{atm-g}}\gamma = b+\frac{1}{C}.$$

Case 3) $R_{\text{g-c}} \to \infty$, $R_{\text{g-c}} = x$, $R_{\text{atm-g}} = a : \lim\limits_{x\to\infty}\gamma = 1$

$$\gamma = \frac{x}{a+x-\dfrac{a}{x\cdot C+1}} = \frac{x}{\dfrac{x\cdot a\cdot C+a+x(x\cdot C+1)-a}{x\cdot C+1}} = \frac{x\cdot C+1}{a\cdot C+(x\cdot C+1)} = \frac{1}{\dfrac{a\cdot C}{x\cdot C+1}+1} \Rightarrow \lim\limits_{x\to\infty}\gamma = 1.$$

Case 4) $R_{\text{g-c}} \to 0$, $R_{\text{g-c}} = x$, $R_{\text{atm-g}} = a : \lim\limits_{x\to 0}\gamma = \dfrac{1}{a\cdot C+1}$

$$\gamma = \left[\text{from }(3)\right] = \frac{1}{\dfrac{a\cdot C}{x\cdot C+1}+1} \Rightarrow \lim\limits_{x\to 0}\gamma = \frac{1}{a\cdot C+1}$$

$$T_{\text{j}} = q_{\text{s}}\left(R_{\text{j-s}}+R_{\text{s-g}}+\gamma\cdot R_{\text{atm-g}}\right)+\gamma\cdot T_{\text{atm}} = q_{\text{s}}\left(R_{\text{j-s}}+R_{\text{s-g}}+\frac{R_{\text{atm-g}}}{R_{\text{atm-g}}\cdot C+1}\right)+\gamma\cdot T_{\text{atm}} =$$

$$= q_{\text{s}}\left(R_{\text{j-s}}+R_{\text{s-g}}+\frac{1}{C+\dfrac{1}{R_{\text{atm-g}}}}\right)+\frac{T_{\text{atm}}}{R_{\text{atm-g}}\cdot C+1} = q_{\text{s}}\left(R_{\text{j-s}}+R_{\text{s-g}}+\frac{R_{\text{c}}\cdot R_{\text{atm-g}}}{R_{\text{c}}+R_{\text{atm-g}}}\right)+\frac{R_{\text{c}}\cdot T_{\text{atm}}}{R_{\text{c}}+R_{\text{atm-g}}}.$$