

Fast and Fault-Tolerant Model Predictive Control of MMCs Under Selective Harmonic Elimination

Ardavan Mohammadhassani, *Graduate Student Member, IEEE*, and Ali Mehrizi-Sani, *Senior Member, IEEE*

Abstract—Modular multilevel converters (MMC) are an attractive choice for various applications, including medium- and high-voltage drives. The large number of semiconductor-based submodules (SM) in an MMC makes it vulnerable to SM switch failures. This paper proposes a fault-tolerant (FT) selective harmonic elimination method to enable seamless operation of an MMC during such failures. The effects of switch failure on phase voltage waveforms are studied first. Then, a method is proposed to design the FT SHE-PWM waveform to preserve its harmonic performance. A model predictive controller (MPC) is also proposed to increase the capacitor voltages during an SM failure to maintain the fundamental component of the faulty phase voltage and balance the line voltages. The advantages of the proposed method are verified through offline and real-time simulation studies on a three-phase nine-level MMC in PSCAD/EMTDC software and RTDS.

Index Terms—Fault-tolerant control, model predictive control, multilevel converters, pulse width modulation, selective harmonic elimination, submodule failure.

I. INTRODUCTION

Modular multilevel converters (MMC) have become a suitable choice for applications such as HVDC, FACTS, and medium- and high-voltage drives [1]. Advantages of MMCs include voltage scalability, total modularity, and use of a single DC-link. An MMC consists of hundreds of identical semiconductor submodules (SM) connected in series in each phase. SMs consist of insulated-gate bipolar transistors (IGBT). IGBTs are highly fragile, and since an MMC has many IGBTs, they are the most likely elements to fail [2]. There are two types of IGBT failures: short-circuit and open-circuit. The existing gate-drive circuits provide protection for short-circuit failures. However, open-circuit failures can remain undetected for a long time and cause overvoltage and overcurrent problems. Once detected, the SMs with faulty IGBTs are bypassed using a fast bidirectional switch [3]. This causes the voltage of the faulty phase to reduce and the line voltages to become unbalanced, degrading the power quality of the converter [4]. Reliability is a key factor in MMC applications as mentioned above, and the control system of the MMC should enable its seamless operation during SM failures.

Various methods are introduced in the literature to enable fault-tolerant (FT) operation of MMCs [4]–[12]. These meth-

ods can be categorized into two groups: hardware-based methods and software-based methods. Hardware-based methods incorporate redundant SMs in each phase, inserted in place of bypassed faulty SMs. However, most of these methods utilize redundant SMs with uncharged capacitors (cold SMs) [9]. Inserting cold SMs into the circuit causes transients and distortions in the output voltage. In addition, cold SMs reduce the semiconductor utilization factor of an MMC. Some redundancy-based methods use pre-charged (hot) SMs [10], [11]. Hot SMs are inserted into circuit even during the normal operation of MMCs. However, this results in increased switching and conduction losses. On the other hand, transient response of the output voltage is better and semiconductor utilization factor is higher. Despite their advantages, both redundancy-based methods have two drawbacks in common [12]: First, utilizing redundant SMs increases the cost and size of the converter. Second, FT operation of MMCs is achieved only when the number of redundant SMs is higher than the number of faulty SMs.

In contrast, software-based methods modify the modulation technique of an MMC to add FT capabilities to its operation. These methods are less common. References [6], [7] study modifying modulation techniques for FT operation of multicell converters. However, they do not maintain the harmonic performance. The merits of modifying space vector modulation (SVM) for FT operation of MMCs are explored in [8]. However, SVM design becomes very complicated when the number of voltage levels increases beyond three. In addition, this method does not use any circulating current controllers during FT mode, which adversely affects the harmonic performance of SVM. Reference [4] modifies the phase-shifted carrier modulation technique (PSC) to enable FT operation in MMCs. However, this method still uses redundant SMs.

A widely known modulation scheme is the selective harmonic elimination pulse-width modulation (SHE-PWM). In SHE-PWM, the switching angles are explicitly calculated to achieve the desired harmonic performance. This technique is commonly used in cascaded H-bridge inverters (CHB) [13], [14]; however, it is not widely employed in MMCs yet. This is because MMCs are commonly used in high-voltage applications, where the number of voltage levels is very high. For instance, an MMC requires 200–400 SMs per arm to reach ± 400 kV (DC) in an HVDC system [15]. Therefore, the number of switching angles is also very high. This significantly complicates SHE-PWM; thus, other modulation techniques such as the nearest level modulation (NLM) are used for such applications. Simultaneously, MMCs are beginning to gain favor in applications such as medium-voltage microgrids [16], [17], where the number of SMs is 5–20 per arm. Thus, the

This work was supported in part by the National Science Foundation (NSF) under awards ECCS-1953198 and EECs-1953213, in part by Manitoba Hydro International, and in part by the Commonwealth Cyber Initiative (CCI), an investment by the Commonwealth of Virginia in the advancement of cyber R&D, innovation, and workforce development.

A. Mohammadhassani and A. Mehrizi-Sani are with the Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg VA 24061 USA (e-mails: arda-vanmh93@vt.edu, mehrizi@vt.edu).

advantages of SHE-PWM can be explored for MMCs in these applications [18], and FT SHE-PWM methods can be designed to increase the reliability of MMC operation [19]. On the other hand, the unequal and sometimes large difference between the switching angles in SHE-PWM can cause large ripples in the circulating current in previously proposed circulating current controllers [20]–[22]. This may cause the circulating current controller to become unstable or create large disturbances in the output voltage. A method is proposed in [18] to limit the circulating current ripple by applying redundant switching states and using two upper and lower limits. However, this method has a slow response. Moreover, choosing the limits is an empirical process, which can become difficult under different MMC ratings. Therefore, a circulating current controller should also be designed to address the aforementioned challenges.

This paper introduces an FT SHE-MPC strategy for MMCs. A procedure is proposed to properly design the FT SHE-PWM waveforms to preserve the harmonic performance of the faulty phase voltage and its fundamental component. This procedure is designed by building upon the $(2N + 1)$ -level SHE-PWM proposed in [18]. An MPC-based controller is proposed to stabilize the operation of the MMC while implementing SHE-PWM during normal and FT operation. MPC is an effective strategy for multi-objective and nonlinear models [23], [24]. The proposed controller increases the capacitor voltages during FT operation to complete the transition into FT operation and maintain the fundamental component of the faulty phase voltage. To verify the performance of the proposed FT SHE-PWM scheme, a detailed model of an MMC with 4 SMs in each arm is modeled in PSCAD/EMTDC software. In addition, real-time results are acquired using RTDS to confirm the results obtained using PSCAD/EMTDC.

The specific contributions of this paper are

- FT SHE-PWM waveform design procedure.
- FT SHE-PWM mathematical derivation.
- Design of MPC-based circulating current controller for normal and FT operation.

The rest of this paper is organized as follows. Section II discusses the mathematical modeling of the MMC. Section III discusses the proposed waveform design procedure for FT SHE-PWM. Section IV presents the proposed MPC strategy. Section V discusses performance evaluation. Section VI discusses the real-time evaluation of the proposed method. Finally, conclusions are presented in Section VII.

II. BASICS OF OPERATION

Fig. 1 shows the generic topology of a three-phase three-wire MMC with N SMs in each phase arm. Half-bridge SMs (HBSM) are considered in this paper as they are the most common choice [1]. Each HBSM is also equipped with a bidirectional switch to bypass it during OC SM faults. The circulating current $i_{diff,i}$ and the output current $i_{o,i}$ of phase i

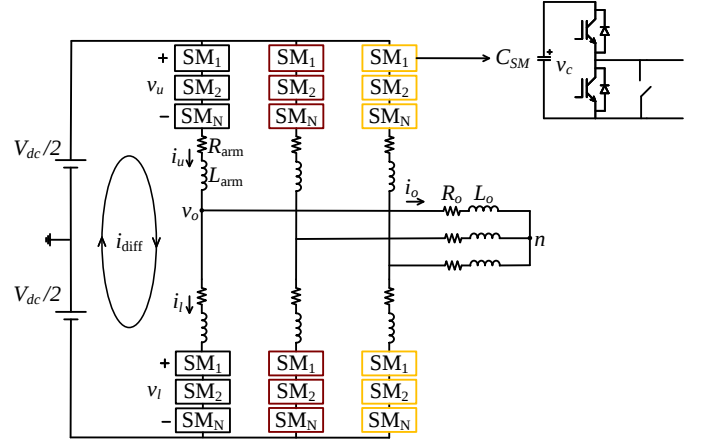


Fig. 1. Generic topology of a three-phase MMC.

are found as

$$\begin{aligned} i_{diff,i} &= \frac{i_{u,i} + i_{l,i}}{2} \\ i_{o,i} &= i_{u,i} - i_{l,i} \\ i &= a, b, c, \end{aligned} \quad (1)$$

where $i_{u,i}$ and $i_{l,i}$ are the upper and lower arm currents, as shown in Fig. 1. The arm voltages are

$$\begin{aligned} v_{u,i} &= \sum_{j=1}^N n_{u,j}^i v_{cu,j}^i \\ v_{l,i} &= \sum_{j=1}^N n_{l,j}^i v_{cl,j}^i \\ n_{u,j}^i, n_{l,j}^i &\in \{0, 1\} \\ i &= a, b, c, \end{aligned} \quad (2)$$

where $v_{u,i}$ and $v_{l,i}$ are the upper and lower arm output voltages, $n_{u,j}^i$ and $n_{l,j}^i$ are the upper arm and lower arm capacitor insertion indices, and $v_{cu,j}^i$ and $v_{cl,j}^i$ are the upper and lower arm capacitor voltages. The balanced steady-state value of the capacitor voltages V_c is

$$V_c = \frac{V_{cu,i}^\Sigma}{N} = \frac{V_{cl,i}^\Sigma}{N}, \quad (3)$$

where $V_{cu,i}^\Sigma$ and $V_{cl,i}^\Sigma$ are the sum of HBSM capacitor voltages in the upper and lower arms, respectively. Therefore, (2) is rewritten as

$$\begin{aligned} v_{u,i} &= \frac{V_{cu,i}^\Sigma}{N} \sum_{j=1}^N n_{u,j}^i = N_{u,i} V_{cu,i}^\Sigma \\ v_{l,i} &= \frac{V_{cl,i}^\Sigma}{N} \sum_{j=1}^N n_{l,j}^i = N_{l,i} V_{cl,i}^\Sigma \\ N_{u,i}, N_{l,i} &\in \left\{ 0, \frac{1}{N}, \frac{2}{N}, \dots, 1 \right\} \\ i &= a, b, c, \end{aligned} \quad (4)$$

where $N_{u,i}$ and $N_{l,i}$ are the upper and lower arm insertion indices. The line-to-neutral voltage $V_{o,i}$ is defined as

$$V_{o,i} = \frac{v_{l,i} - v_{u,i}}{2} - \frac{R_{arm}}{2} i_{o,i} - \frac{L_{arm}}{2} \frac{di_{o,i}}{dt}. \quad (5)$$

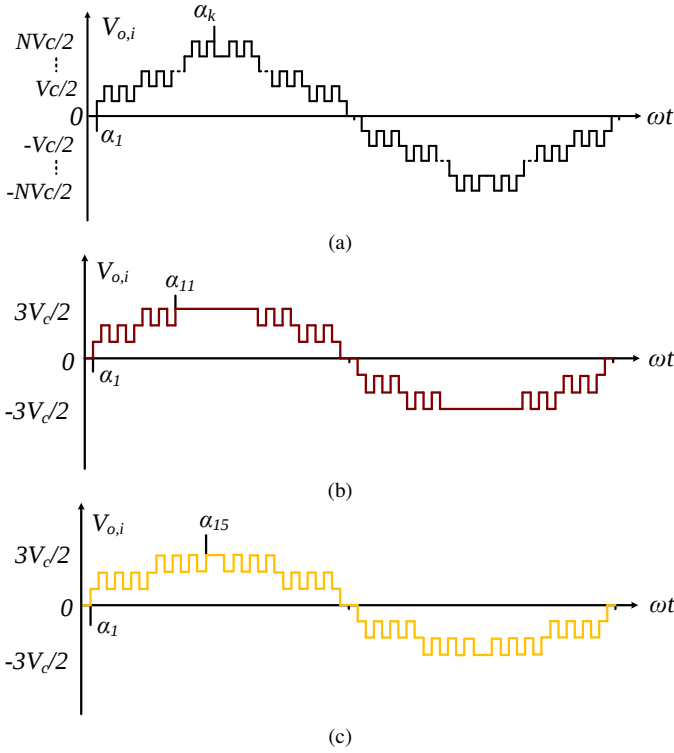


Fig. 2. $V_{o,i}$ waveform during (a) normal operation, (b) an HBSM failure, and (c) FT operation when $M = 1$.

The complete dynamic model of the MMC is found as

$$\begin{cases} \frac{di_{\text{diff},i}}{dt} = \frac{1}{2L_{\text{arm}}} V_{\text{diff},i} - \frac{R_{\text{arm}}}{L_{\text{arm}}} i_{\text{diff},i} \\ \frac{dV_{cu,i}^{\Sigma}}{dt} = \frac{NN_{u,i}}{C_{\text{SM}}} i_{u,i} \\ \frac{dV_{cl,i}^{\Sigma}}{dt} = \frac{NN_{l,i}}{C_{\text{SM}}} i_{l,i}, \end{cases} \quad (6)$$

where L_{arm} is the arm inductance, R_{arm} is the arm resistance, and C_{SM} is the HBSM capacitance.

III. PROPOSED WAVEFORM DESIGN PROCEDURE FOR FAULT-TOLERANT $(2N + 1)$ -LEVEL SHE-PWM

A. Overview of the $(2N + 1)$ -Level SHE-PWM

Fig. 2(a) shows the general $(2N + 1)$ -level phase output voltage waveform $V_{o,i}$ of an MMC with SHE-PWM. The waveform has quarter-wave symmetry. There are k switching angles in one quarter wave, which corresponds to k degrees of freedom. Due to quarter-wave symmetry, the Fourier series expansion of $V_{o,i}$ has only odd sine coefficients:

$$\begin{aligned} V_{o,i}(\omega_o t) &= \sum_{n=1,3,5,7,\dots}^{\infty} b_n \sin(n\omega_o t) \\ b_n &= \frac{2V_c}{n\pi} \sum_{i=1}^k m_i \cos(n\alpha_i) \\ m_i &= \begin{cases} 1, & \text{Rising step} \\ -1, & \text{Falling step} \end{cases} \\ 0 &< \alpha_1 < \alpha_2 < \dots < \alpha_{k-1} < \alpha_k < \frac{\pi}{2}, \end{aligned} \quad (7)$$

where ω_o is the fundamental frequency.

The general $(2N + 1)$ -level SHE-PWM problem is defined

in (8), which is solved offline to obtain switching angles for normal operation. This formulation can be solved using different methods, e.g., using Groebner bases and symmetrical polynomials [25] and virtual angles [18], which are verified on commercially available software packages such as Maple18, Mathematica, and MATLAB. The first equation corresponds to the fundamental component, and the remaining $k - 1$ equations correspond to the low-order harmonics to be eliminated. Since a three-phase system is studied, triplen harmonics are canceled in line voltages and are not considered in this formulation.

$$\begin{cases} \frac{2V_{dc}}{\pi N} \sum_{i=1}^k m_i \cos(\alpha_i) = \frac{m_a V_{dc}}{2} \\ \frac{2V_{dc}}{5\pi N} \sum_{i=1}^k m_i \cos(5\alpha_i) = 0 \\ \frac{2V_{dc}}{7\pi N} \sum_{i=1}^k m_i \cos(7\alpha_i) = 0 \\ \vdots \\ \frac{2V_{dc}}{l\pi N} \sum_{i=1}^k m_i \cos(l\alpha_i) = 0, \end{cases} \quad (8)$$

where $0 \leq m_a \leq 1$, and l is the highest harmonic to be eliminated.

B. Proposed FT SHE-PWM

To design the FT SHE-PWM method, the effect of bypassed HBSMs on $V_{o,i}$ is studied first. When one HBSM is bypassed in the upper and lower arms of one phase, the number of voltage levels in $V_{o,i}$ reduces to $2(N - 1) + 1 = 2N - 1$. When $M < N$ HBSMs are bypassed in the upper and lower arms of one phase, the number of voltage levels in $V_{o,i}$ reduces to $2(N - M) + 1$. This means that the maximum voltage available for the faulty phase reduces, which in turn makes the line voltages unbalanced and reduces the transferred power. Moreover, the harmonic performance of $V_{o,i}$ and power quality of the MMC deteriorate.

To address this issue, the number of switching angles in the corrupted $V_{o,i}$ waveform is increased so that the same number of harmonic components are eliminated as in the prefailure case and its fundamental component is preserved. The waveforms need to be designed for each value of M . Hence, the more waveforms designed, the more fault-tolerant the converter becomes. However, this also increases the complexity of the controller and requires a larger memory.

As an example, consider the FT SHE-PWM waveform design procedure for a nine-level MMC with $N = 4$ and $M = 1$. The $V_{o,i}$ waveform for normal operation of this MMC has 15 switching angles in each quarter-wave. Therefore, 14 low-order harmonics can be eliminated while the fundamental component is controlled at its setpoint. When $M = 1$, the faulty HBSM and another HBSM in the opposite arm are bypassed. Hence, the faulty phase can no longer generate $\pm 2V_c$ voltage levels (highest levels). As shown in Fig. 2(b), the number of switching angles in one quarter-wave is reduced to 11, which degrades its harmonic performance. To design the FT $V_{o,i}$ waveform as discussed, additional switching angles

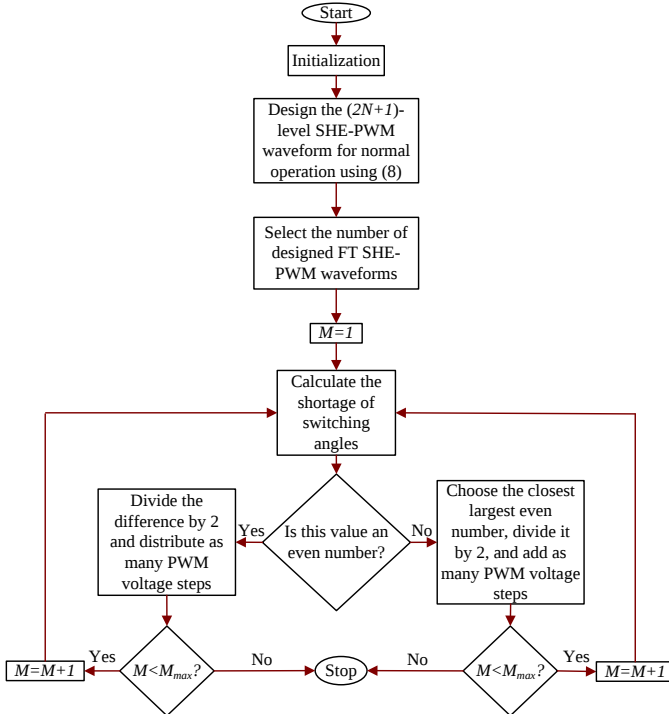


Fig. 3. Proposed process for designing the FT SHE-PWM waveforms.

are required to be added to the waveform. These switching angles can be arbitrarily placed in the waveform shown in Fig. 2(b) as long as its quarter-wave symmetry is maintained. The difference between the number of switching angles in the waveform shown in Figs. 2(b) and (c) is 4. Thus, by adding two extra voltage steps, the number of switching angles can return to 15, ensuring that the harmonic performance of $V_{o,i}$ is preserved. The switching angles for constructing the FT SHE-PWM waveforms and preserving the fundamental component of $V_{o,i}$ are found by solving (8) with N changed to $N - M = N - 1$ for the faulty phase.

Fig. 3 summarizes the proposed design procedure for FT waveforms:

- 1) Design the $(2N + 1)$ -level SHE-PWM waveforms according to Fig. 2(a).
- 2) Choose the maximum design value for M .
- 3) If the shortage of switching angles is an even number, add half as many voltage steps to the faulted waveform. Otherwise, find the closest largest even number and add half as many voltage steps to the faulted waveform.
- 4) Continue designing waveforms until the final value of M is reached.

IV. PROPOSED MPC-BASED STRATEGY FOR CIRCULATING CURRENT CONTROL

Implementing SHE-PWM requires stable control of $i_{diff,i}$, $V_{cu,i}^\Sigma$, and $V_{cl,i}^\Sigma$ while generating the correct SHE-PWM waveform. This paper proposes an MPC-based $i_{diff,i}$ controller to stabilize the MMC during normal and FT operation and prevent distortion in the output voltage. The proposed controller receives the designed SHE-PWM waveforms, chooses the optimum $N_{u,i}$ and $N_{l,i}$, and balances $V_{cu,i}^\Sigma$ and $V_{cl,i}^\Sigma$ to control the output voltages. The proposed controller also increases V_c

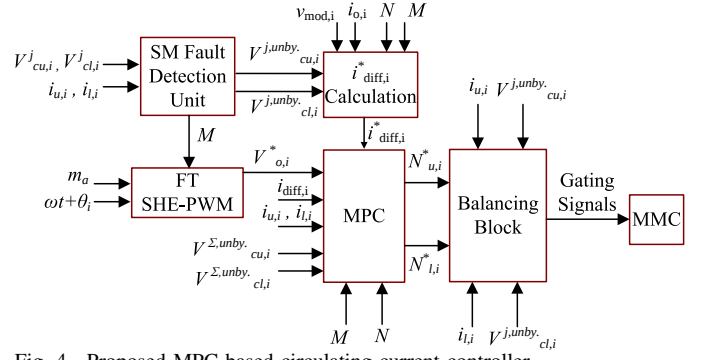


Fig. 4. Proposed MPC-based circulating current controller.

during FT operation to preserve the fundamental component of the faulty output voltage and balance the line voltages.

Fig. 4 shows the proposed controller. If $M = 0$, the controller operates in the normal mode. Otherwise, FT operation is activated. The proposed controller receives the reference SHE-PWM waveform $V_{o,i}^*$ and the sampled values of $i_{diff,i}$, $V_{cu,i}^\Sigma$, and $V_{cl,i}^\Sigma$ to predict their next sampled values using forward Euler's method. This is done through a discrete form of (6) with a sampling period of T_s

$$\begin{cases} i_{diff,i}((n+1)T_s) = a_1 V_{diff,i}(nT_s) + a_2 i_{diff,i}(nT_s) \\ V_{cu,i}^\Sigma((n+1)T_s) = a_3 i_{u,i}(nT_s) + V_{cu,i}^\Sigma(nT_s) \\ V_{cl,i}^\Sigma((n+1)T_s) = a_4 i_{l,i}(nT_s) + V_{cl,i}^\Sigma(nT_s), \end{cases} \quad (9)$$

where

$$\begin{cases} a_1 = \frac{T_s}{2L_{arm}}, & a_2 = 1 - \frac{T_s R_{arm}}{L_{arm}} \\ a_3 = \frac{T_s(N-M)N_{u,i}}{C_{SM}} \\ a_4 = \frac{T_s(N-M)N_{l,i}}{C_{SM}}. \end{cases} \quad (10)$$

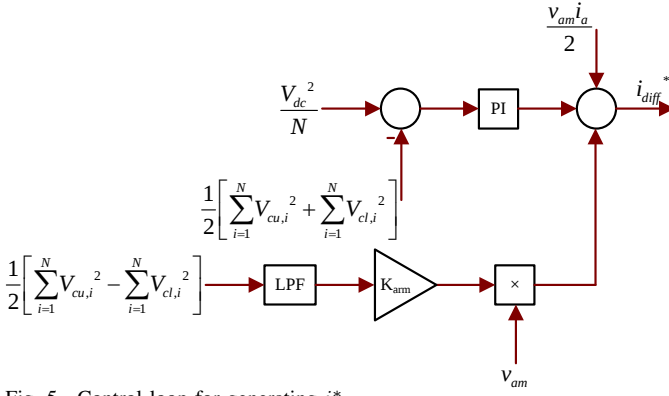
$N_{u,i}$ and $N_{l,i}$ are defined as

$$N_{u,i}, N_{l,i} \in \{0, \frac{1}{N-M}, \frac{2}{N-M}, \dots, 1\}. \quad (11)$$

Equation (11) defines a limited set. The optimum $N_{u,i}$ and $N_{l,i}$ that minimize the cost function defined in (12) are chosen and fed to the balancing block. This block determines which HBSMs to insert or bypass according to their V_c values and arm current directions. Using the method proposed in [18], the switching frequency of the proposed method is set to that by the SHE-PWM block. However, MPC controls $i_{diff,i}$ by determining $N_{u,i}$ and $N_{l,i}$. Therefore, it adds extra switchings to properly control the MMC.

$$\text{Cost} = \sigma \|X((n+1)T_s) - X^*((n+1)T_s)\|_2^2, \quad (12)$$

where σ is vector containing the weight factors, X is the state vector, X^* is the reference state vector, and $\|\cdot\|_2$ is the Euclidean norm. The weighting factors are determined using the per-unit conversion method in [26] to set $i_{diff,i}$ as the main control objective while setting the relative importance of $V_{cu,i}^\Sigma$ and $V_{cl,i}^\Sigma$. In contrast to the SHE-MPC strategy in [22], the proposed MPC method does not treat the SHE-PWM waveform as an input to the MPC cost function. Instead, it predicts the state variables for each voltage level in the reference SHE-PWM waveform and chooses the optimum $N_{u,i}$ and $N_{l,i}$ to tighten control on the output voltage and ensure fast and stable control of circulating currents. To maintain energy balance between

Fig. 5. Control loop for generating i_{diff}^* .TABLE I
SIMULATION PARAMETERS

Parameter	Value
Number of HBSMs in each phase arm N	4
DC-link voltage V_{dc}	10.87 kV
HBSM capacitance C_{SM}	1200 μ F
Arm inductance L_{arm}	9 mH
Load resistance R_o	12 Ω
Load inductance L_o	4 mH
Fundamental frequency f_o	60 Hz
Modulation index m_a	0.8
MPC control frequency f_s	50 kHz
Rated V_c for normal operation	2.72 kV
Rated V_c for FT operation	3.62 kV

the DC and AC sides and balance the energy through phase arms, the method proposed in [27], also shown in Fig. 5, is used to generate i_{diff}^* based on the instantaneous information of the MMC, including the instantaneous values of sum of capacitor voltages and the output current.

If an HBSM fails, the proposed controller increases the V_c values by the amount defined in (13) to complete the transition to FT operation. To maintain $V_{cu,i}^\Sigma$ and $V_{cl,i}^\Sigma$ at V_{dc} after M HBSM failures, V_c should be increased to $V_{dc}/(N - M)$ requiring larger capacitors. However, as N increases, the increase in capacitor voltages ΔV_c during HBSM failures decreases:

$$\Delta V_c = \frac{M V_{dc}}{N(N - M)}. \quad (13)$$

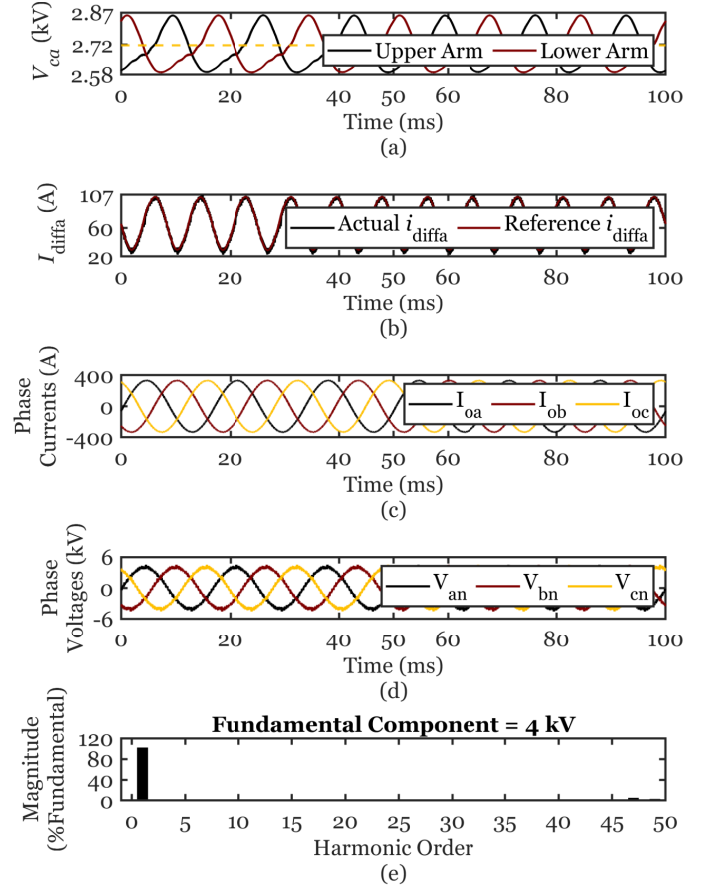
Even though this method requires overdesign, it is less costly than conventional redundancy-based methods, which add extra HBSMs [8].

V. NON-REAL-TIME EVALUATION

A detailed-model of a three-phase nine-level MMC with $N = 4$ is created in PSCAD/EMTDC software for non-real-time simulation. Table I summarizes the simulation parameters. The capacitance is calculated using the method in [28] to achieve a 5% voltage ripple. The switching angles are calculated using exchange market algorithm [13] to eliminate harmonics 5 to 43.

A. Steady-State Performance

This section evaluates the steady-state performance of the proposed method during normal operation. Fig. 6(a) shows the capacitor voltages of phase a . The proposed method success-

Fig. 6. Steady-state simulation results for (a) $v_{cu,j}^a$ and $v_{cl,j}^a$, (b) $i_{diff,a}$, (c) $i_{o,i}$, (d) $V_{o,i}$, and (e) harmonic spectrum of $V_{o,i}$.

fully controls the capacitor voltages at 2.72 kV with a ripple of 4.89%. Fig. 6(b) shows $i_{diff,a}$; it correctly follows its reference with a maximum of 106.1 A. Fig. 6(c) shows the output currents. The proposed method generates balanced three-phase output currents with a peak magnitude of 335.3 A. Fig. 6(d) shows the output voltages. The proposed method generates balanced three-phase output voltages with a peak magnitude of 4 kV. Fig. 6(e) shows the harmonic spectrum of the output voltages: the peak value of the fundamental component is 4 kV, and the low-order harmonics are eliminated.

B. Response to Change in m_a

This section evaluates the response of the proposed method to a step change in m_a during normal operation. Fig. 7(a) shows the capacitor voltages of phase a . At $t = 50$ ms, m_a increases in a step from 0.8 to 1. After a small transient with an overshoot to 2.87 kV, the capacitor voltages stabilize at 2.72 kV with a ripple of 5.03%. The settling time of capacitor voltages is 50 ms, which is almost half of that for the method proposed in [18]. Fig. 7(b) shows $i_{diff,a}$. At $t = 50$ ms, m_a increases in a step from 0.8 to 1. $i_{diff,a}$ successfully follows its new reference, increasing its maximum to 156.3 A. The settling time for the circulating current is 20 ms, which is almost one-fifth of that for the method proposed in [18]. Fig. 7(c) shows the output currents. The proposed method successfully generates balanced three-phase output currents and increases their peak magnitude to 413.8 A.

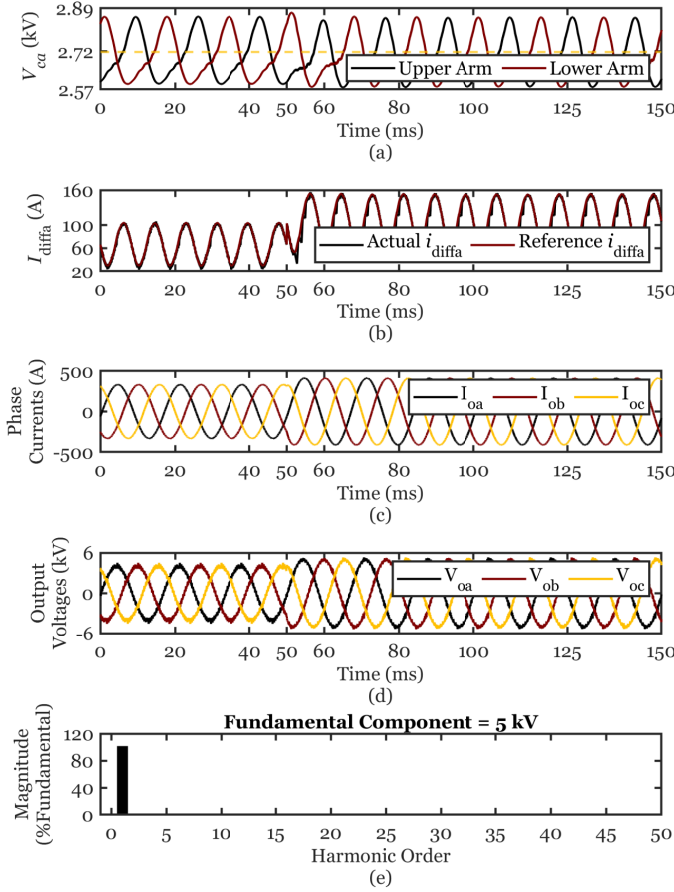


Fig. 7. Simulation results for step change in m_a : (a) $v_{cu,j}^a$ and $v_{cl,j}^a$, (b) $i_{diff,a}$, (c) $i_{o,i}$, (d) $V_{o,i}$, and (e) harmonic spectrum of $V_{o,i}$ with $m_a = 1$.

Fig. 7(d) shows the output voltages. The proposed method successfully generates balanced three-phase output voltages and increases their peak magnitude to 5 kV. Fig. 7(e) shows the harmonic spectrum of the output voltages. The peak value of the fundamental component is increased to 5 kV while eliminating the low-order harmonics.

C. Response to HBSM Failures

This case study evaluates the performance of the proposed method under HBSM failures. Fig. 8(a) shows the capacitor voltages of phase a . At $t = 50$ ms, SM_{u1a} and SM_{l1a} are bypassed and FT operation is established. The proposed method stabilizes the remaining capacitor voltages at 3.62 kV with a ripple of 3.85% at $t = 126.43$ ms. Fig. 8(b) shows $i_{diff,a}$; it stabilizes with a maximum of 99.8 A at $t = 126.43$ ms and an overshoot to 248.6 A. The settling time of capacitor voltages and circulating current is 76.43 ms, which is significantly faster than the method proposed in [5] which takes 428.8 ms to establish FT operation. Fig. 8(c) shows the output currents. The proposed method generates balanced three-phase output currents and keeps their peak magnitude constant. However, the output currents become slightly more distorted. Fig. 8(d) shows the output voltages. The proposed method generates balanced three-phase output voltages with a modified waveform for $V_{o,a}$. Fig. 8(e) shows the harmonic spectrum of $V_{o,a}$ during FT operation; the low-order harmonics are still eliminated and the peak value of the fundamental component

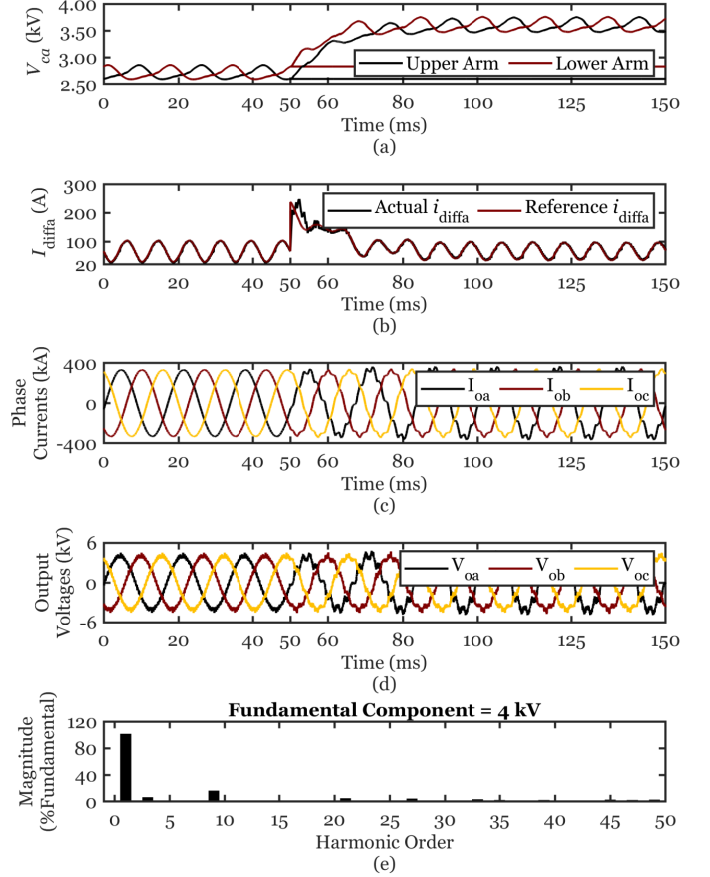


Fig. 8. Simulation results after an HBSM failure in phase a : (a) $v_{cu,j}^a$ and $v_{cl,j}^a$, (b) $i_{diff,a}$, (c) $i_{o,i}$, (d) $V_{o,i}$, and (e) harmonic spectrum of $V_{o,a}$.

is preserved. However, some of the triplen harmonics are increased compared to normal operation.

VI. REAL-TIME EVALUATION

This section evaluates the performance of the proposed method in real-time to validate the results of Section V. The MMC system is modeled on an RTDS NovaCor chassis with one core. It is modeled in the substep environment using the CHAINV5 model. This model uses a surrogate circuit to model each HBSM. The surrogate circuit consists of an upward diode, a capacitor, and a discharge resistor in parallel. In an electromagnetic transient simulation, HBSM capacitor branches are modeled with a resistance and a Thevenin history voltage source (V_{hc}). Alternating calculations of the HBSM capacitor voltage and V_{hc} occur during each time step. In addition, the MMC model in RTDS includes DC-link resistances, but not the parallel bypass switches. Instead, the bottom switch of the faulty HBSM is turned on to bypass that HBSM.

A. Steady-State Performance

This section evaluates the steady-state performance of the proposed method in real time. Fig. 9(a) shows the real-time steady-state results for capacitor voltages of phase a during normal operation. The proposed method successfully stabilizes the capacitor voltages at 2.72 kV with a ripple of 4.87%. Therefore, real-time and non-real-time capacitor voltage results are similar. Fig. 9(b) shows the real-time steady-state re-

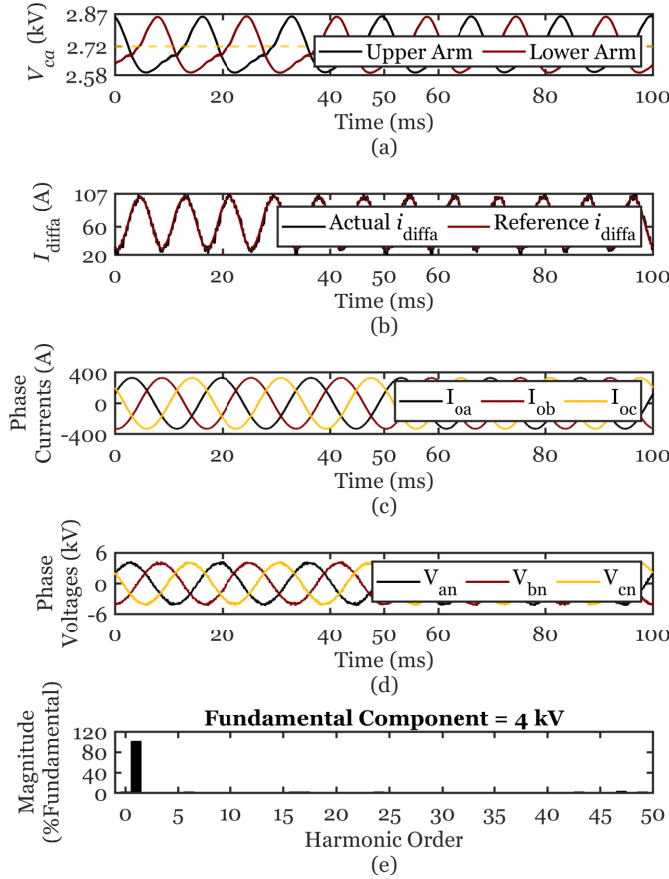


Fig. 9. Real-time steady-state results for (a) $v_{cu,j}^a$ and $v_{cl,j}^a$, (b) $i_{diff,a}$, (c) $i_{o,i}$, (d) $V_{o,i}$, and (e) harmonic spectrum of $V_{o,a}$ during normal operation.

sults for $i_{diff,a}$ during normal operation. It follows its reference and has a maximum of 108.6 A. Real-time and non-real-time results for $i_{diff,a}$ are similar. Fig. 9(c) shows the output currents. The proposed method generates balanced three-phase output currents with a peak magnitude of 333.2 A. Therefore, real-time and non-real-time results are similar. Fig. 9(d) shows $V_{o,i}$. The proposed method generates balanced three-phase output voltages with a peak magnitude of 4 kV, similar to non-real-time results. Fig. 9(d) shows the harmonic spectrum of $V_{o,i}$. The peak value of the fundamental component is 4 kV, and the low-order harmonics are eliminated, similar to non-real-time results.

B. Response to HBSM Failures

This section evaluates the performance of the proposed method under HBSM failures in real time. At $t = 50$ ms, SM_{u1a} and SM_{l1a} are bypassed and FT operation is established. Fig. 10(a) shows the capacitor voltages of phase a . The proposed method stabilizes the remaining capacitor voltages at 3.62 kV with a ripple of 3.81% at $t = 126.43$ ms, similar to their non-real-time response. Fig. 10(b) shows $i_{diff,a}$; it stabilizes with a maximum of 103.4 A at $t = 126.43$ ms and an overshoot to 243.8 A, similar to the non-real-time results. Fig. 10(c) shows the output currents. The proposed method generates balanced three-phase output currents and keeps their peak magnitude constant. However, the output currents become slightly more distorted. Fig. 10(d) shows the real-time results

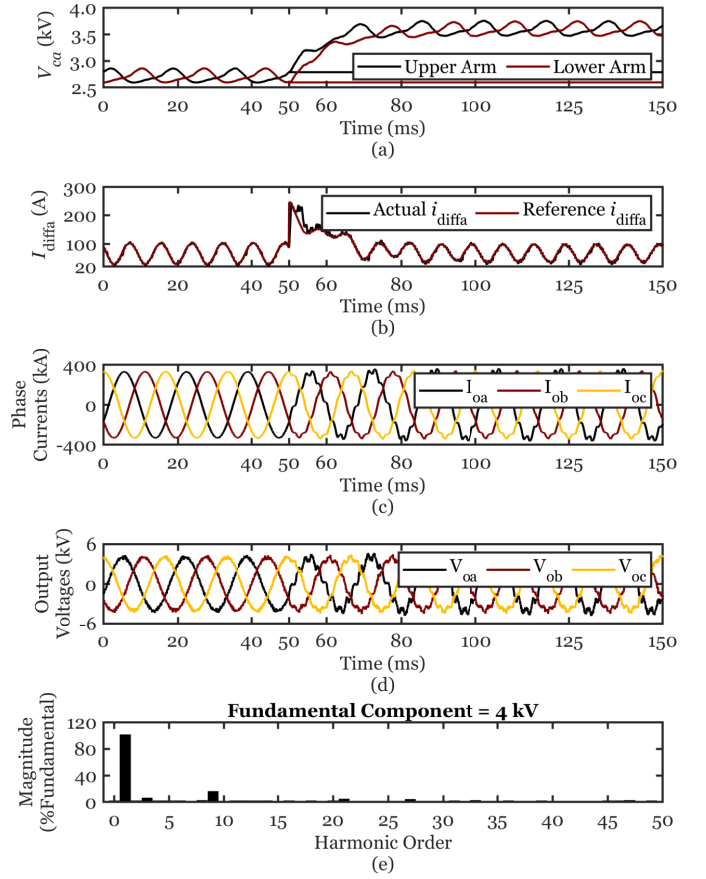


Fig. 10. Real-time results after an HBSM failure in phase a : (a) $v_{cu,j}^a$ and $v_{cl,j}^a$, (b) $i_{diff,a}$, (c) $i_{o,i}$, (d) $V_{o,i}$, and (e) harmonic spectrum of $V_{o,a}$ during FT operation.

for $V_{o,i}$ during FT operation. The proposed method generates balanced three-phase output voltages with a peak magnitude of 5 kV during FT operation and changes the waveform of $V_{o,a}$. Fig. 10(e) shows the harmonic spectrum for real-time $V_{o,a}$ during FT operation. The low-order harmonics are eliminated, and the fundamental component is preserved. However, some of the triplen harmonics are increased compared with normal operation. Therefore, the harmonic performance of real-time and non-real-time $V_{o,a}$ are similar.

VII. CONCLUSIONS

This paper proposes an FT SHE-PWM control method for MMCs. An MPC strategy is proposed to control the capacitor voltages and circulating currents. When an HBSM fails, the corresponding FT SHE-PWM waveform is constructed and sent to the MPC. Afterwards, the MPC applies the optimum insertion indices to properly control the MMC and generate the designed waveform at its output terminals. The proposed method is evaluated on a three-phase nine-level MMC in PSCAD/EMTDC and RTDS. Non-real-time simulation results demonstrate that the proposed method successfully controls the capacitor voltages and circulating currents while generating the correct SHE-PWM waveform the output terminals of the MMC during normal and FT operations. Real-time simulation results are provided to validate the non-real-time simulation results.

REFERENCES

- [1] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
- [2] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011.
- [3] E. Solas, G. Abad, J. A. Barrera, S. Aurtenexea, A. Cárcar, and L. Zając, "Modular multilevel converter with different submodule concepts—Part II: Experimental validation and comparison for HVDC application," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4536–4545, Oct. 2013.
- [4] J. Wang and Y. Tang, "A fault-tolerant operation method for medium voltage modular multilevel converters with phase-shifted carrier modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9459–9470, Oct. 2019.
- [5] S. Yang, Y. Tang, and P. Wang, "Seamless fault-tolerant operation of a modular multilevel converter with switch open-circuit fault diagnosis in a distributed control architecture," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7058–7070, Feb. 2018.
- [6] P. W. Hammond and M. F. Aiello, "Multiphase power supply with series connected power cells with failed cell bypass," U.S. Patents US5 986 909A, 2001.
- [7] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1080–1085, Aug. 2005.
- [8] M. Aleenejad, H. Mahmoudi, S. Jafarishadeh, and R. Ahmadi, "Fault-tolerant space vector modulation for modular multilevel converters with bypassed faulty submodules," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2463–2473, Mar. 2019.
- [9] P. Hu, D. Jiang, Y. Zhou, Y. Liang, J. Guo, and Z. Lin, "Energy-balancing control strategy for modular multilevel converters under submodule fault conditions," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 5021–5030, Sep. 2014.
- [10] Q. Yang, J. Qin, and M. Saeedifard, "Analysis, detection, and location of open-switch submodule failures in a modular multilevel converter," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 155–164, Feb. 2016.
- [11] F. Deng, Y. Tian, R. Zhu, and Z. Chen, "Fault-tolerant approach for modular multilevel converters under submodule faults," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7253–7263, Nov. 2016.
- [12] Q. Yang, J. Qin, and M. Saeedifard, "A postfault strategy to control the modular multilevel converter under submodule failure," *IEEE Trans. Power Del.*, vol. 31, no. 6, pp. 2453–2463, Dec. 2016.
- [13] A. MohammadHassani and E. Babaei, "Exchange market algorithm for selective harmonic elimination in cascaded multilevel inverters," *13th Int. Conf. Theory Appl. of Fuzzy Syst. Soft Comp.*, pp. 594–601, Dec. 2019.
- [14] S. Ziaeeinejad, Y. Sangsefidi, and A. Mehrizi-Sani, "A generalized switching strategy and capacitor sizing algorithm for granular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4443–4453, Jun. 2018.
- [15] Siemens, "The smart way HVDC plus-one step ahead." [Online]. Available: <https://www.energy.siemens.com/us/en/power-transmission/hvdc/hvdcplus/>
- [16] S. Yang, J. Fang, Y. Tang, H. Qiu, C. Dong, and P. Wang, "Modular multilevel converter synthetic inertia-based frequency support for medium-voltage microgrids," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8992–9002, Nov. 2019.
- [17] Q. Xiao, Y. Jin, L. Chen, X. Yu, H. Jia, H. Liu, R. Teodorescu, and F. Blaabjerg, "A simple operation approach for modular multilevel converter under grid voltage swell in medium-voltage microgrids," *IEEE Access*, vol. 7, pp. 147 280–147 291, Oct. 2019.
- [18] A. Pérez-Basante, S. Ceballos, G. Konstantinou, J. Pou, J. Andreu, and I. M. de Alegría, "(2N+1) selective harmonic elimination-PWM for modular multilevel converters: A generalized formulation and a circulating current control method," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 802–818, Jan. 2018.
- [19] A. Mohammadhassani and A. Mehrizi-Sani, "A fault tolerant selective harmonic elimination method for modular multilevel converters," *IEEE Power Energy Soc. General Meeting*, Aug. 2020.
- [20] D. Samajdar, T. Bhattacharya, and S. Dey, "A reduced switching frequency sorting algorithm for modular multilevel converter with circulating current suppression feature," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 480–10 491, Nov. 2019.
- [21] S. Yang, P. Wang, Y. Tang, M. Zagrodnik, X. Hu, and K. J. Tseng, "Circulating current suppression in modular multilevel converters with even-harmonic repetitive control," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 298–309, Jan. 2018.
- [22] R. P. Aguilera, P. Acuña, P. Lezana, G. Konstantinou, B. Wu, S. Bernet, and V. G. Agelidis, "Selective harmonic elimination model predictive control for multilevel power converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2416–2426, Mar. 2017.
- [23] Y. Sangsefidi, S. Ziaeeinejad, and A. Mehrizi-Sani, "Low switching frequency-based predictive control of a grid-connected voltage-sourced converter," *IEEE Trans. Energy Convers.*, vol. 32, no. 2, pp. 686–697, Jun. 2017.
- [24] A. Y. Fard and M. B. Shadmand, "Cooperative model predictive control scheme for dispersed smart inverters at the grid edge," *IEEE Texas Power Energy Conf.*, pp. 1–6, Feb. 2020.
- [25] K. Yang, Q. Zhang, R. Yuan, W. Yu, J. Yuan, and J. Wang, "Selective harmonic elimination with groebner bases and symmetric polynomials," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2742–2752, Apr. 2016.
- [26] M. Narimani, B. Wu, V. Yaramasu, and N. R. Zargari, "Finite control-set model predictive control (FCS-MPC) of nested neutral point-clamped (NNPC) converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7262–7269, Dec. 2015.
- [27] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015.
- [28] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.