24.6 A Time-Interleaved Filtering-by-Aliasing Receiver Front-End with >70dB Suppression at <4×Bandwidth Frequency Offset

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Programmable receiver front-ends has been a topic of enormous interest in recent years. Both N-path filtering [1,2] and charge-domain filtering [2] achieve sharp filtering but suffer from poor matching [1] or high noise figure (NF) [2]. Combining noise cancellation with the mixer-first architecture achieves low NF and high linearity [3], but only for far-out blockers.

The Filtering-by-Aliasing (FA) approach uses a sampled integrate-and-dump circuit with an appropriately chosen periodically time-varying resistor, $R(t)=R(t+T_S)$, to realize an equivalent FIR filter with desired impulse response, $g(\tau)$ (Fig. 24.6.1) [4]. Sharp transition bands, good S_{11}, and high linearity are achieved even for close-in blockers. Nevertheless, filter stop-band attenuation (A_{stop}) is limited since (1) the length of $g(\tau)$ is constrained to T_S, and (2) $R(t)$ itself is constrained due to S_{11} requirements. This may lead to residual blockers that alias in-band and cannot be further suppressed by additional filtering thereafter. While A_{stop} can be increased with a longer T_S (for the same transition band), the output sampling rate reduces correspondingly leaving adjacent aliasing bands unfiltered.

This work applies time-interleaving [5] to achieve A_{stop}>70dB without sacrificing filter sharpness, linearity, S_{11}, or NF. As shown in Fig. 24.6.2, two integrate-and-dump circuits are employed, each varied and sampled in a time-interleaved fashion, but with period $2T_S$. The filter realized, $g(\tau)$, is thus $2T_S$ long, while the overall sampling period remains T_S. This allows filters with higher A_{stop} without sacrificing filter sharpness. The channels interact, thus complicating the design of $R(t)$ to achieve desired filter response while achieving good S_{11}. Nonetheless, the 50Ω source sees the parallel combination of two resistors, relaxing the constraints on $R(t)$ compared to [4]. An example $R(t)$ designed for good S_{11} ideally realizes a filter with A_{stop} ~120dB. Suppression is ultimately limited by the accuracy of the resistor variation, with A_{stop} ~70dB when $R(t)$ is realized using an ideal 10b binary scaled resistor DAC (RDAC) (Fig. 24.6.2). Additionally, suppression is limited by the channel with lower precision. Hence, this work utilizes 13b RDACs to allow for calibrated accuracy of 10 to 11 bits in each channel.

While a 13b binary scaled RDAC is sufficient to realize $R(t)$ for A_{stop}>70dB, parasitics limit performance. The capacitors across the RDAC switches (C_{ds}) produce a code-dependent corner frequency between the resistance realized and the net parasitic capacitance in the off paths (Fig. 24.6.3). The frequency is lowest for large values of $R(t)$, degrading RDAC dynamic range. This effect can be alleviated in a differential configuration by adding cross-coupling capacitors equaling the total RDAC parasitic capacitance, leading to a code independent corner frequency as shown. Measurements show an improvement of 17dB in A_{stop} due to this technique.

The block diagram of the implemented RF front-end is shown in Fig. 24.6.3. The 50Ω input is converted to differential using an external balun transformer. The receiver IC consists of two identical time-interleaved paths. In each path the balun output is connected to 13b RDACs, $R(t)$, whose control bits are periodic with the period, $2T_s$, and are varied at the rate, f_{CK}. The cross-coupled capacitors are implemented using dummy RDACs with all switches turned off. The differential RF current generated is mixed down to baseband by a set of eight 25% duty-cycle mixer switches switching at the LO frequency, f_{LO}. The base-band is composed of inverter-based op-amps with ping-pong capacitor banks around them. This allows for one capacitor to be connected across the op-amp while the voltage stored on the other is read and then reset. RDAC controls are stored in a register-based memory, and are read out cyclically based on the input clock, f_{CK}. The sampling and reset clocks for the capacitor banks are generated by dividing f_{CK}. The RDAC controls and the sampling and reset clocks for the two paths are offset in time by T_s to achieve the time-interleaving operation. The IC can be reconfigured for single-ended and non-interleaved operation as well.

The IC was fabricated in TSMC 1P6M 65nm CMOS process and was packaged in a 40-pin 5mmx5mm QFN package. The op-amps use non-minimum length high-Vt devices, have a DC gain of ~35dB, and g_m of ~125mS. The 13b RDAC uses *rppoly* resistors and is designed for a minimum resistance of 15Ω. All switches are implemented using transmission gates with equally sized NMOS and PMOS transistors, with LO switches designed to have an on-resistance of 3Ω. The RDAC is calibrated at start-up using a DC resistor divider arrangement. MIM capacitors are used for the capacitors, C, that are tunable from 10-70pF. A supply voltage of 1.2V is used for the op-amps, the LO dividers, as well as the drivers for controlling the RDAC and LO switches. The DC bias of the entire chain is set to around 0.6V due to the op-amp biasing at reset. The rest of the circuitry runs on a 1V supply. For a 10MHz bandwidth (BW) filter centered on f_{LO} =500MHz, a current of 64.7mA is drawn from the 1.2V supply, with each op-amp consuming 6.5mA, the LO divider and switch drivers consuming about 12.7mA, while the other digital blocks draw 7.75mA from the 1V supply for a nominal clock frequency of f_{CK}=1GHz. The system was verified to work up to f_{CK}=2GHz.

The sampled outputs of the time-interleaved paths are buffered and combined externally. Figure 24.6.4 shows the measured filter response in three different time-interleaved 10MHz BW filter configurations (filters 1-3) that vary in transition BW and attenuation. The transition BWs for filters 1, 2, and 3 were 17MHz, 25MHz, and 40MHz respectively, while the achieved stop-band rejection was observed to be better than 45dB, 58dB, and 70dB respectively. In comparison, the measured non-interleaved filter achieved a stop-band rejection of only 40dB with a transition BW of 35MHz. The filter BW was varied from 2.5-40MHz by varying T_s. The receiver gain obtained for the 10MHz BW filter with C=70pF was 23dB. The gain scales linearly with T_s and inversely with C. f_{LO} was also varied from 100MHz to 1GHz as shown in Fig. 24.6.4. The gain reduced by ~4dB from f_{LO}=100MHz to 1GHz.

Figure 24.6.5 shows linearity and S_{11} measurements for a 10MHz BW filter 1 configuration with f_{LO} =500MHz and C=70pF. While the in-band IIP_3 was measured to be about +8.2dBm, OOB IIP_3 was better than +21.4dBm, and OOB IIP_2 was better than +64dBm, both at 12MHz offset from the carrier. The S_{11} is better than -10dB for most of the receiver LO range, and degrades to only -9dB at f_{LO} =1GHz. The measured NF was 7dB, and worsened by only 4.5dB when a 0dBm CW blocker was present at 30MHz offset. The small-signal NF and S_{11} are degraded slightly compared to the non-interleaved case [4] due to parasitic capacitance from the additional RDACs at the input.

Figure 24.6.6 compares this work with recent designs. This work maintains the high linearity of FA [4] with sharper filtering than state-of-the-art [2]. Figure 24.6.7 shows the die-photo of the fabricated IC. The active area is 2.3mm^2, 70% of which is occupied by capacitors.

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References:
[1] Darvishi, M., et al., "A 0.1-to-1.2GHz Tunable 6th-Order N-Path Channel-Select Filter with 0.6dB Passband Ripple and +7dBm Blocker Tolerance," ISSCC Dig. Tech Papers, pp.172-173, Feb. 2013.
[2] Xu, Y., et al., " A Switched-Capacitor RF Front End With Embedded Programmable High-Order Filtering," IEEE J. Solid-State Circuits, vol.51, no.5, pp.1154-1167, May 2016.
[3] Murphy, D., et al., "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications," IEEE J. Solid-State Circuits, vol.47, no.12, pp.2943-2963, Dec. 2012.
[4] Hameed, S., et al., "A Programmable Receiver Front-End Achieving >17dBm IIP_3 at <1.25×BW Frequency Offset," ISSCC Dig. Tech Papers, pp.446-447, Feb. 2016.
[5] M. Rachid, et al., "Filtering by Aliasing," IEEE Trans. on Signal Processing, vol.61, no.9, pp. 2319-2327, May 2013.

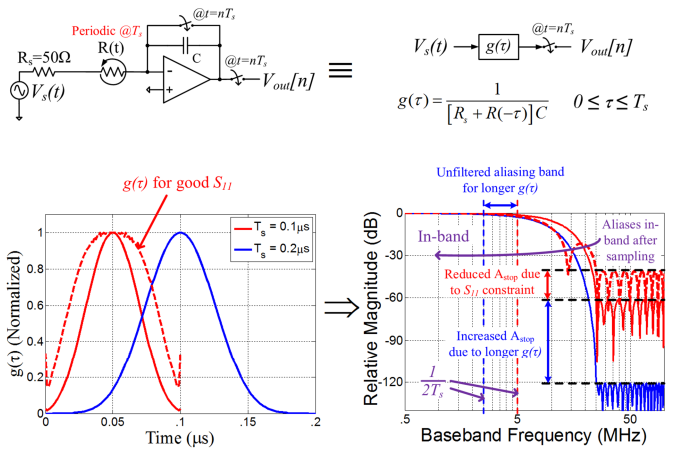

Figure 24.6.1: Limitations of the baseband used in [4], and the effects of lengthening its equivalent impulse response, g(τ), by increasing sampling period T_s (increased A_{stop} but extra aliasing bands).

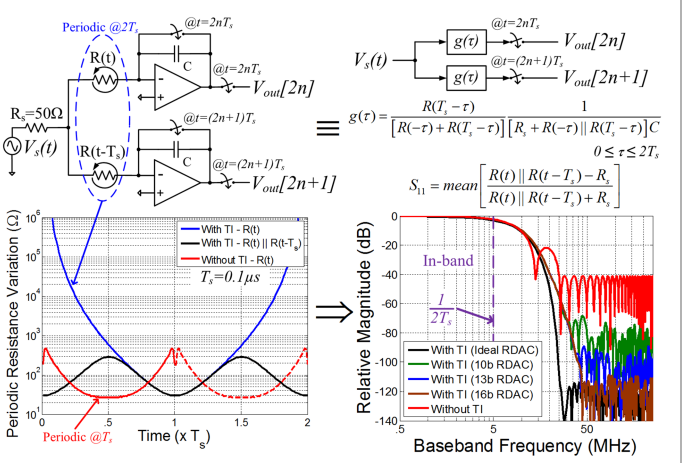

Figure 24.6.2: The baseband of the implemented receiver front-end with time-interleaving (TI), its equivalent impulse response, g(τ), and the achieved baseband filter (RDAC min resistance = 30Ω).

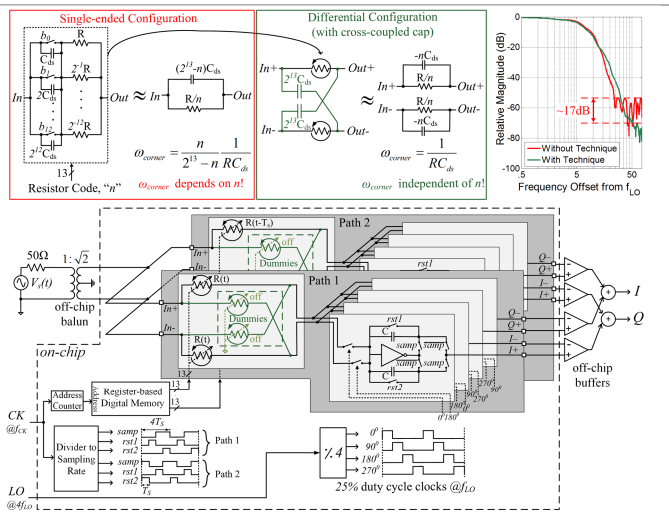

Figure 24.6.3: top) Effect of parasitics on a 13b binary-scaled RDAC and its mitigation in a differential configuration, bottom) Block diagram of the fabricated IC.

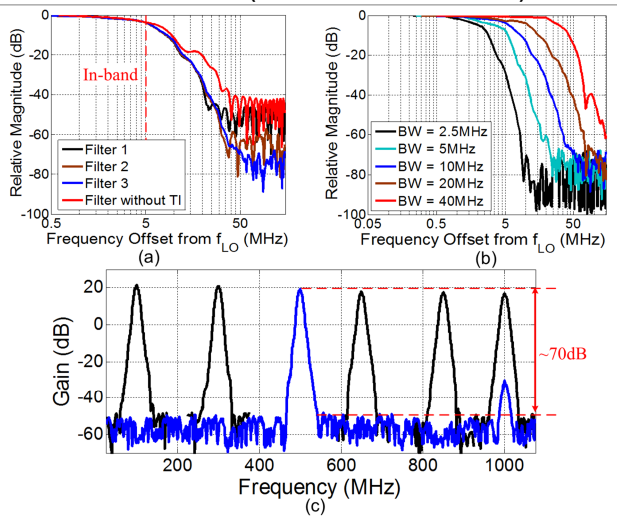

Figure 24.6.4: a) Measured 10MHz RF BW filter responses, b) Filter 3 responses for BW tuned from 2.5 to 40MHz, c) Filter 3 responses for the LO varied from 0.1 to 1GHz (in 6 steps).

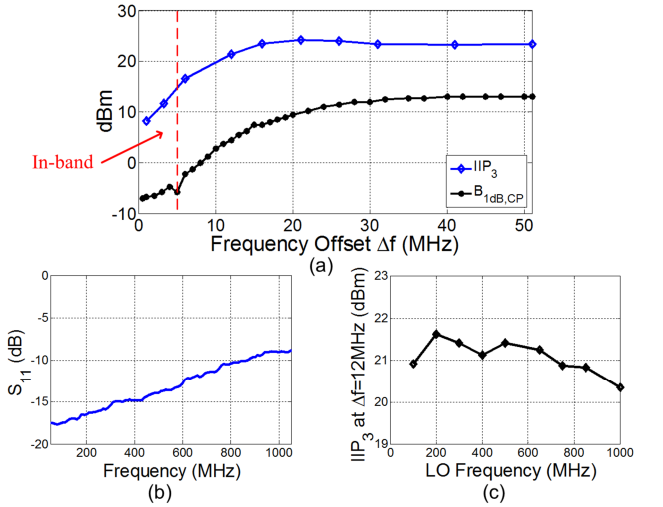

Figure 24.6.5: a) Measured IIP_3 and $B_{1dB,CP}$ at different frequency offsets from LO, b) S_{11}, c) OOB IIP_3 at Δf=12MHz for LO varied from 0.1 to 1GHz, all for a 10MHz RF BW filter in filter 1 configuration.

Metric / Architecture	[1] N-path	[2] N-path + DT filtering	[3] Mixer-first with Noise Cancelling	[4] FA	This Work FA with Time Interleaving
Technology	65nm	40nm	40nm	65nm	65nm
RF Frequency (GHz)	0.1-1.2	0.1-0.7	0.08-2.7	0.1-1	0.1-1
RF Input	Differential	Differential	Single-ended	Single-ended	Differential
BW (MHz)*	8	6.4-9.6	4	2.5-40	2.5-40
Stop-band Rejection (Transition BW)	59dB (12×BW)	>70dB (~8.5×BW)	NA	>35dB (2.5×BW) >50dB (6.5×BW)	>45dB (1.7×BW) >70dB (4×BW)
In-band IIP_3 (dBm)	-12	NA	-20	+1	+8
Out-of-band IIP_3 (dBm)	+26 (Δf=6.25×BW)	+24 (Δf=4.7×BW)	+13.5 (Δf=20×BW)	+17 (Δf=1.2×BW)	+21 (Δf=1.2×BW)
Out-of-band IIP_2 (dBm)	NA	NA	+55	+60	+64
$B_{1dB,CP}$ (dBm)	+7 (Δf=6.25×BW)	+14.7 (Δf=4.7×BW)	-2 (Δf=20×BW)	+0.7 (Δf=2×BW) +8 (Δf=4×BW)	+9.5 (Δf=2×BW) +13 (Δf=4×BW)
S_{11} (dB)	-5 to -8	<-10	<-8.8	<-10	<-9
Gain (dB)	25	40	72	18.9	23
NF (dB)	2.8	6.8-9.7	1.9	6.5	7*
Supply Voltage (V)	1.2	1.2/1.6	1.2/2.5	1.2/1	1.2/1
Power Consumption	15-48mA	59-105mW	27-60mA	56-62mA	64-84mA**
Active Area (mm²)	0.27	2.03	1.2	2	2.3

*RF bandwidth (twice the baseband bandwidth).
*Excludes balun loss.
**Varies with f_{LO}. Power consumption = 73mA for f_{LO} = 0.5GHz.

Figure 24.6.6: Comparison table.

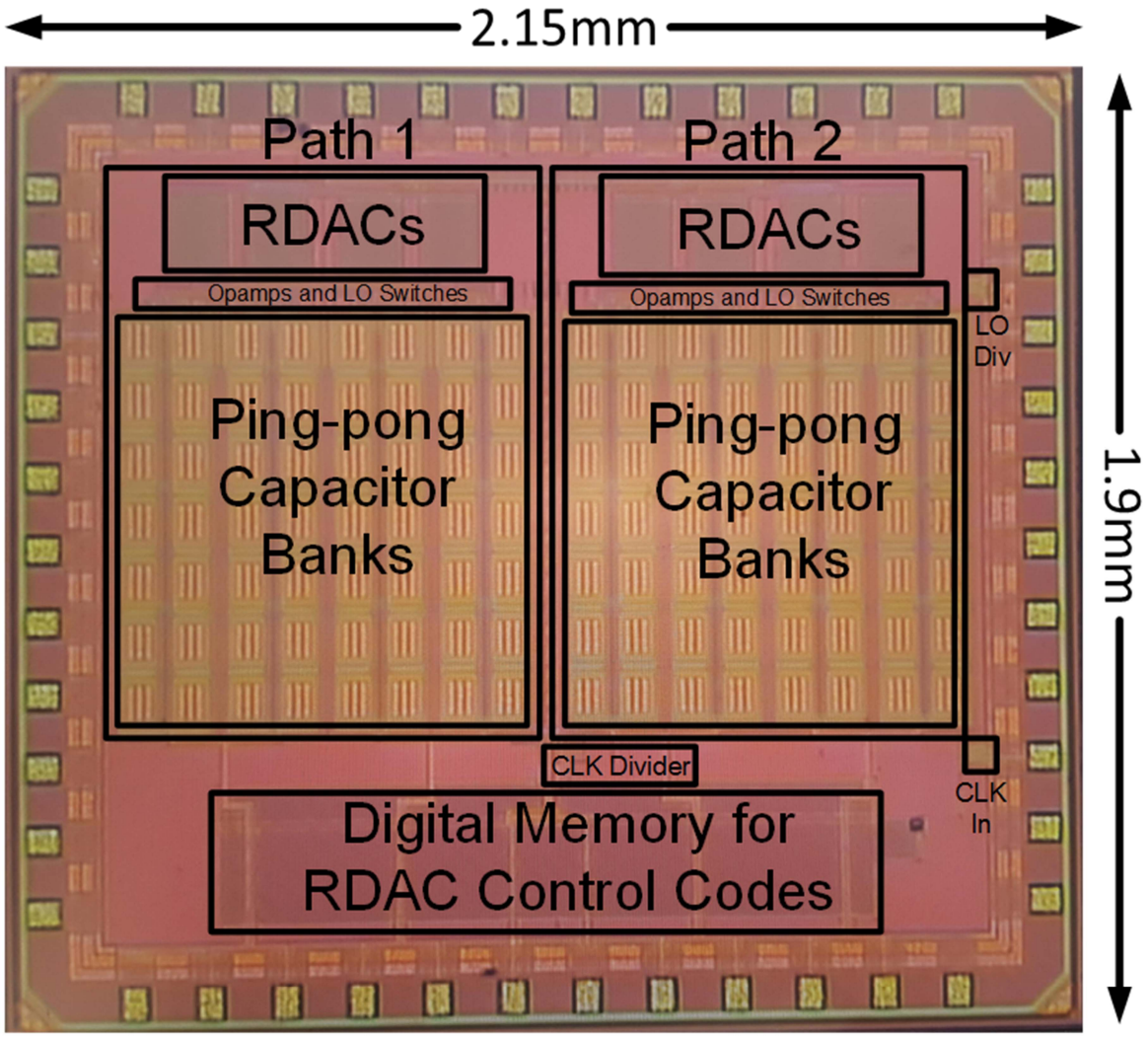

Figure 24.6.7: Die micrograph.