26.6 A Programmable Receiver Front-End Achieving >17dBm IIP3 at <1.25×BW Frequency Offset

Sameed Hameed[1], Neha Sinha[1], Mansour Rachid[2], Sudhakar Pamarti[1]

[1]University of California, Los Angeles, CA, [2]Silvus Technologies, Los Angeles, CA

Recent work on highly selective reconfigurable radios has focused on techniques such as DT analog signal processing [1], N-path filtering [2], and mixer-first approaches [3,4]. Mixer-first receivers have been able to achieve excellent out-of-band (OOB) linearity even with noise cancellation [3], but only for far-out blockers due to only first order baseband filtering. Higher order baseband gives sharper filtering, but is not as linear [4], while high order active N-path filters have poor S_{11} [2]. DT approaches are also limited by the linearity of the front-end LNTA [1]. Hence, new approaches are needed to handle large blockers that are close to the signal band.

This paper proposes a programmable receiver front-end that achieves sharp filtering, while maintaining linearity in the presence of large close-in blockers. It uses the recent concept of Filtering by Aliasing (FA) [5] that is explained in Fig. 26.6.1. Suppose we have a simple filter, $h(\tau)$, whose output is sampled at a sampling period, T_s. It can be shown that if the input, $x(t)$, to the filter is first multiplied with a periodic signal $d(t)$ whose period is T_s, then the system is equivalent to the input being passed through an apparent LTI filter, $g(\tau)= h(\tau)d(-\tau)$, before sampling. Furthermore, if $d(t)$ is designed appropriately, $g(\tau)$ will be a far more selective filter than $h(\tau)$. It is easier to see what happens in the frequency domain. The input spectrum, $X(f)$, is spread in the frequency domain due to the convolution with $D(f)$, before filtering by $H(f)$. On sampling, the spread copies of the unwanted input signal bands cancel off, while the wanted signal band remains. Hence, filtering by aliasing! Note that the multiplication of the input with a periodic $d(t)$ essentially makes the system linear periodically time-varying (LPTV) for the input.

FA was recently demonstrated using a passive LPTV circuit [6]. While the circuit was able to demonstrate sharp filtering responses, it is primarily intended as a baseband filter, and cannot be directly used at RF due to its poor matching with the antenna interface. To circumvent this issue, we propose the FA structure shown in Fig. 26.6.2. The source is loaded by an LPTV resistor, $R(t)$, that is followed by a current integrator, whose output is periodically sampled and reset. This structure achieves the following: first, the current, $i(t)$, depends only on $R(t)$ (due to op-amp virtual ground), and so any desired periodic $d(t)$ variation can be achieved. Since $i(t)$ is then passed to a current integrator, the filter $h(\tau)$ is simply a step function, $u(\tau)$, weighed by the capacitance, C. Thus, the apparent filter, $g(\tau)$, primarily depends on the resistance variation, $R(t)$, with C only affecting DC gain. Second, it can be shown that the S_{11} for the structure also depends only on $R(t)$ (shown in Fig. 26.6.2). Hence, while designing the optimum filter $g(\tau)$ using [5], an additional S_{11} constraint can be added to ensure matching. Furthermore, the integrator avoids any voltage gain at RF, and keeps the op-amp in feedback (like in [3]), making it highly linear.

Figure 26.6.2 shows an example variation of $R(t)$ over a period, T_s, resulting in an apparent LTI filter with impulse response, $g(\tau)$, and magnitude response, $G(f)$, for R_s=50Ω. Note that in reality, $R(t)$ can only be varied in discrete time steps, for example at a rate, f_{CK}. Hence, the resultant impulse response is a sampled and held version of the ideal impulse response, resulting in images in the magnitude response at offsets of f_{CK}. Nevertheless, the images are shaped by a sinc envelope, and so can be reduced below the filter stop-band floor with a high enough f_{CK}.

The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, T_s, and are varied at the rate, f_{CK}. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, f_{LO}. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor bank. Hence, while one capacitor is connected across the op-amp, the voltage stored on the other is read and then reset. The controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, f_{CK}. The sampling and reset clocks for the capacitor banks are generated by dividing f_{CK}.

The IC was fabricated in TSMC 1P6M 65nm CMOS process and was packaged in a 40-pin 5mmx5mm QFN package. The op-amps use non-minimum length devices, and have a DC gain of about 20dB, with g_m of about 125mS. The 9-bit resistor DAC uses *rppoly* resistors and is designed for a minimum resistance of 15Ω. All switches are implemented using transmission gates with equally sized NMOS and PMOS transistors to minimize clock feed-through and charge injection, with the LO switches designed to have an on-resistance of 3Ω. MIM capacitors are used for the capacitors, C, that are tunable from 20-140pF. A supply voltage of 1.2V is used for the op-amps, the LO dividers, as well as the drivers for controlling the resistor DAC and LO switches. The DC bias of the entire chain is set to around 0.6V due to the op-amp biasing at reset. The rest of the circuitry runs on a 1V supply. For a 5MHz bandwidth (BW) filter centered on f_{LO} =500MHz, the 1.2V supply draws a current of 57mA from the supply, with each op-amp consuming 13mA, the LO divider and switch drivers consuming about 5mA, while the digital and clock generation blocks draw 2mA from the 1V supply for a nominal clock frequency of f_{CK}=1GHz. The system was verified to work up to f_{CK}=2GHz.

The outputs are buffered externally for measurements. Four filter configurations were considered – filters 1, 2, and 3 were designed with an S_{11} constraint and different transition BWs, while filter 4 only had a transition BW constraint. Figure 26.6.4 shows the measured frequency response of the filter in these configurations. The receiver gain obtained for the 5MHz BW filter with C=100pF was 18.9dB when configured for matching (filters 1, 2, and 3) and 15.4dB for filter 4. The transition BWs for filters 1, 2, 3, and 4 were 12.5MHz, 22.5MHz, 32.5MHz, and 17.5MHz respectively, while the achieved stop-band rejection was observed to be better than 35dB, 45dB, 50dB, and 48dB respectively. The filter BW was varied from 2.5-40MHz by varying the resistor variation period (and sampling interval), T_s. The gain scales linearly with T_s and inversely with C. f_{LO} was also varied from 100MHz to 1GHz as shown in Fig. 26.6.4. The gain reduced by ~2dB from f_{LO}=100MHz to 1GHz.

Figure 26.6.5 shows linearity and S_{11} measurements. For a 5MHz BW filter 1 configuration (designed for matching) with f_{LO} =500MHz and C=100pF, while the in-band IIP_3 was measured to be about +1dBm, OOB IIP_3 was better than +17dBm, and OOB IIP_2 was better than +60dBm without calibration, both at 6MHz offset from the carrier. The S_{11} was at least -11dB, and better than -12dB for most of the receiver LO range. The measured noise figure (NF) was 6.5dB. The NF degraded by 12dB if a 0dBm blocker was present at 16MHz offset (simulated LO phase noise at blocker offset was -155dBc/Hz). It should be noted that if matching is not needed (filter 4 configuration), the in-band IIP_3 improves to +5dBm, while the OOB IIP_3 was +15dBm at 6MHz offset. The blocker 1dB gain compression point ($B_{1dB,CP}$) is also improved. The S_{11} degrades to only -8dB.

Figure 26.6.6 compares this work with recent designs. This work achieves comparable linearity for blockers at much lower frequency offsets than prior art, with good S_{11} and acceptable NF. Figure 26.6.7 shows the die-photo. The active area is 2mm^2, two-thirds of which is occupied by capacitors.

Acknowledgements:

This work was supported in part by the National Science Foundation under NSF grant ECCS 1408647.

References:

[1] Tohidian, M., et al., "3.8 A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International , vol., no., pp.1-3, 9-13 Feb. 2014

[2] Darvishi, M., et al., "A 0.1-to-1.2GHz tunable 6th-order N-path channel-select filter with 0.6dB passband ripple and +7dBm blocker tolerance," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , vol., no., pp.172-173, 17-21 Feb. 2013

[3] Murphy, D., et al., "A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications," in Solid-State Circuits, IEEE Journal of , vol.47, no.12, pp.2943-2963, Dec. 2012

[4] Run Chen; Hashemi, H., "19.3 Reconfigurable SDR receiver with enhanced front-end frequency selectivity suitable for intra-band and inter-band carrier aggregation," in Solid- State Circuits Conference - (ISSCC), 2015 IEEE International , vol., no., pp.1-3, 22-26 Feb. 2015

[5] M. Rachid, et al., "Filtering by Aliasing," in Signal Processing, IEEE Transactions on , vol.61, no.9, pp.2319-2327, May1, 2013

[6] N. Sinha, et al., "A sharp programmable passive filter based on filtering by Aliasing," in VLSI Circuits (VLSI Circuits), 2015 Symposium on , vol., no., pp.C58-C59, 17-19 June 2015

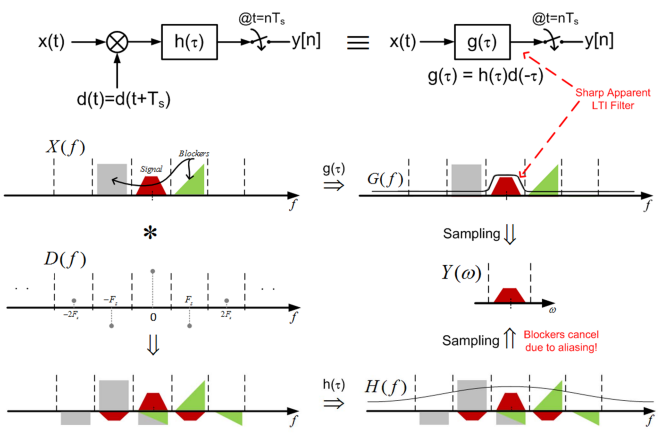

Figure 26.6.1: The concept of Filtering by Aliasing (FA)

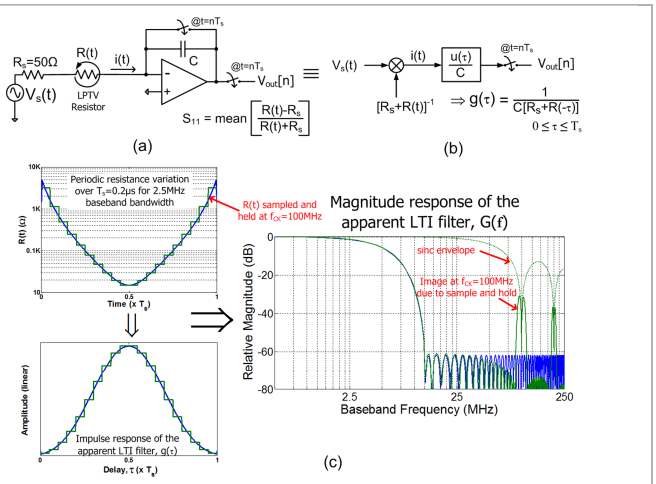

Figure 26.6.2: a) Proposed baseband of FA based receiver and its wideband S_{11}, b) Equivalent FA system, c) Example periodic resistor variation and corresponding filtering obtained

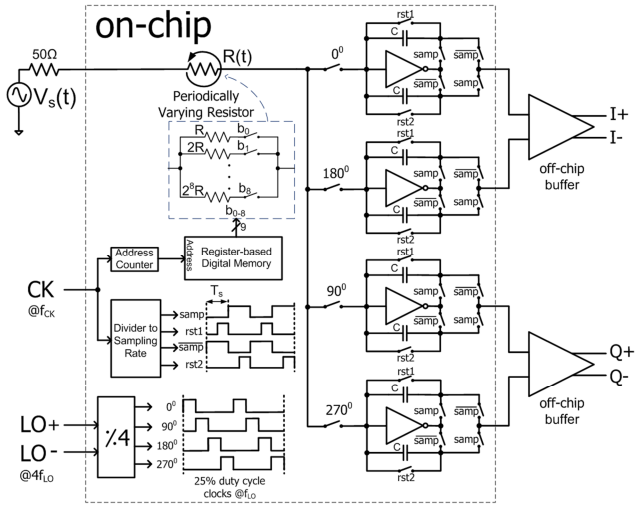

Figure 26.6.3: Block diagram of the fabricated IC

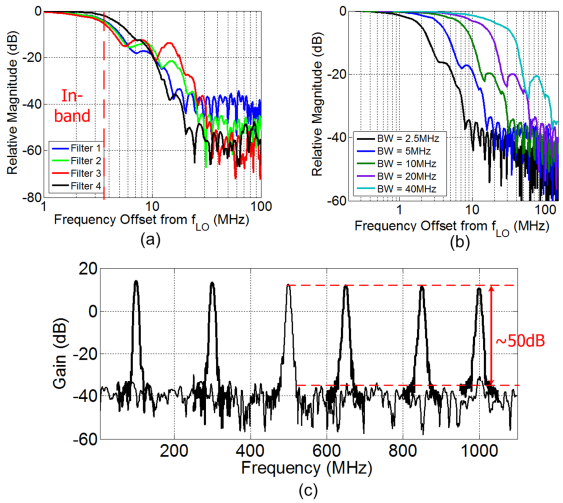

Figure 26.6.4: a) Measured 5MHz RF BW filter responses. Filters 1-3 are designed with an S_{11} constraint, b) Filter 1 responses for BW tuned from 2.5-40MHz, c) Filter 4 responses for the LO varied from 0.1-1GHz

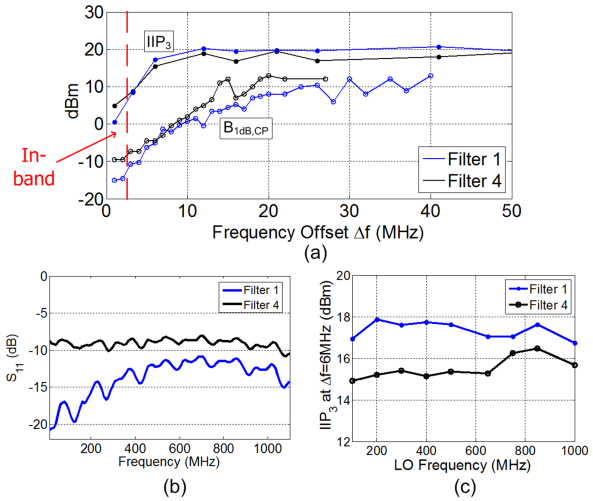

Figure 26.6.5: a) Measured IIP_3 and $B_{1dB,CP}$ for different frequency offsets from LO for a 5MHz RF BW filter, b) S_{11} for filter 1 (designed for matching) and filter 4, c) OOB IIP_3 at Δf=6MHz for LO from 0.1-1GHz

Metric	[1]	[2]	[3]	[4]	This Work	
Architecture	DT Analog	N-path	Mixer-first with Noise Cancelling	Mixer-first + 2nd Order Baseband	FA	FA with Matching
Technology	65nm	65nm	40nm	65nm	65nm	65nm
RF Frequency (GHz)	1.8-2.5	0.1-1.2	0.08-2.7	0.5-3	0.1-1	0.1-1
RF Input	Single-ended	Differential	Single-ended	Differential	Single-ended	Single-ended
BW (MHz)*	0.2-20	8	4	2-60	2.5-40	2.5-40
Transition BW	~4 x BW	12 x BW	NA	~5 x BW	3.5 x BW	2.5˜ x BW
Stop-band Rejection (dB)	>70	59	NA	>30	>48	>35˜
In-band IIP_3 (dBm)	-7	-12	-20	-4.8	+5	+1
Out-of-band IIP_3 (dBm)	NA	+26 (Δf/BW=6.25)	+13.5 (Δf/BW=20)	-4.8 (Δf/BW=2)	+15 (Δf/BW=1.2)	+17 (Δf/BW=1.2)
Out-of-band IIP_2 (dBm)	+85	NA	+55	NA	+55	+60
$B_{1dB,CP}$ (dBm)	NA	+7 (Δf/BW=6.25)	-2 (Δf/BW=20)	-10 (Δf/BW=2)	+2 (Δf/BW=2), +13 (Δf/BW=4)	+0.7 (Δf/BW=2), +8 (Δf/BW=4)
S_{11} (dB)	<-10	-5 to -8	<-8.8	<-10	<-8	<-10
Gain (dB)	82	25	72	50	15.4	18.9
NF (dB)	3.2-4.5	2.8	1.9	4.7	9.8	6.5
Supply Voltage (V)	1.2/2	1.2	1.2/2.5	1.2/2.5	1.2/1	1.2/1
Power Consumption	55-65mW	15-48mA	27-60mA	96mW	56-62mA**	56-62mA**
Active Area (mm^2)	1.1	0.27	1.2	7.8	2	2

*RF bandwidth (twice the baseband bandwidth).
˜For filter 1. Tunable with a trade-off between transition BW and stop-band rejection.
**Varies with f_{LO}. Power consumption = 59mA for f_{LO}=0.5GHz.

Figure 26.6.6: Comparison Table

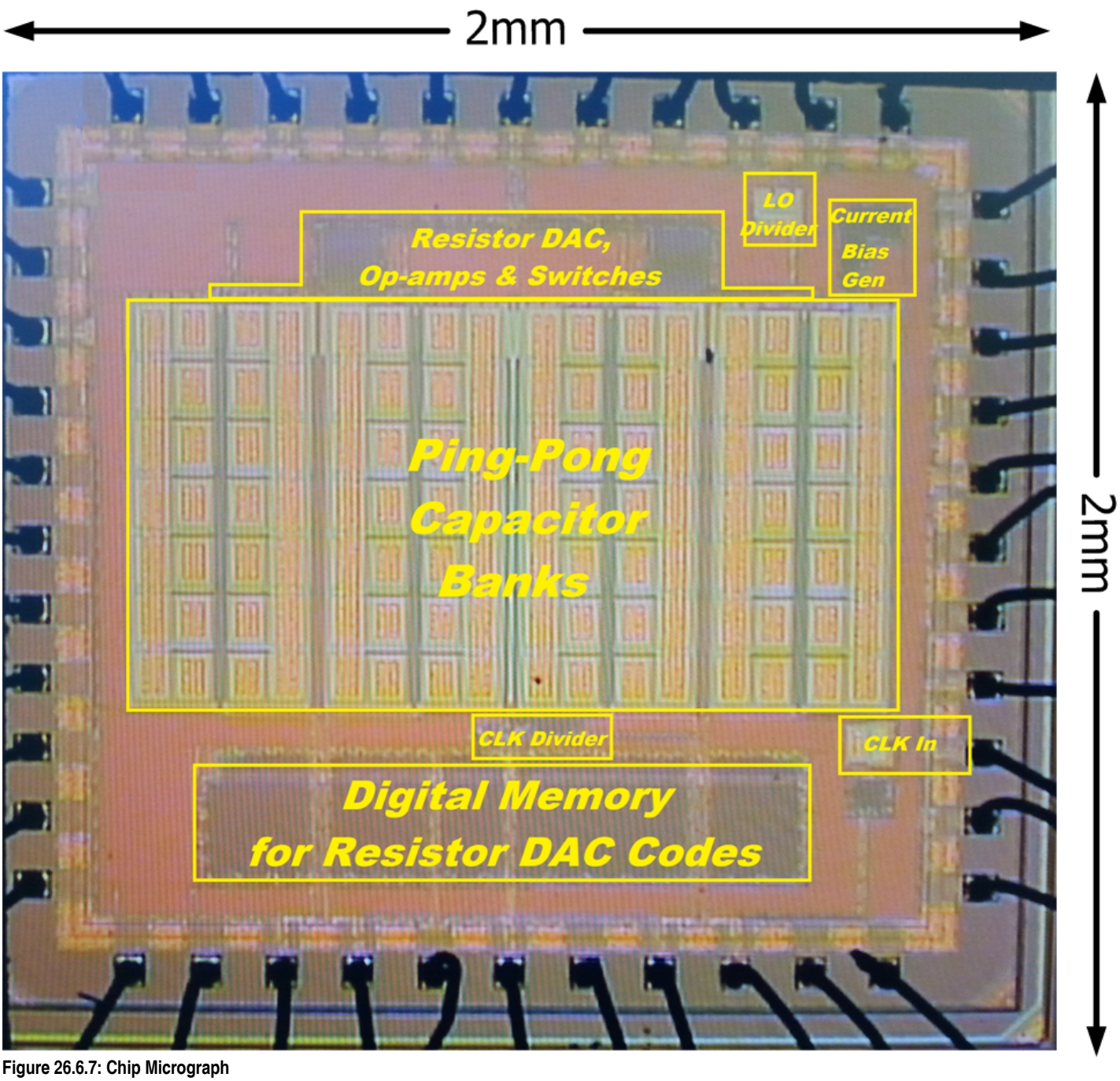

Figure 26.6.7: Chip Micrograph