Recent work on highly selective reconfigurable radios has focused on techniques such as DT analog signal processing [1], N-path filtering [2], and mixer-first approaches [3,4]. Mixer-first receivers have been able to achieve a high enough $f_{\text{CK}}$. Nevertheless, the images are shaped $G(f)$, for $R_s=50\Omega$, also depends only on $R(t)$ (shown in Fig. 26.6.2). Hence, while designing the input with a periodic $d(t)$ essentially makes the system linear periodically time-varying (LPTV) for the input. 

FA was recently demonstrated using a passive LPTV circuit [6]. While the circuit was able to demonstrate sharp filtering responses, it is primarily intended as a baseband filter, and cannot be directly used at RF due to its poor matching to a high enough $f_{\text{CK}}$. The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, $T_s$, and are varied at the rate, $f_{\text{CK}}$. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, $f_{\text{LO}}$. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor, and the controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, $f_{\text{CK}}$. The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, $T_s$, and are varied at the rate, $f_{\text{CK}}$. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, $f_{\text{LO}}$. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor, and the controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, $f_{\text{CK}}$. The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, $T_s$, and are varied at the rate, $f_{\text{CK}}$. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, $f_{\text{LO}}$. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor, and the controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, $f_{\text{CK}}$. The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, $T_s$, and are varied at the rate, $f_{\text{CK}}$. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, $f_{\text{LO}}$. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor, and the controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, $f_{\text{CK}}$. The block diagram of the implemented FA-based RF front-end is shown in Fig. 26.6.3. The antenna input is connected to the LPTV resistor, $R(t)$, that is built as a 9-bit resistor DAC whose control bits are periodic with the period, $T_s$, and are varied at the rate, $f_{\text{CK}}$. The RF current thus generated is mixed down to baseband by a set of four 25% duty-cycle mixer switches switching at the LO frequency, $f_{\text{LO}}$. The base-band is composed of integrators using inverter-based op-amps. The capacitor around each op-amp is built as a ping-pong capacitor, and the controls for the resistor DAC are stored in an on-chip register based memory, and read out cyclically based on the input clock, $f_{\text{CK}}$.
Figure 26.6.1: The concept of Filtering by Aliasing (FA)

Figure 26.6.2: a) Proposed baseband of FA based receiver and its wideband $S_{11}$, b) Equivalent FA system, c) Example periodic resistor variation and corresponding filtering obtained

Figure 26.6.3: Block diagram of the fabricated IC

Figure 26.6.4: a) Measured 5MHz RF BW filter responses. Filters 1-3 are designed with an $S_{11}$ constraint, b) Filter 1 responses for BW tuned from 2.5-40MHz, c) Filter 4 responses for the LO varied from 0.1-1GHz

Figure 26.6.5: a) Measured IIP3 and $B_{1dB,CP}$ for different frequency offsets from LO for a 5MHz RF BW filter, b) $S_{11}$ for filter 1 (designed for matching) and filter 4, c) OOB IIP3 at $\Delta f$=6MHz for LO from 0.1-1GHz

Figure 26.6.6: Comparison Table