Time-Varying Circuit Approaches for Software Defined and Cognitive Radio Applications

S. Pamarti, N. Sinha, S. Hameed
Electrical Engineering Department
University of California, Los Angeles
Los Angeles, CA, U.S.A.
{spamarti,nsinha,sameed}@ucla.edu

M. Rachid
Silvus Technologies
Los Angeles, CA, U.S.A.
mansour.k.rachid@gmail.com

Abstract— **A brief overview of the recently developed "Filtering by Aliasing" (FA) technique is presented. FA utilizes a linear, periodically time varying (LPTV) circuit followed by a sampler to achieve sharp apparent filters from a continuous-time (CT) input to a discrete-time (DT) output. Applications to RF front-ends and spectrum scanners along with the effect of circuit parasitics on achievable performance is also described.**

Keywords: SDR, Cognitive Radio, LPTV, Spectrum Sensing, Recievers

I. INTRODUCTION

As communications technology migrates towards wideband software-defined radios (SDR) and cognitive radios (CR), receivers are expected to dynamically acquire or monitor one or more signals of interest whose frequency locations, bandwidths, and interference scenarios may not be known *apriori*. Direct digitization at the antenna itself has long been a cherished goal but analog-to-digital converter (ADC) performance is improving far too slowly for this to be feasible in the foreseeable future. So, sharp programmable analog filters are essential to the operation of such receivers. Off-chip filters (e.g., SAW filters), which are employed in traditional receivers, provide the requisite sharp filtering but are too bulky, costly, and inflexible. Conventional integrated filters e.g., gm-C or active-RC are programmable but exhibit strict trade-offs between power, area, noise, linearity and filter sharpness and are difficult to implement in fine CMOS processes. Techniques such as DT analog signal processing [1] and N-path filters [2], allow for sharp programmable filters at baseband and RF, respectively, but suffer from non-linearity.

The authors recently developed a new linear periodically time varying (LPTV) circuit technique [3] and demonstrated agile RF front-end [4] and a passive spectrum scanner [5] with best reported linearity (and in the latter case, power consumption) of comparable prior art. This paper presents (a) an overview of the LPTV technique and its application to RF front-ends and spectrum scanners, and (b) examines the role of transistor parasitics in their performance. Section II describes the basic idea, referred to as "Filtering by Aliasing (FA)" while Section III summarizes its application to RF front-ends and spectrum scanners. Section IV presents a discussion on the effects of transistor parasitics on LPTV circuit performance.

This work was supported, in part, by National Science Foundation Award ECCS-1408647.

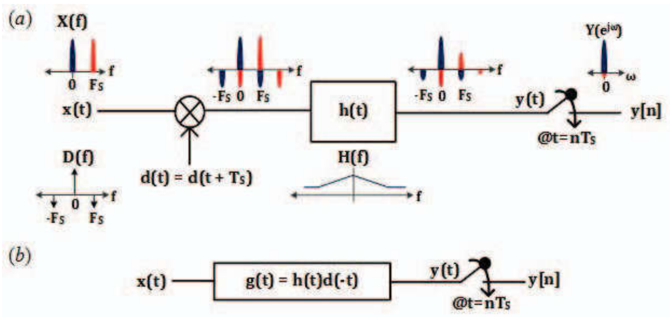

Figure 1: (a) Block diagram of Filtering by Aliasing (FA) (b) Equivalent LTI system for samples of y[n].

II. FILTERING BY ALIASING

Fig. 1(a) shows a simplified block diagram of Filtering by Aliasing [3]. The input, x(t), is multiplied (or "spread") by a periodic signal, $d(t) = d(t+T_s)$, and filtered by a simple analog filter e.g., an integrator or 1st order RC; the result is sampled uniformly at a rate, $F_S = 1/T_S$. The system is equivalent to the input being passed through an equivalent LTI filter with impulse response, $g(t) = h(t)d(-t)$, followed by sampling (see Fig. 1(b)). Essentially, multiplication with a periodic d(t) causes weighted and frequency translated copies of the input spectrum. Subsequent sampling causes these weighted spectral copies to alias on top of each other. By choosing d(t) appropriately for the given h(t), the low-frequency in-band signals, $[0, F_S/2)$, will remain unaltered whereas high-frequency out-of-band signals, $[F_S/2, \infty)$, will be significantly suppressed owing to the aliasing spectral copies canceling out each other, as illustrated. Effectively, desired sharp equivalent filters, $G(f)$, can be realized by designing d(t) for given, simple filters, h(t).

The authors have demonstrated that multiplication by d(t) can be effectively achieved with high linearity and low power consumption by employing an LPTV resistor, $R(t) = R(t+T_S)$. The following section briefly describes the application of this LPTV technique to (a) an agile RF front end [4], and (b) a passive spectrum scanner [5].

III. EXAMPLE PRACTICAL LPTV CIRCUITS

A. Agile RF Front End

Fig. 2(a) shows a simplified schematic of an agile RF front end: the LPTV resistor, R(t), connects the input to the virtual ground of an inverter-based integrator, through a passive square wave mixer. Momentarily ignoring the F_O mixer, it is relatively straight forward to observe that the remaining circuit implements a sharp FA-based LPF with $d(t) = \{R_S+R(t)\}^{-1}$ and h(t) being an integrate-and-dump block. The F_O mixer simply translates the LPF to a BPF centered at F_O.

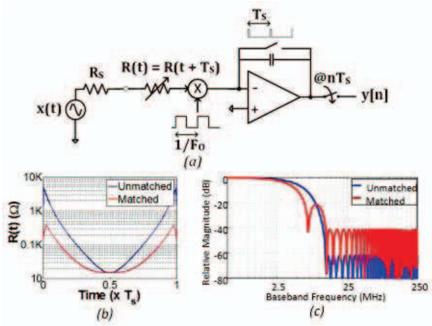

Figure 2: (a) Simplified schematic of BW and center frequency programmable RF front end with best reported close-in blocker tolerance, demonstrated in [4], (b) example R(t) choices and (c) equivalent filter responses without and with the impedance matching constraint.

As described in Section II, sharp equivalent filters can be realized by choosing R(t) appropriately. However, for use directly at the antenna, input impedance match is required. It was shown that S_{11} = mean([R(t)–R_S]/[R(t)+R_S]). Desired maximum S_{11} places a constraint on the optimal choice of R(t). Sharp filters with >40dB stop-band attenuation can be achieved even for S_{11}<–20dB (see Fig. 2(b),(c)). Measurements of a 65nm CMOS prototype [4] demonstrated a receiver with programmable BW and center frequency while achieving >17dBm IIP3 even when the blocker is just 1.25x BW away.

B. Passive Spectrum Scanner

A spectrum scanner can be readily realized using a sharp programmable BPF by sweeping the filter center frequency. To achieve the required high linearity and low power consumption, a purely passive LPTV circuit, shown in Fig. 3(a), was employed [5]. Compared to Fig. 2(a), in the absence of a virtual ground, proper integration is not achieved here.

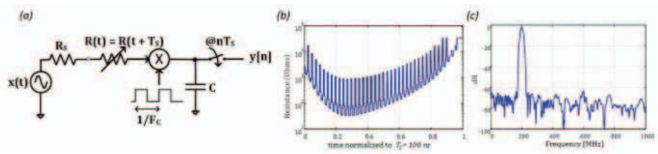

Figure 4: (a) Simplified block diagram of passive spectrum scanner demonstrated in [5] with lowest power consumption and best linearity reported. Example R(t) choice and equivalent filter response ((b) and (c)) are also shown.

However, sharp filtering is still achieved by FA principles since R(t) modulates the current and hence the charge integrated on the capacitor, thereby realizing d(t). This LPTV circuit offers many benefits. Foremost, a passive implementation without amplifiers results in very low power consumption and excellent linearity. In a 65nm prototype where R(t) is realized as a 2GS/s, 9-bit resistor DAC, <8mW and >31dBm IIP3 were demonstrated. Secondly, R(t) is chosen such that the effective impulse response, g(t), includes the sinusoidal carrier, $g(t) = \cos(\omega_c t)g_0(t)$ where $g_0(t)$ is the impulse response of a sharp LPF. Consequently, images at multiples of Fc, in the filter response are suppressed.

IV. IMPLEMENTATION OF LPTV ELEMENTS

As expected, the performance of the LPTV filters depends on errors and parasitic effects in the realization of R(t). It was demonstrated that 10-bit DAC is sufficient for up to 60dB of filter stop band attenuation.

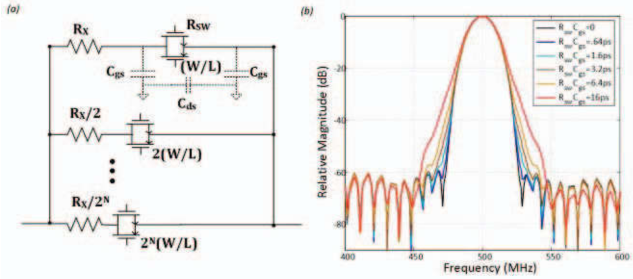

Figure 3: (a) Binary weighted resistor DAC schematic showing example transmission gate switch parasitics. (b) Effect of switch non-idealities (R_{SW}, C_{gs}) on the performance of the filter in Fig. 2(a).

Consider the binary weighted single-ended resistor DAC running at F_{CK} shown in Fig. 4(a). Resistor errors are caused by sizing errors and unequal variation (with PVT) of the value of the poly resistors and the transmission gates R_{ON}. The former errors dominate and can be easily calibrated using DC measurements. The latter can be minimized by setting R_{sw}/R_X=0.2 or less. However, using large transmission gates increases capacitive parasitics, particularly C_{gs}. This limits the speed of the resistor DAC. Note that even though R(t) runs at F_{CK}, actual R(t) is a lower bandwidth signal. However, C_{gs} degrades filter sharpness and stop band attenuation. Example simulated filter responses for the RF front end described in Section II.A are plotted for a range of $R_{sw}C_{gs}$ products to quantify the effect of switch parasitics. Noticeable degradation is observed for $R_{sw}C_{gs}$ > 3ps. Note that $R_{sw}C_{gs}$ gets progressively smaller with CMOS technology scaling.

ACKNOWLEDGMENT

The authors thank Dr. M.C. Chang, TSMC for fabrication.

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