Open-Circuit Submodule Fault Diagnosis in MMCs Using Support Vector Machines

Ardavan Mohammadhassani, *Graduate Student Member, IEEE,* and Ali Mehrizi-Sani, *Senior Member, IEEE*

***Abstract*—Series connection of semiconductor submodules (SM) in a modular multilevel converter (MMC) makes the MMC prone to open-circuit (OC) IGBT failures inside SMs. If left undetected, these faults degrade the operation of the MMC and lead to its instability. This paper proposes a method to detect, localize, and classify single OC SM faults in an MMC using support vector machines (SVM) trained with data obtained from the capacitor voltage balancing block of the MMC control system. The proposed method relies on data extracted from the sorted capacitor voltage arrays of the upper and lower phase arms. Therefore, it does not require extra measurements and hardware. Additionally, it offers a fixed time for detecting and localizing OC SM faults. This method is easy to implement as SVM has a simple decision function. Time-domain simulation case studies are performed on a three-phase nine-level MMC to evaluate the performance of the proposed method.**

***Index Terms*—Fault detection, fault diagnosis, fault location, modular multilevel converters, open-circuit faults, support vector machines.**

I. Introduction

Modular multilevel converters (MMC) are vastly deployed in applications such as HVDC, FACTS, and medium- and high-voltage motor drives [1]–[3]. MMCs comprise of several series-connected semiconductor submodules (SM) in each phase, which fuel their wide adoption by enabling several advantages, including simple scalability, high modularity, and high output voltage quality. However, this also increases the chance of SM switch failures in MMCs. Switch failures disrupt MMC operation, eventually leading to its complete shutdown. In medium- and high-voltage applications, any interruption in the flow of power is critical. Hence, a switch failure detection and localization method is required to activate the protection system of the MMC to ensure its reliable operation [4].

IGBT failures are classified into two types: short-circuit (SC) and open-circuit (OC). SC failures quickly discharge the SM capacitor bank and cause overcurrents that might damage the SM. Protection against SC failures is usually done using the gate drive circuit by turning off the faulty IGBT. OC failures, however, can remain undetected for a longer period of time. They overcharge the SM capacitor bank and cause distortion in the output voltage waveform. They can also create consecutive OC failures and eventually make the MMC unstable. Thus, the main focus of this paper is to detect, localize, and classify OC SM faults. [5] Various methods are proposed in the literature to detect OC SM faults in MMCs [6]–[15]. These methods can be divided into two groups: hardware-based methods and software-based methods. Hardware-based methods are simple and reliable, but add extra devices and circuitry to the basic MMC design and significantly increase its cost, volume, and complexity. Moreover, they are not suitable for existing systems. Software-based methods, however, do not require any extra devices for OC SM fault diagnosis. Sliding-mode observer is designed in [9] to detect and localize OC SM faults in MMCs. However, it has several drawbacks:

1) They rely on the precise switching model of each SM, which significantly increases their computational burden when the number of SMs is high;
2) They localize the fault when an SM capacitor voltage is higher than the healthy ones, which significantly increases their detection time as it takes several fundamental cycles for the capacitor voltage to increase appreciably;
3) Accurate observer design requires a precise mathematical model of the system. The mathematical model of the MMC is high-order, nonlinear, and highly coupled. Thus, observer design for MMCs can become very complicated.

Kalman filter is utilized in [16] to detect and localize OC SM faults. However, this method has drawbacks as well:

1) Its robustness and accuracy could be put in jeopardy due to long delay between detection and localization;
2) Unless the prediction stage is accurate enough, the capacitor voltage estimation results can be poor.

Besides the shortcomings mentioned above, sliding-mode observer-based methods and Kalman filter-based methods also have some drawbacks in common:

1) They both may become ineffective under nearest-level modulation;
2) Neither method can classify the fault type;
3) Choosing the empirical threshold for these methods can be difficult under different MMC voltage or power ratings.

Utilizing state observers for OC SM fault diagnosis is proposed in [8]. However, it has a long detection time of 50–150 ms, and it is vulnerable to parameter uncertainties. A variance-based statistical method is proposed in [10] to diagnose OC SM faults in MMCs. However, it relies on empirical thresholds, which increase its detection time. Artificial neural networks (ANN) are used in [14] to only classify the OC SM fault. Support vector machine (SVM) is used in [15] to only detect and localize single OC SM faults under double switch failures. Moreover, its training dataset is small, which can affect its accuracy for acting on new data.

This paper proposes a new method to detect, localize, and classify OC SM faults in MMCs. During OC SM faults, the sorting algorithm of the capacitor voltage balancing block

A. Mohammadhassani and A. Mehrizi-Sani are with the Bradley Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg VA 24061 USA (e-mails: ardavanmh93@vt.edu, mehrizi@vt.edu).

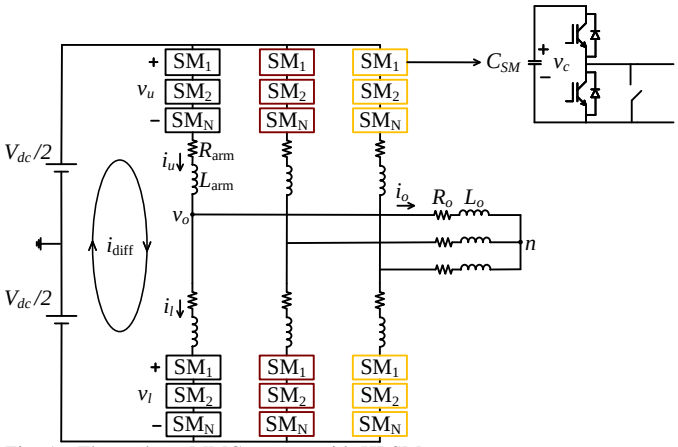

Fig. 1. Three-phase MMC system with HBSMs.

always puts the capacitor voltages of the faulty SMs at the beginning or at the end of the sorted array, depending on arm current direction. Thus, by counting the number of times each SM appears at the beginning of the sorted array when arm current is negative and at the end of the sorted array when arm current is positive, a dataset can be constructed to train a two-class SVM for each SM to detect and localize the OC SM fault. Simultaneously, the sum of the number of times each SM appears at the beginning of the sorted array when arm current is positive and at the end of the sorted array when arm current is negative is used to create a dataset to train a multiclass SVM for each SM to classify the OC SM fault. This method has a fixed detection, localization, and classification time of one fundamental period. Additionally, it does not require any extra hardware and is very simple to implement. Time-domain simulation case studies on a detailed switching model of a three-phase nine-level MMC system in PSCAD/EMTDC software evaluate the performance of the proposed method.

The specific contributions of this paper are

- Statistical analysis of capacitor voltage balancing response to OC SM faults.
- Design of an SVM-based OC SM fault detection and localization method.
- Design of an SVM-based OC SM fault classification method.

The rest of this paper is structured as follows. Section II presents the basics of operation of MMC. Section III discusses the three types of OC SM faults and their effects on MMC operation. The proposed OC SM fault diagnosis method is presented in Section IV. Performance evaluation of the proposed method is presented in Section V. Finally, conclusions are presented in Section VI.

II. Basics of Operation of MMC

Fig. 1 shows the main circuit design of a three-phase MMC with half-bridge SMs (HBSM). It consists of three legs, each comprising of two arms with N HBSMs in each arm. The sum of the HBSM output voltages of each phase can be modeled as controlled voltage sources, denoted by v_{ui} and v_{li}, respectively, as

$$\begin{aligned} v_{ui} &= \sum_{j=1}^{N} n^i_{uj} v^i_{cuj} \\ v_{li} &= \sum_{j=1}^{N} n^i_{lj} v^i_{clj} \\ n^i{}_{uj}, n^i_{lj} &\in \{0,1\} \\ i &= a,b,c, \end{aligned} \tag{1}$$

where n^i_{uj} and n^i_{lj} are the switching states of the jth HBSM, and v^i_{cuj} and v^i_{clj} are the capacitor voltages of the jth HBSM in the upper and lower arms of phase i. In the steady-state, the capacitor voltages are balanced. Thus, v^i_{cuj} and v^i_{clj} are equal to V^Σ_{cui}/N and V^Σ_{cli}/N, respectively, where V^Σ_{cui} and V^Σ_{cli} are the sum of the HBSM capacitor voltages. Using this, (1) can be rewritten as

$$\begin{aligned} v_{ui} &= \frac{V^\Sigma_{cui}}{N} \sum_{j=1}^{N} n^i_{uj} = N_{ui} V^\Sigma_{cui} \\ v_{li} &= \frac{V^\Sigma_{cli}}{N} \sum_{j=1}^{N} n^i_{lj} = N_{li} V^\Sigma_{cli} \\ N_{ui}, N_{li} &\in \left\{0, \frac{1}{N}, \frac{2}{N}, \ldots, 1\right\} \\ i &= a,b,c, \end{aligned} \tag{2}$$

where N_{ui} and N_{li} are insertion indices of phase i. The circulating current $i_{\text{diff}i}$ and the output current i_{oi} are defined as

$$\begin{aligned} i_{\text{diff}i} &= \frac{i_{ui} + i_{li}}{2} \\ i_{oi} &= i_{ui} - i_{li} \\ i &= a,b,c, \end{aligned} \tag{3}$$

where i_{ui} and i_{li} are the arm currents. Using KCL, the dynamic equation for the sum of the HBSM capacitor voltages in the upper and lower arms is found as

$$\begin{aligned} \frac{dV^\Sigma_{cui}}{dt} &= \frac{N N_{ui}}{C_{\text{SM}}} i_{ui} \\ \frac{dV^\Sigma_{cli}}{dt} &= \frac{N N_{li}}{C_{\text{SM}}} i_{li} \\ i &= a,b,c, \end{aligned} \tag{4}$$

where C_{SM} is the capacitance of each HBSM. The dynamic equation for i_{oi} is defined using KVL as

$$\frac{di_{oi}}{dt} = \frac{1}{L_{\text{arm}} + 2L_{\text{o}}} (v_{li} - v_{ui}) - \frac{R_{\text{arm}} + 2R_{\text{o}}}{L_{\text{arm}} + 2L_{\text{o}}} i_{oi}, \tag{5}$$

where R_{arm} is the arm resistance, R_{o} is the load resistance, L_{arm} is the arm inductance, and L_{o} is the load inductance. Using KVL, the dynamic equation for $i_{\text{diff}i}$ is found as

$$\frac{di_{\text{diff}i}}{dt} = \frac{1}{2L_{\text{arm}}} (V_{dc} - v_{ui} - v_{li}) - \frac{R_{\text{arm}}}{L_{\text{arm}}} i_{\text{diff}i}, \tag{6}$$

where V_{dc} is the input DC voltage.

III. MMC Operation under OC SM Faults

Fig. 2 shows the three types of OC SM faults depending on the failed IGBT: OC failure in the upper IGBT (S_u), OC failure in the lower IGBT (S_l), and OC failure in both IGBTs

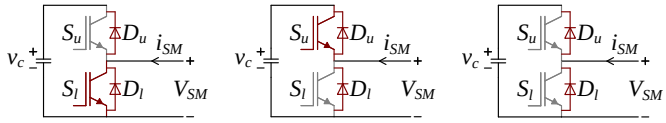

Fig. 2. OC SM fault cases in MMCs with HBSMs: (a) S_u OC failure, (b) S_l OC failure, and (c) simultaneous S_u and S_l OC failures.

TABLE I
EFFECTS OF S_u OC FAILURE ON MMC OPERATION

SM Current i_{SM}	**Voltage Response**	
	Normal Operation	S_u OC Failure
Positive	Charging (Insert) Unchanged (Bypass)	Charging (Insert) Unchanged (Bypass)
Negative	Discharging (Insert) Unchanged (Bypass)	Unchanged (Insert) Unchanged (Bypass)

TABLE II
EFFECTS OF S_l OC FAILURE ON MMC OPERATION

SM Current i_{SM}	**Voltage Response**	
	Normal Operation	S_l OC Failure
Positive	Charging (Insert) Unchanged (Bypass)	Charging (Insert) Charging (Bypass)
Negative	Discharging (Insert) Unchanged (Insert)	Discharging (Insert) Unchanged (Insert)

TABLE III
EFFECTS OF SIMULTANEOUS S_u AND S_l OC FAILURES ON MMC OPERATION

SM Current i_{SM}	**Voltage Response**	
	Normal Operation	S_u&S_l OC Failure
Positive	Charging (Insert) Unchanged (Bypass)	Charging (Insert) Charging (Bypass)
Negative	Discharging (Insert) Unchanged (Bypass)	Unchanged (Insert) Unchanged (Bypass)

(S_u and S_l). The MMC has a different response to each OC IGBT failure case. Therefore, MMC operation is analyzed for each case according to the reference SM current direction depicted in Fig. 2.

A. S_u OC Fault

Table I summarizes the effects of S_u OC failure on MMC operation. If i_{SM} is positive, S_u OC failure does not affect MMC operation, as the current passes through D_u and C_{SM}. However, if i_{SM} is negative, the current flows only through D_l and the HBSM capacitor loses its ability to discharge.

B. S_l OC Failure

Table II summarizes the effects of MMC operation under S_l OC failure. In this case, MMC operation is unaffected if i_{SM} is negative. Therefore, the HBSM capacitor keeps its ability to discharge. However, when the i_{SM} is positive, the HBSM current flows via D_u and C_{SM}. Therefore, the HBSM capacitor does not get bypassed and keeps charging.

C. Simultaneous S_u and S_l OC Failures

Table III summarizes the effects of simultaneous S_u and S_l OC failures on MMC operation. In this case, the MMC operation is affected for both current directions. When i_{SM} is positive, the HBSM does not get bypassed and the HBSM capacitor keeps charging through D_u. When i_{SM} is negative, the HBSM gets bypassed via D_l and does not discharge. Therefore, the HBSM capacitor keeps charging with a rate higher than the other two scenarios.

IV. PROPOSED OC SM FAULT DIAGNOSIS METHOD

A. Capacitor Voltage Balancing During OC SM Failures

Capacitor voltage balancing is an essential block of the MMC control system. This block makes sure that the charge and discharge rates of SM capacitor voltages in each phase arm are equal, so that the MMC can properly accomplish its control objectives. The capacitor voltage balancing block measures the capacitor voltages in each phase arm, sorts them according to arm current direction, and finally inserts or bypasses SMs according to N_{ui} and N_{li}. The capacitor voltage balancing algorithm used in this paper is summarized as below:

1) If arm current is positive, capacitors need to be charged. Thus, the capacitor voltages are sorted in ascending order and capacitors with lower voltages are inserted.
2) If arm current is negative, capacitors need to be discharged. Thus, the capacitor voltages are sorted in descending order and capacitors with higher voltages are inserted.

The sum of the number of times the ith capacitor voltage appears in the first slot of the sorting array during negative arm current and in the last slot during positive arm current $N_{\text{sum},i}^{\text{discharge}}$ for one fundamental period T_o shows how severely the capacitor voltage balancing algorithm wants to discharge that capacitor. Ideally, $N_{\text{sum},i}^{\text{discharge}}$ has an integer value, which is calculated using

$$N_{\text{sum},i}^{\text{discharge}} = \frac{T_o}{NT_{\text{SW}}}, \tag{7}$$

where T_{SW} is the switching period and N is the number of SMs in one arm. However, this does not hold true in practice as N and T_{SW} are designed according to different rules. Therefore, $N_{\text{sum},i}^{\text{discharge}}$ becomes a random variable with a mean of

$$\mu = \frac{T_o}{NT_{\text{SW}}}. \tag{8}$$

Using l samples of $N_{\text{sum},i}^{\text{discharge}}$, the standard deviation σ of $N_{\text{sum},i}^{\text{discharge}}$ is

$$\sigma = \sqrt{\frac{1}{l}\sum_{j=1}^{l}\left(N_{\text{sum},i,j}^{\text{discharge}} - \mu\right)^2}. \tag{9}$$

Using (8) and (9), a Gaussian distribution $f\left(N_{\text{sum},i}^{\text{discharge}}\right)$ can be fit to $N_{\text{sum},i}^{\text{discharge}}$ as

$$f\left(N_{\text{sum},i}^{\text{discharge}}\right) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{N_{\text{sum},i}^{\text{discharge}} - \mu}{\sigma}\right)^2}. \tag{10}$$

The probability of $N_{\text{sum},i}^{\text{discharge}}$ falling between a and b is found

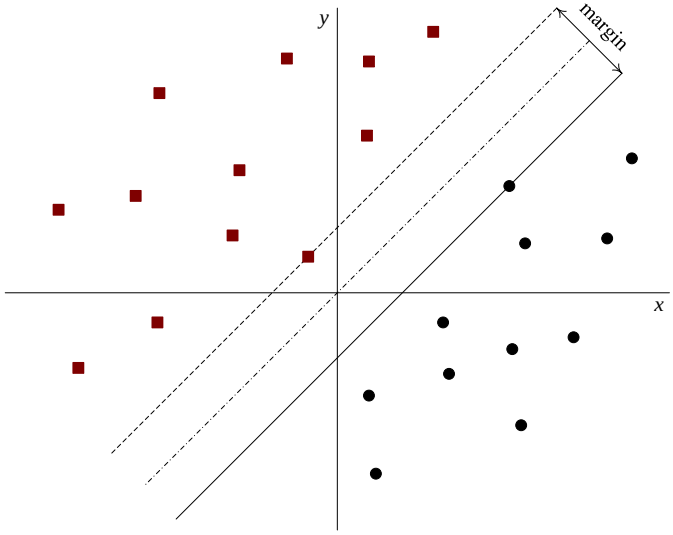

Fig. 3. Proposed SVM-based OC SM fault diagnosis method.

by calculating the area under the curve in (10) using

$$P[a \leq N_{\text{sum},i}^{\text{discharge}} \leq b] = \int_a^b f\left(N_{\text{sum},i}^{\text{discharge}}\right) dN_{\text{sum},i}^{\text{discharge}}. \quad (11)$$

$N_{\text{sum},i}^{\text{discharge}}$ can be used to detect and localize OC SM faults. Around 99.7% of the area under the curve in (10) is covered by values between $\mu-2\sigma$ and $\mu+2\sigma$. That is, it is most likely that $N_{\text{sum},i}^{\text{discharge}}$ will fall within this range during normal operation of the MMC. On the other hand, during OC SM faults, the capacitor voltage of the faulty SM increases beyond that of the remaining healthy SMs. This means that the capacitor voltage balancing algorithm keeps trying to discharge it and always puts it either in the first slot or the last slot of the sorting array. Hence, its $N_{\text{sum},i}^{\text{discharge}}$ increases at the onset of an OC SM fault and finally saturates at T_o/T_{SW}. Equation (10) shows that when $N_{\text{sum},i}^{\text{discharge}}$ increases, its probability of falling within normal range decreases and eventually becomes zero. This shows that $N_{\text{sum},i}^{\text{discharge}}$ can be used to detect and localize OC SM faults.

Analogous to $N_{\text{sum},i}^{\text{discharge}}$, the sum of the number of times the ith capacitor voltage appears in the first slot of the sorting array during negative arm current and in the last slot during positive arm current $N_{\text{sum},i}^{\text{charge}}$ for one fundamental period T_o shows how severely the capacitor voltage balancing algorithm needs to charge that capacitor. $N_{\text{sum},i}^{\text{charge}}$ can be used to distinguish between the three types of OC SM faults. The capacitor voltage of the faulty SM increases with a different rate of change under each type of fault. Therefore, its $N_{\text{sum},i}^{\text{charge}}$ decreases to zero with a different rate of change under each type of fault. The capacitor voltages of the remaining healthy SMs respond differently to the three types of OC SM faults. Thus, $N_{\text{sum},i}^{\text{charge}}$ values of the SMs are different under each type of fault and they can be used to distinguish between OC SM fault.

B. OC SM Fault Diagnosis Using SVM

Statistical methods such as the method proposed in [10] can be used to set empirical thresholds for $N_{\text{sum},i}^{\text{discharge}}$ and $N_{\text{sum},i}^{\text{charge}}$ to distinguish between normal and abnormal operations and classify the OC SM fault type. However, given that $N_{\text{sum},i}^{\text{discharge}}$ and $N_{\text{sum},i}^{\text{charge}}$ are random variables, finding the threshold to optimize the diagnosis time becomes a daunting task. Interestingly, OC SM fault diagnosis can be solved as a classification problem in the realm of machine learning. Classification refers to a problem where a class label is predicted for a sample input data. An established classification method is the support vector machine (SVM) [17]. SVM eliminates the need for setting empirical thresholds. Therefore, it is a viable and better solution to the problem of OC SM fault diagnosis. SVM separates two classes via finding an optimal hyperplane in a multidimensional space. For linearly-separable datasets, the optimal hyperplane that separates the two classes with target labels $t_i = \pm 1$ is defined as

$$y(x) = w^T \phi(x) + b, \quad (12)$$

where $y(x)$ is the score, w is the vector containing the weight factors, $\phi(x)$ is a feature-space transformation, and b is the bias. In a two-dimensional input space, $y(x)$ becomes a straight line, such the one shown in Fig. 3. If $y(x) > 0$, the label $+1$ is predicted; otherwise, the label -1 is predicted. The objective of SVM is to maximize the margin ρ between selected support vectors of the two classes or minimize $\|w\|$ by solving

$$\begin{aligned} &\min_w \ \frac{1}{2}||w||^2 + C\sum_{i=1}^{n}\zeta_i \\ &\text{subject to } \ t_i\left(w \cdot x_i + b\right) \geq 1 - \zeta_i, \ \ \zeta_i \geq 0 \ \ \forall i, \end{aligned} \quad (13)$$

where C is a cost parameter, n is the length of the training dataset, and ζ_i is the penalty assigned for the ith nonseparable feature vector. This problem is usually simplified into its dual form and easily solved by quadratic programming:

$$\begin{aligned} &\max \ L_D = \sum_i \alpha_i - \frac{1}{2}\sum_{i,j}\alpha_i\alpha_j y_i y_j x_i^T x_j \\ &\text{subject to } \ 0 \leq \alpha_i \leq C \ \ \forall i, \ \ \sum_i \alpha_i y_i = 0, \end{aligned} \quad (14)$$

where α is a Lagrangian multiplier. To improve classification for nonseparable datasets, a kernel function $K(x_i, x_j) = \phi(x_i)^T\phi(x_j)$ is used. Kernels are mathematical functions that are used to convert linearly inseparable input datasets to linearly separable ones by converting the input dataset to one with higher dimensions. Three major types of kernel functions are the linear kernel $K(x_i, x_j) = {x_i}^T x_j$, the polynomial kernel $K\left(x_i, x_j\right) = \left(\gamma\left(x_i \cdot x_j\right) + r\right)^d$, and the Gaussian kernel $K\left(x_i, x_j\right) = \exp\left(-\gamma||x_i - x_j||^2\right)$. After the proper kernel is selected, the optimal hyperplane in (12) becomes

$$y\left(x\right) = \text{sign}\left(\sum_{i=1}^{n}\alpha_i t_i K\left(x, x_i\right) + b\right), \quad (15)$$

where b is calculated by solving $\alpha_i\left(t_i\left(w \cdot x_i + b\right) - 1\right) = 0, i = 1, \ldots, n$, such that α_i is not zero.

Two SVMs are trained for each SM: one for detection and localization of OC SM faults and another for classifying the fault type. The feature samples for the detection and localization SVM of one SM consist of $N_{\text{sum},i}^{\text{discharge}}$ data from all SMs in the same arm obtained by applying all three types of OC SM faults on that particular SM. In this way, the SVM detects and localizes the OC SM fault simultaneously

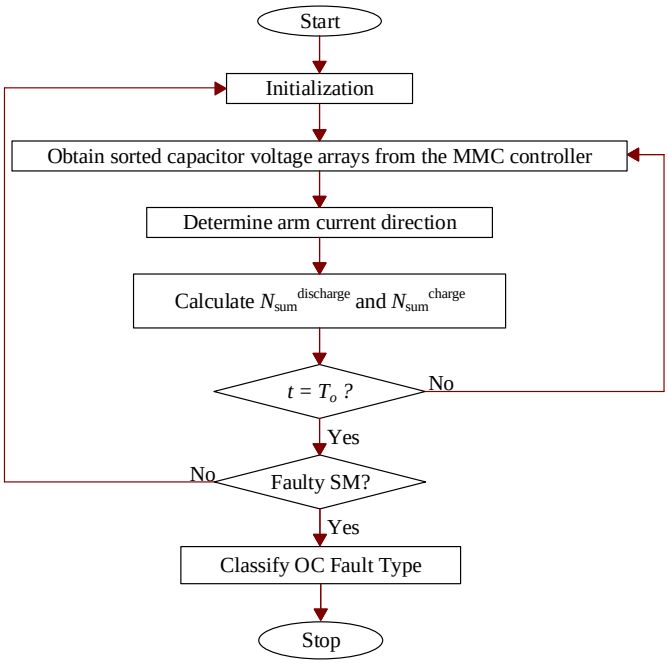

Fig. 4. Proposed SVM-based OC SM fault diagnosis method.

in T_o seconds. The `fitcsvm` function in MATLAB is used to train the detection and localization SVM. The Gaussian kernel is selected for this purpose due to its ability to classify highly nonseparable datasets. To classify the OC SM fault type, a multiclass SVM is trained for each SM using the $N_{\text{sum},i}^{\text{charge}}$ data from all SMs in the same arm as feature samples obtained by applying all three types of OC SM faults on that particular SM. Afterwards, the `fitcecoc` function in MATLAB is used to train the OC fault classification SVM using the Gaussian kernel. Solving classification problems with multiple classes is not inherently supported by SVM. Therefore, various coding designs are available to break down the multiclass classification problem into multiple two-class ones. The *one-versus-one* method is used in this paper as the coding design. This method splits a multiclass classification problem into multiple two-class classification problems. The multiclass dataset is split into one dataset for each class against every other class and the class with the majority of votes is predicted as the class label.

Fig. 4 summarizes the proposed SVM-based OC SM fault diagnosis method:

1) Initialize timer, $N_{\text{sum},i}^{\text{discharge}}$, and $N_{\text{sum},i}^{\text{charge}}$.
2) Obtain the sorted capacitor voltage arrays from the MMC controller.
3) Determine arm current direction.
4) Calculate $N_{\text{sum},i}^{\text{discharge}}$ and $N_{\text{sum},i}^{\text{charge}}$ for each SM according to arm current direction.
5) If timer has reached T_o, pass $N_{\text{sum},i}^{\text{discharge}}$ of all SMs to each detection and localization SVM. Otherwise, go to step two.
6) If a fault is detected, pass $N_{\text{sum},i}^{\text{charge}}$ of all SMs to the fault classification SVM of the faulty SM to classify fault type.

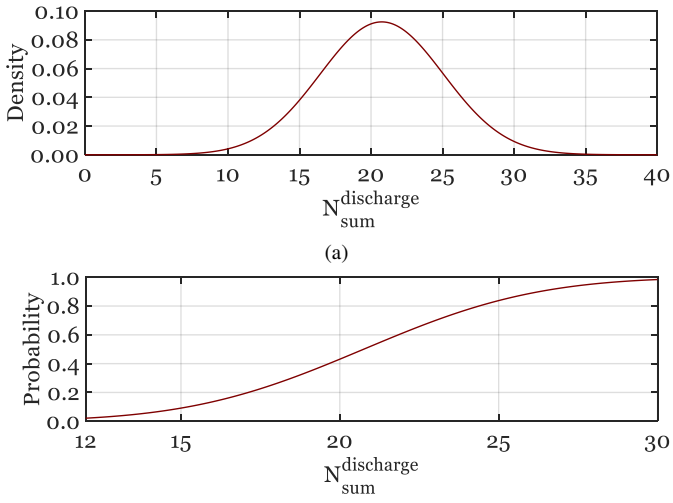

Fig. 5. Characteristics of $N_{\text{sum}}^{\text{discharge}}$ during normal operation: (a) Normal distribution of $N_{\text{sum}}^{\text{discharge}}$ and (b) cumulative distribution function of $N_{\text{sum}}^{\text{discharge}}$.

TABLE IV
SIMULATION PARAMETERS

Parameter	Value
Number of SMs in each phase arm N	4
DC-link voltage V_{dc}	10 kV
SM capacitance C_{SM}	4600 μF
Arm inductance L_{arm}	9 mH
Load resistance R_o	12 Ω
Load inductance L_o	4 mH
Fundamental frequency f_o	60 Hz
Modulation index m_a	0.8
MPC Sampling frequency f_s	5 kHz
Rated V_c for normal operation	2.5 kV

V. PERFORMANCE EVALUATION

A. Training Data Acquisition and Statistical Analysis

A detailed switching model of a three-phase nine-level MMC with $N = 4$ is built in PSCAD/EMTDC to simulate all types of OC SM faults on each SM to obtain training data for each SVM. Simulation parameters are described in Table IV. The MPC controller proposed in [4] is used in this paper. The OC SM fault should be diagnosed in less than 100 ms to avoid subsequent damage to other devices [9]. Therefore, 20 fundamental cycles worth of training data is extracted from the simulation, of which 10 fundamental cycles belong to normal operation and 10 fundamental cycles belong to abnormal operation. Each type of fault is simulated at ten different time instances to create a diverse training dataset for each SM. Training dataset for detection and localization SVM of one SM consists of $N_{\text{sum},i}^{\text{discharge}}$ for all four SMs in one arm under each type of fault. Therefore, the size of the feature matrix is 600×4 for each SM. The training dataset for the fault type classification SVM of one SM consists of $N_{\text{sum},i}^{\text{discharge}}$ for all four SMs in one arm under each type of fault. To increase the accuracy of the fault type classification SVM, the variance and Euclidean norm of each feature sample is also added to the feature matrix of each SM. Thus, the feature matrix grows to have a size of 600×6 for each SM. Fig. 5(a) shows the normal distribution of $N_{\text{sum}}^{\text{discharge}}$ during normal operation.

$N_{\text{sum}}^{\text{discharge}}$ is dispersed around $\mu = 20.75$ with a standard deviation of $\sigma = 4.31$. Around 99.7% of the area under the curve in Fig. 5(a) is covered by values between $\mu - 2\sigma \approx 12$ and $\mu + 2\sigma \approx 30$. Therefore, the cumulative distribution function (CDF) of $N_{\text{sum}}^{\text{discharge}}$ during normal operation, also shown in Fig. 5(b), is found by calculating the area under the curve for $12 \leq N_{\text{sum}}^{\text{discharge}} \leq 30$. Fig. 5(b) shows that $P\left(N_{\text{sum}}^{\text{discharge}} \leq 12\right) \approx 2\%$ and $P\left(N_{\text{sum}}^{\text{discharge}} \leq 30\right) \approx 98\%$, meaning that $P\left(12 \leq N_{\text{sum}}^{\text{discharge}} \leq 30\right) \approx 96\%$. Therefore, it is highly probable that $N_{\text{sum}}^{\text{discharge}}$ falls within this range during normal MMC operation.

B. Case 1: S_u Fault in SM_{u1a}

To evaluate the performance of the proposed OC SM fault diagnosis method on new data, an OC fault is applied to the top switch in SM_1 in the upper arm of phase a at $t = 100$ ms. Fig. 6(a) shows $vcua$. Prior to $t = 100$ ms, the capacitor voltages are balanced at 2.5 kV each. After $t = 100$ ms, the capacitor voltages start to increase, as described in Table I. Fig. 6(b) shows $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a at each fundamental period cycle during simulation. Fig. 6(b) shows that before $t = 100$ ms, or the 6th fundamental period cycle, $N_{\text{sum}}^{\text{discharge}}$ for all SMs is between 10 and 30, which complies with the statistical analysis presented in Section V-A. Fig. 6(b) also shows that $N_{\text{sum}}^{\text{discharge}}$ values remain in the same range for up to two fundamental period cycles after $t = 100$ ms. After that, $N_{\text{sum}}^{\text{discharge}}$ starts to increase drastically for SM_{u1a} and decrease significantly for the other SMs. Fig. 6(c) shows that SVM detects and localizes the OC SM fault in one fundamental period cycle, or 16.67 ms. Fig. 6(d) shows $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a. Similar to $N_{\text{sum}}^{\text{discharge}}$, $N_{\text{sum}}^{\text{charge}}$ remains close to its prefault values for two fundamental period cycles after the fault. Afterwards, $N_{\text{sum}}^{\text{charge}}$ for SM_{u1a} drastically decreases, while others increase. Fig. 6(e) shows that SVM predicts the correct type of fault in one fundamental period cycle or 16.67 ms.

C. Case 2: S_l Fault in SM_{u1a}

Fig. 7(a) shows $vcua$. Prior to $t = 100$ ms, capacitor voltages are balanced at 2.5 kV each. At $t = 100$ ms, a S_l fault occurs in SM_{u1a} and its capacitor voltage starts to increase, while other capacitor voltages start to decrease. Fig. 7(b) shows $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a. Prior to $t = 100$ ms, or the 6th fundamental cycle, $N_{\text{sum}}^{\text{discharge}}$ varies between 10 and 30, which complies with the analysis presented in Section V-A. This figure also shows that $N_{\text{sum}}^{\text{discharge}}$ values remain in the same range for up to two fundamental period cycles after $t = 100$ ms. After that, $N_{\text{sum}}^{\text{discharge}}$ starts to increase drastically for SM_{u1a} and decrease significantly for other SMs. Fig. 7(c) shows that SVM is able to detect and localize the fault in 16.67 ms. Fig. 7(d) shows $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a. Similar to $N_{\text{sum}}^{\text{discharge}}$, $N_{\text{sum}}^{\text{charge}}$ remains close to its prefault values for two fundamental period cycles after the fault. Afterwards, $N_{\text{sum}}^{\text{charge}}$ for SM_{u1a} drastically decreases while others increase. Fig. 7(e) shows that SVM predicts the correct type of fault in one fundamental period cycle or 16.67 ms.

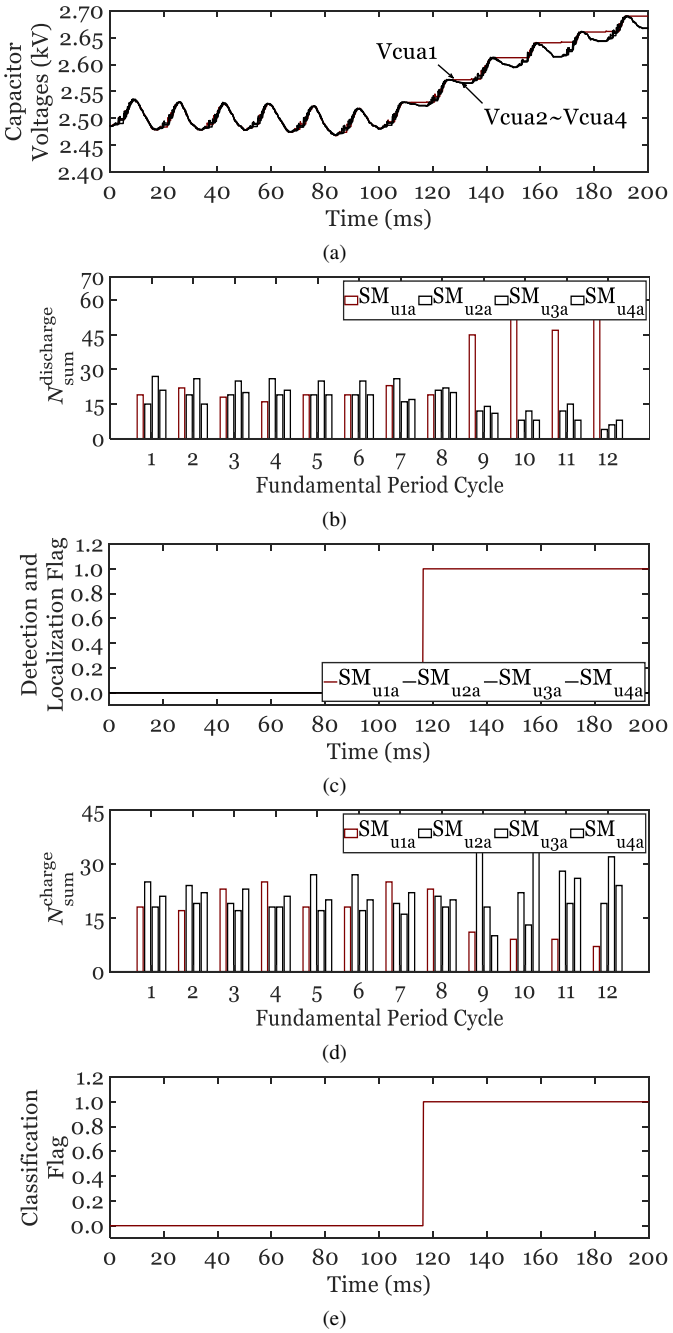

Fig. 6. Simulation results after applying a S_u fault in SM_{u1a}: (a) capacitor voltages of SMs in the upper arm of phase a, (b) $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a, (c) detection and localization flag for SMs in the upper arm of phase a, (d) $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a, and (e) classification flag for SM_{u1a}.

D. Case 3: Simultaneous S_u and S_l Faults in SM_{u1a}

Fig. 8(a) shows $vcua$. Prior to $t = 100$ ms, the capacitor voltages are balanced at 2.5 kV each. At $t = 100$ ms, simultaneous S_u and S_l faults occur in SM_{u1a}. Fig. 8(a) shows that v_{cu1a} immediately starts to increase at the onset of the fault, while getting bypassed intermittently, and others decrease. Fig. 8(b) shows $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a. Prior to $t = 100$ ms, or the 6th fundamental cycle, $N_{\text{sum}}^{\text{discharge}}$ varies between 10 and 30, which complies with the analysis presented in Section V-A. This figure also shows that $N_{\text{sum}}^{\text{discharge}}$ values remain in the same range for up

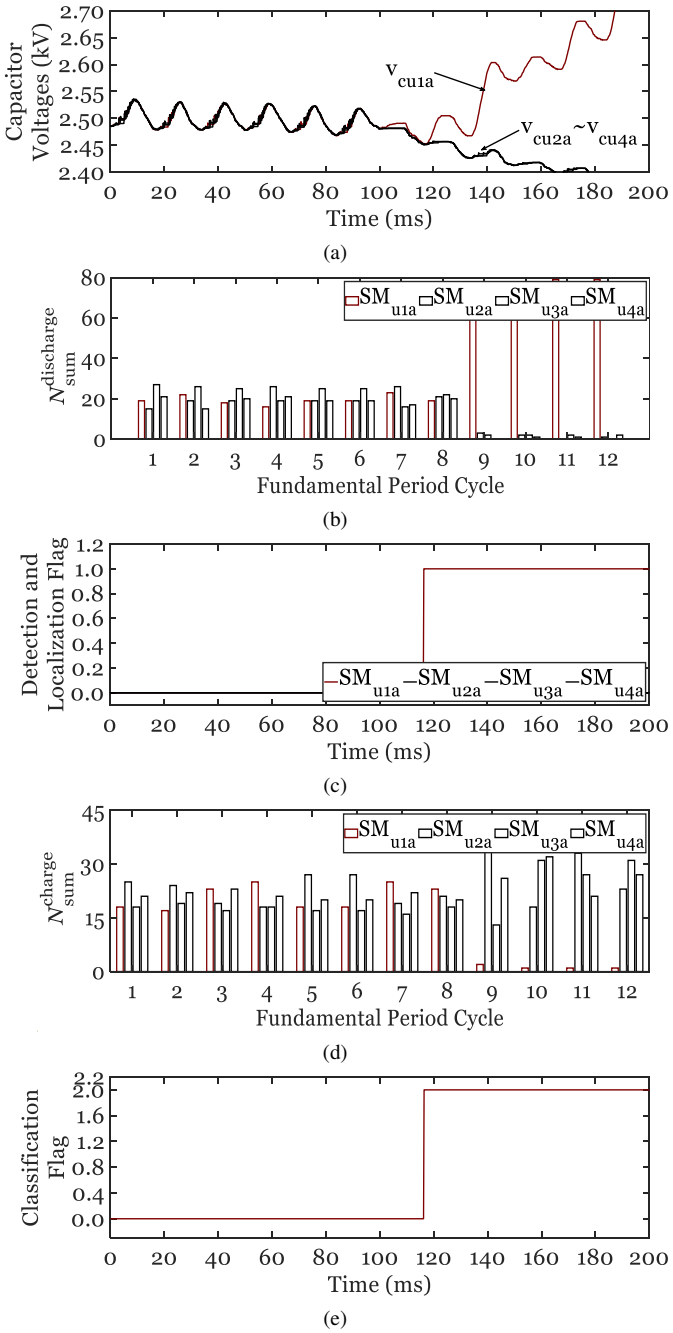

Fig. 7. Simulation results after applying a S_l fault in SM_{u1a}: (a) capacitor voltages of SMs in the upper arm of phase a, (b) $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a, (c) detection and localization flag for SMs in the upper arm of phase a, (d) $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a, and (e) classification flag for SM_{u1a}.

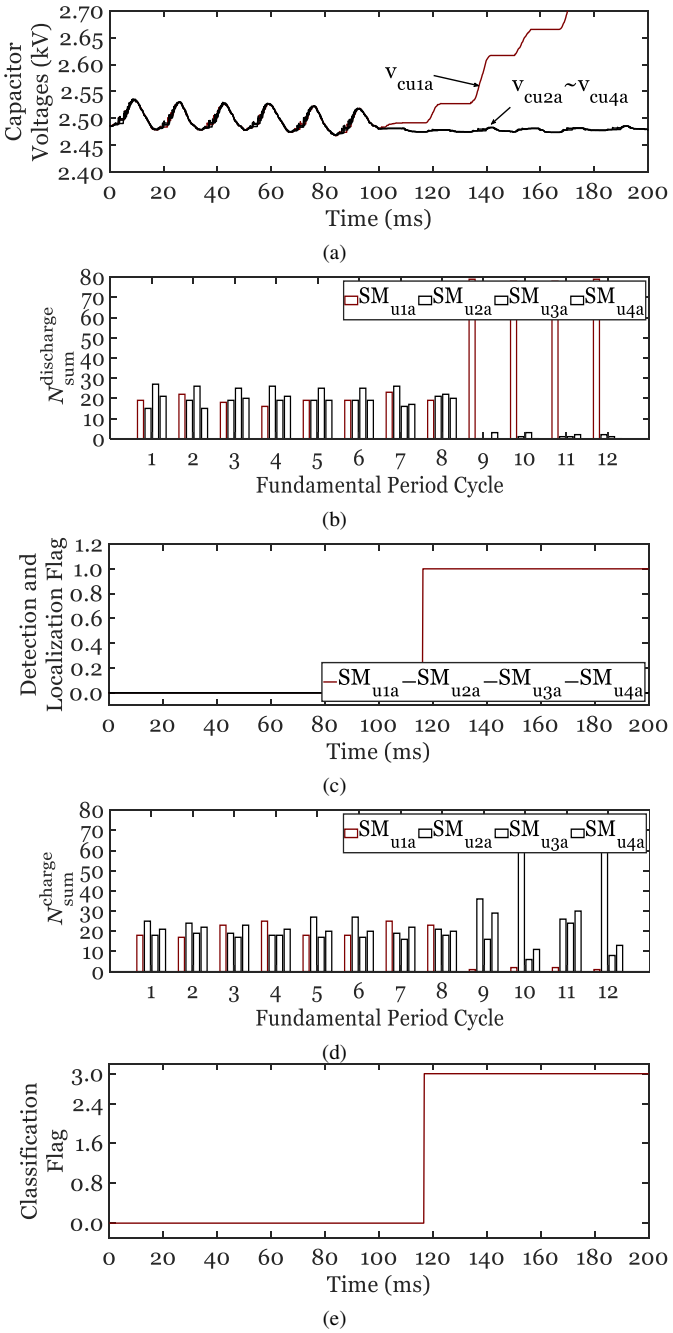

Fig. 8. Simulation results after applying simultaneous S_u and S_l faults in SM_{u1a}: (a) capacitor voltages of SMs in the upper arm of phase a, (b) $N_{\text{sum}}^{\text{discharge}}$ for SMs in the upper arm of phase a, (c) detection and localization flag for SMs in the upper arm of phase a, (d) $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a, and (e) classification flag for SM_{u1a}.

to two fundamental period cycles after $t = 100$ ms. After that, $N_{\text{sum}}^{\text{discharge}}$ starts to increase drastically for SM_{u1a} and decrease significantly for other SMs. Fig. 8(c) shows that SVM is able to detect and localize the fault in 16.67 ms. Fig. 8(d) shows $N_{\text{sum}}^{\text{charge}}$ for SMs in the upper arm of phase a. Similar to $N_{\text{sum}}^{\text{discharge}}$, $N_{\text{sum}}^{\text{charge}}$ remains close to its prefault values for two fundamental period cycles after the fault. Afterwards, $N_{\text{sum}}^{\text{charge}}$ for SM_{u1a} starts to drastically decrease while it increases for other SMs. Fig. 8(e) shows that SVM predicts the correct type of fault in 16.67 ms.

VI. Conclusions

This paper proposes a method to detect, localize, and classify single OC SM faults in MMCs. This method counts the number of times each capacitor voltage appears in the first and last slots of the sorting array and then uses two SVMs to diagnose the OC SM fault. Since the sorted arrays are already available in the MMC controller, this method does not require new measurements or extra hardware. Moreover, it has a simple implementation. It detects, localizes, and classifies the OC SM fault in only one fundamental cycle (16.67 ms for a 60 Hz fundamental frequency), regardless of the time

of fault occurrence. The proposed method is evaluated using time-domain simulation case studies on a three-phase nine-level MMC in PSCAD/EMTDC. Simulation results confirm the merits of the proposed method.

REFERENCES

[1] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[2] S. Ziaeinejad, Y. Sangsefidi, and A. Mehrizi-Sani, "A generalized switching strategy and capacitor sizing algorithm for granular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4443–4453, Jun. 2018.

[3] S. Ziaeinejad and A. Mehrizi-Sani, "PWM A-CHB converter based on trinary multilevel converter: Topology, switching algorithm, and stability analysis," *IEEE Trans. Ind. Electron.*, vol. 66, no. 6, pp. 4166–4176, Jun. 2019.

[4] A. Mohammadhassani and A. Mehrizi-Sani, "A fault tolerant selective harmonic elimination method for modular multilevel converters," *IEEE Power Energy Soc. General Meeting*, Aug. 2020.

[5] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, no. 1, pp. 96–107, Jan. 2013.

[6] J. Zhang, X. Hu, S. Xu, Y. Zhang, and Z. Chen, "Fault diagnosis and monitoring of modular multilevel converter with fast response of voltage sensors," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 5071–5080, Jun. 2020.

[7] J. Wang, H. Ma, and Z. Bai, "A submodule fault ride-through strategy for modular multilevel converters with nearest level modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1597–1608, Feb. 2018.

[8] B. Li, Y. Zhang, R. Yang, G. Wang, and D. Xu, "An IGBT open-circuit fault detection method for modular multilevel converters," *2015 Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia)*, pp. 1573–1578, Jun. 2015.

[9] S. Shao, A. J. Watson, J. C. Clare, and P. W. Wheeler, "Robustness analysis and experimental validation of a fault detection and isolation method for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3794–3805, May 2016.

[10] H. Yang, W. Zhou, J. Sheng, H. Luo, C. Li, W. Li, and X. He, "A statistical submodule open-circuit failure diagnosis method for modular multilevel converters (MMCs) with variance measurement," *IEEE Open J. Power Electron.*, vol. 1, pp. 180–189, May 2020.

[11] Z. Geng, M. Han, Z. W. Khan, and X. Zhang, "Detection and localization strategy for switch open-circuit fault in modular multilevel converters," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2630–2640, Dec. 2020.

[12] Z. Wang and L. Peng, "Grouping capacitor voltage estimation and fault diagnosis with capacitance self-updating in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1532–1543, Feb. 2021.

[13] F. Deng, M. Jin, C. Liu, M. Liserre, and W. Chen, "Switch open-circuit fault localization strategy for MMCs using sliding-time window based features extraction algorithm," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 10 193–10 206, Oct. 2021.

[14] Z. Ke, J. Pan, R. Na, K. Potty, J. Zhang, J. Wang, and L. Xu, "Single-submodule open-circuit fault diagnosis for a modular multilevel converter using artificial intelligent-based techniques," *IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 3056–3063, Mar. 2019.

[15] S. Venkatachari, A. Mohammadhassani, and A. Mehrizi-Sani, "Submodule fault detection in MMCs using support vector classification," *IEEE Innov. Smart Grid Tech. Conf. Eur.*, Oct. 2021.

[16] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721–2732, May 2015.

[17] C. M. Bishop, "Pattern recognition and machine learning," *Springer*, 2006.

Ardavan Mohammadhassani received the B.Sc. degree in electrical engineering from Urmia University, Urmia, Iran, in 2016, and the M.Sc. degree from the University of Tabriz, Tabriz, Iran, in 2018.

He is currently working towards his Ph.D. degree in electrical engineering at Virginia Tech, Blacksburg, VA, USA. His areas of interest include protection and fault-tolerant control of power electronic converters, protective relaying in inverter-based microgrids and power electronics-rich power systems, control system design for inverter-based microgrids, and power system communications and cybersecurity.

Ali Mehrizi-Sani (S'05–GS'08–M'12–SM'15) received the B.Sc. degrees in electrical engineering and petroleum engineering from Sharif University of Technology, Tehran, Iran, both in 2005. He received the M.Sc. degree from the University of Manitoba, Winnipeg, MB, Canada, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, both in electrical engineering, in 2007 and 2011.

He is currently an Associate Professor at Virginia Tech, Blacksburg, VA, USA, where he is Director of the Resilient Renewable Energy Grid Adaptation Laboratory (REGAL). From 2012 to 2019, he was an Associate Professor and Assistant Professor at Washington State University, Pullman, WA. He has held Visiting Professor appointments at TU Graz, Graz, Austria, in 2014, 2016, and 2018. He was a Research Engineer with CanmetENERGY, Montreal, QC, in 2019 and a Visiting Scientist with Manitoba Hydro International, Winnipeg, MB, in 2018. His areas of interest include power system applications of power electronics, integration of renewable energy resources, and low-inertia systems.

Dr. Mehrizi-Sani is an editor of IEEE TRANSACTIONS ON ENERGY CONVERSION, IEEE POWER ENGINEERING LETTERS, MDPI Energies, and MDIP Electronics. He is a past editor of IEEE TRANSACTIONS ON POWER DELIVERY (2012–2019), IEEE TRANSACTIONS ON POWER SYSTEMS (2016–2020), and *Wiley International Transactions on Electrical Energy Systems (ITEES)* (2017–2019). He was the Chair of IEEE Task Force on Dynamic System Equivalents and the Secretary of CIGRE Working Group C4.34 on Application of PMUs for Monitoring Power System Dynamic Performance. He is the recipient of 2018 IEEE PES Outstanding Young Engineer Award, 2018 ASEE PNW Outstanding Teaching Award, 2017 IEEE Mac E. Van Valkenburg Early Career Teaching Award, 2017 WSU EECS Early Career Excellence in Research, 2016 WSU VCEA Reid Miller Excellence in Teaching Award, 2011 NSERC Postdoctoral Fellowship, and 2007 Dennis Woodford prize for his M.Sc. thesis. From 2007 to 2011, he was a Connaught Scholar at the University of Toronto.