Narrowband Radio Frequency CMOS Low-Noise Amplifier (LNA) Design

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Abstract

The aim of this coursework is to design a radio frequency CMOS low noise amplifier (LNA) for the center frequency 2.2 GHz. The amplifier should have the minimum noise figure matching and impedance matching both at the input and the output.

1. Amplifier architecture

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio [1,3]. An amplifier magnifies the power of the signal and the noise that are fed to the input. LNAs are designed to minimize additional noise. A successful amplifier design must reduce noise by considering trade-offs such as impedance matching, picking the right amplifier technology (such as low-noise components) and choosing low noise biasing conditions.

LNAs are widely used in radio communications systems, medical instruments and other electronic equipment. A typical LNA may have a power gain of 100 (20 decibels (dB)) while decreasing the signal-to-noise ratio by less than a factor of two (a 3 dB noise figure (NF)). Although LNAs are primarily concerned with weak signals that are just above the noise floor, they must also consider the presence of larger signals that cause intermodulation distortion [2, 4].

The most popular circuit of the LNA is shown on Figure 1, The LNA consists of two transistors M1, M2, inductors L_g and L_s, and the load Z_l. The transistor M1 is used to amplify the RF signal on the amplifier input (IN). The transistor M2 is used as a current buffer to eliminate Miller effect, to increase the decoupling between input and output and to increase the stability. The source degeneration inductor L_s is used to introduce feedback.

The feedback is used to match input impedance. The inductor L_g plays the role of the input matching circuit.

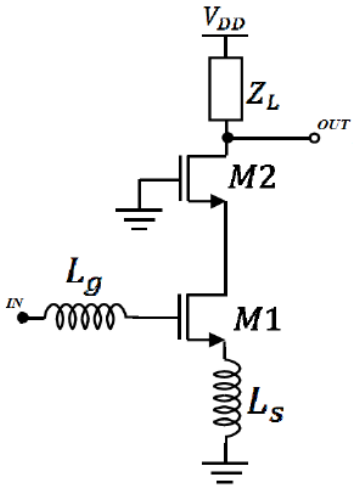

Figure 1 – Simplified circuit of LNA with source degeneration

The full circuit of the LNA is shown on Figure 2 below, its implemented in ADS software:

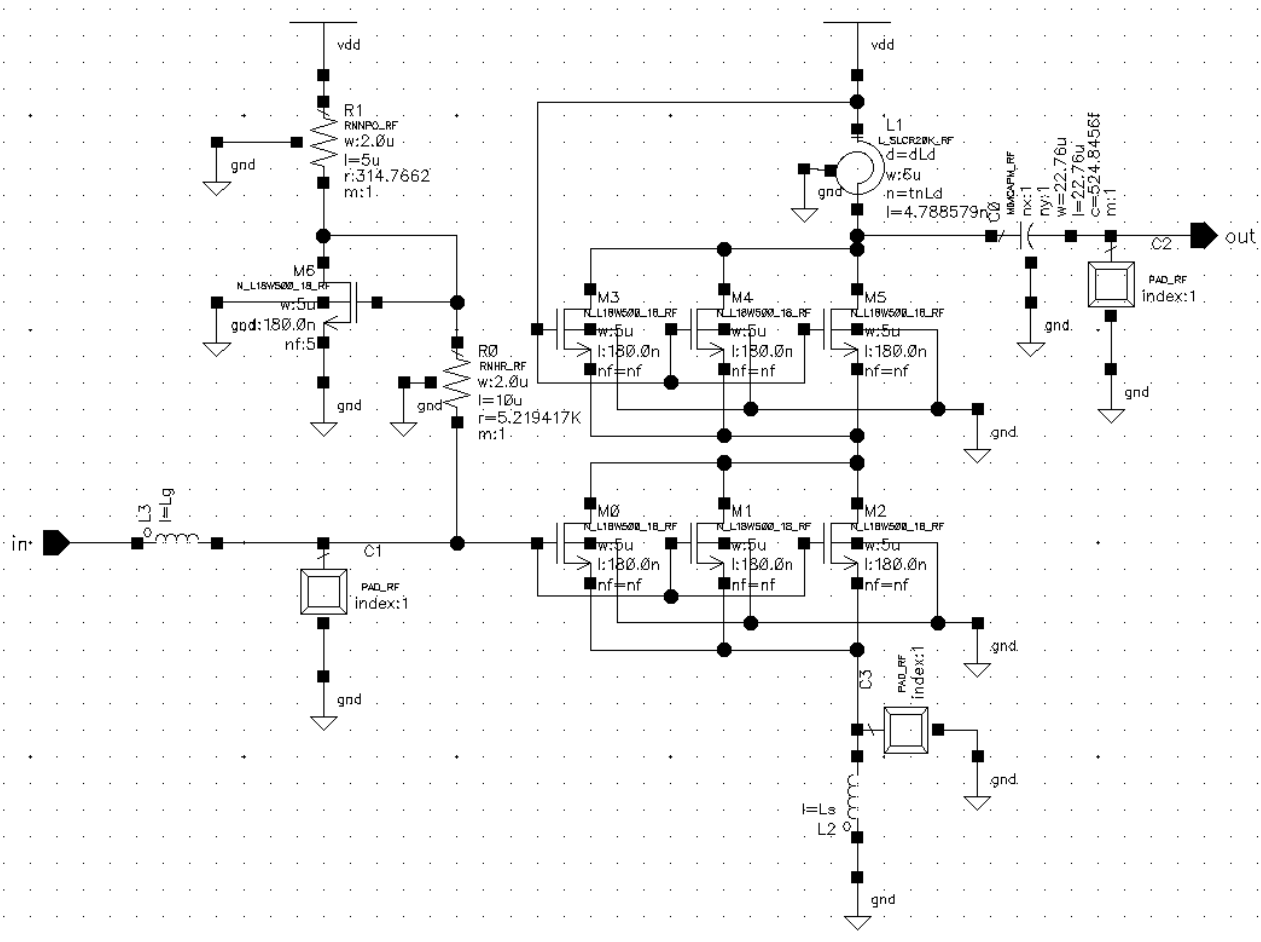

Figure 2 – The circuit diagram of the low noise amplifier.

2. Design technique

2.1 Minimum noise figure and biasing

The noise figure of the amplifier depends on the minimum noise figure and source impedance.

$$F = Fmin + RnGs\ [\ (Gs-Gopt)^2 + (Bs-Bopt)^2\ ]$$

Where F_{min} – minimum noise figure, R_n – equivalent noise resistance, G_s – real part of source admittance, B_s – imaginary part of source admittance, G_{opt} – the real part of optimum source admittance, B_{opt} – the imaginary part of optimum source admittance.

The minimum noise figure depends on the MOS transistor parameters and is expressed by formula

$$NF_{\min} = 1+\frac{2\omega}{\omega T\sqrt{5}}\sqrt{\gamma\delta(1-|c|)^2}$$

there ω – center frequency, ω_T – transient frequency, the constant γ and δ are equal 2/3 and 4/3 for the long channel transistor in saturation consequently, c is the correlation coefficient.

The $NF_{\min}$ primary depends on the ω_T. The ω_T does not depend on the width of the transistor W and depends on the length of the transistor L and the bias of the transistor. It is known that the transient frequency at first increased as the biasing voltage of the transistor V_{bias} increased (gate-source voltage) and after that it starts to decrease. Thus, there is a gate source voltage where the ω_T reach the maximum value. This bias point leads to the minimum noise figure.

Find the bias point where the transistor has minimum $NF_{\min}$ to design the LNA with minimal noise figure:

Examine the transistor minimum noise figure using a test bench circuit shown on Figure 3. The test bench circuit consist of transistor under test what is formed by parallel connection of transistors M2, M3, M4. Capacitor C3 and C4 block the DC current flow to the RF ports. Inductor L0 and L1 block the AC current flow to the voltage source Vbias.

The voltage source Vbias sets the bias point of the transistor (value of the Vbias is the design parameter V_{bias}). The ports Term1 and Term2 are needed for RF simulation.

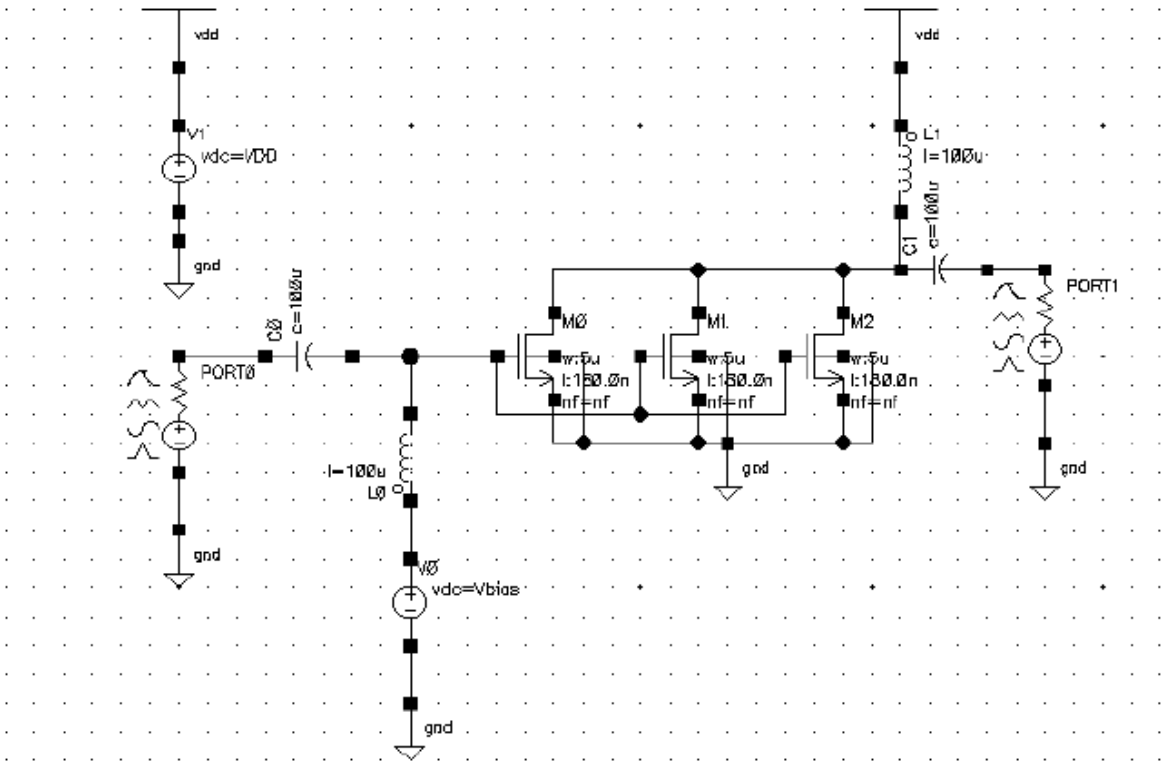

Figure 3 - Transistor test bench.

From the configuration above (figure 3), the voltage value can be found that gives the minimum value of NF, which is 0.720 Volts, later that value will be used in the further simulations.

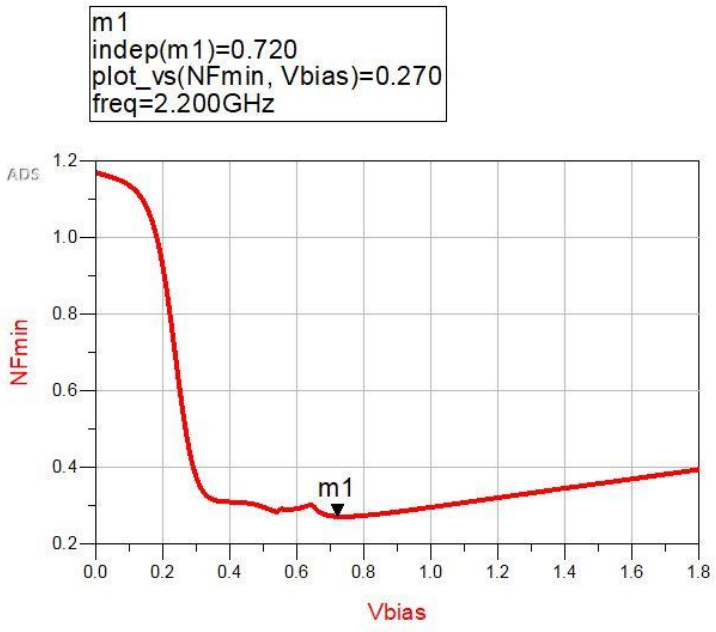

Figure 4 – Finding the optimal value of Vbias

2.2 The optimum source impedance (real part) and transistor width

The noise figure of the amplifier depends on the minimum noise figure and source impedance. When the minimum reachable noise figure is found. The optimum source impedance can be determined. The optimum source impedance Z_{opt} depends on the transistor gate-source capacitance C_{gs} and can be described by formula:

$$Zopt = \frac{1}{\mathrm{Gopt+j\ Xopt}}$$

where

$$Gopt = \alpha\ \omega\ \mathrm{Cgs}\sqrt{\frac{\delta}{5\gamma}\ (1 - |\mathrm{c}|2)}$$

is the real part of source admittance, and

$$Bopt = -\ \omega\ \mathrm{Cgs}\sqrt{\frac{\delta}{5\gamma}}$$

is imaginary part of source admittance.
The input imaginary admittance of the transistor is

$$Bin = \omega Cgs$$

So, the value of B_{opt} and B_{in*} quite close and do not need a matching. The G_{opt} should be matched with the source real admittance for that the C_{gs} should be found that gives

$$Re\{Zopt\} = 50\ \Omega.$$

For that the width W of the transistor should be found because

$$Cgs = 23\ WL\ Cox$$

where C_{ox} is the oxide capacitance per unit area. The W depends on the number of the finger.

- We set the finger number of the transistors on Figure 3 as a design variable (e.g., **nf)**.
- We set sweep variable of S-parameter analysis as finger number of the transistors.
- We simulate the dependence of Z_{opt} as a function of number of fingers using S-parameter analysis.
- The dependence Z_{opt} is represented vs. number of transistor finger on the Z-Smith chart after the simulation. The dependence Z_{opt} vs. number of transistor finger is shown on figure. The point where the curve crosses the 50 Ohm circle is a searchable impedance.
- We choose the finger number corresponded that point (e.g., nf=17 in our case).

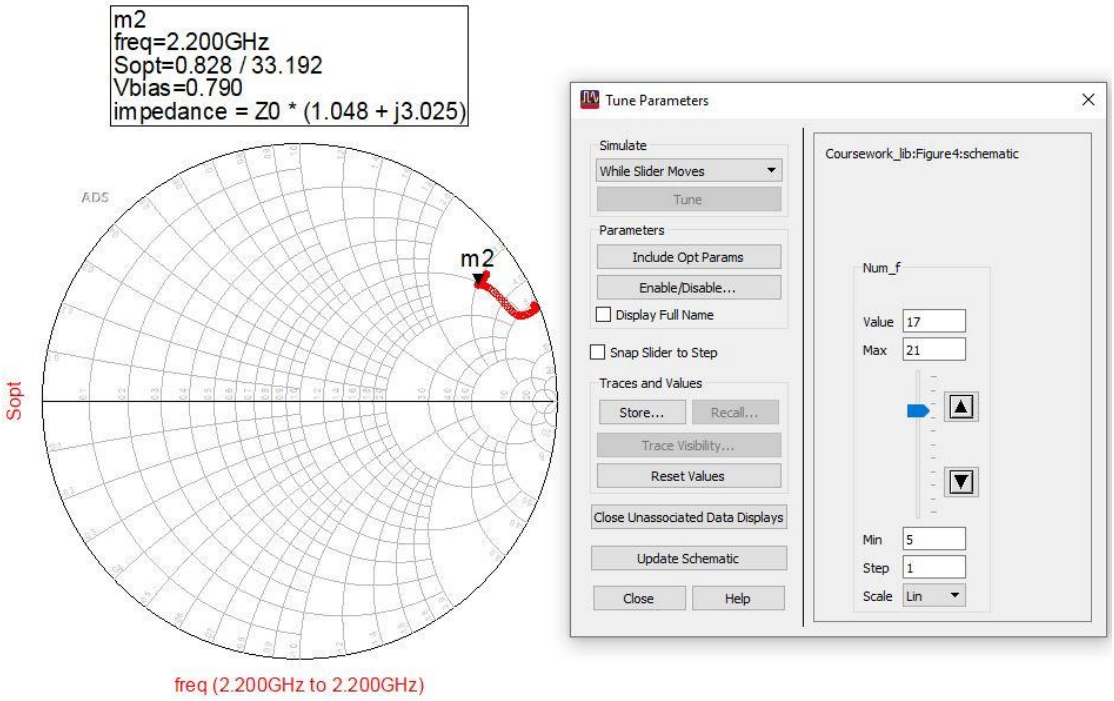

Figure 5 – Tuning the finger number (Num-f) to find the best value

The results show that the best value for finger number is 17, this value will be kept being used in the following schemes.

Another important parameter is the input impedance, the amplifier should be matched with the source impedance. The real part of input impedance could be expressed as

$$R_{in} = \frac{\text{gm}}{\text{Cgs}} Ls = \omega_T L_s$$

where g_m is a transconductance of the transistor, L_s is the inductance of the source degeneration.

- To perform that, we need to add an inductor to the input of the system as shown in figure 6.
- We set the inductance L_s of the inductor as the design variable (e.g **Ls**).
- We set the sweep variable of the S-parameter analysis as inductance L_s.
- The circuit is simulated on the central frequency.
- We plot the dependence S_{11} vs. inductance Ls to represent the dependence of Zin vs. Ls on the center frequency. The point there the curve crosses the 50 Ω circle is the point where Rin is equal 50 Ω.
- We choose the value of Ls that corresponds this point.

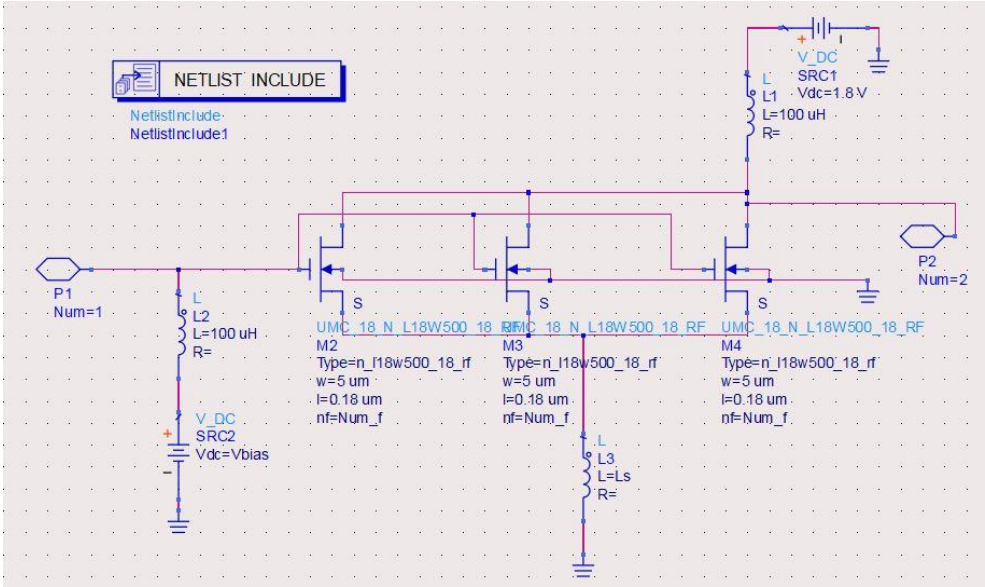

Figure 6 – Low noise amplifier with inductor at the input

Using the scheme in the figure 6 above, we may choose the value of Ls to obtain matched input impedances Zs and Zin (real part), the result is shown below (figure 7), the real part is close to 1 (1.001) which leads to 50, because that is the normalized value.

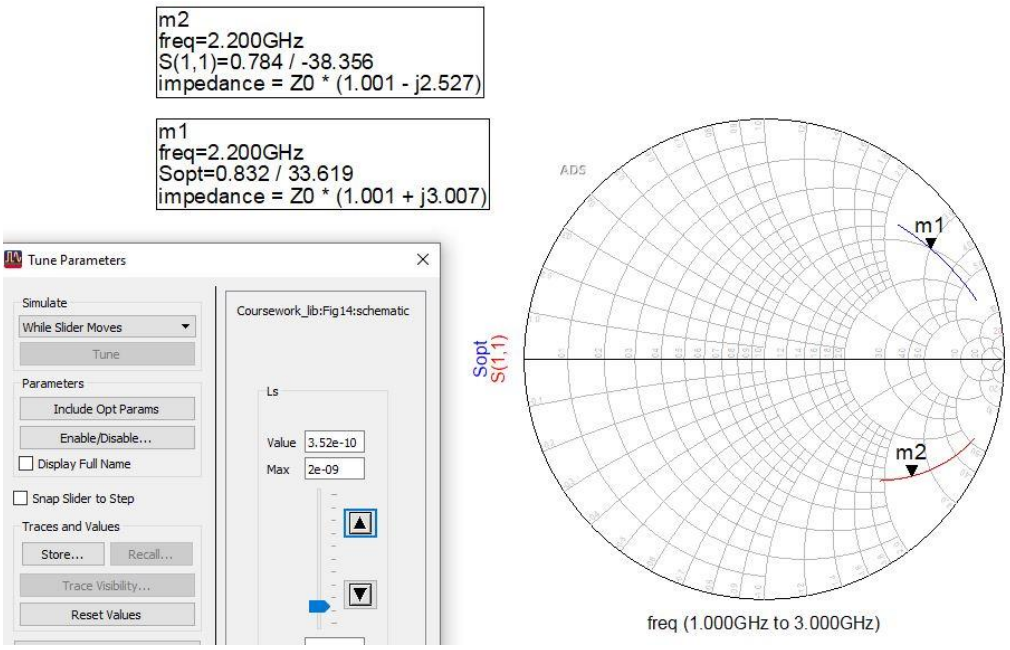

Figure 7 – Results of matching the real part of the impedances Zs and Zin

2.3 Imaginary part of the input impedance and gate inductance

the real part of the impedance as mentioned in section 2.3 is now matched, the imaginary part also has to be matched, the circuit in figure 8 is used for that purpose.

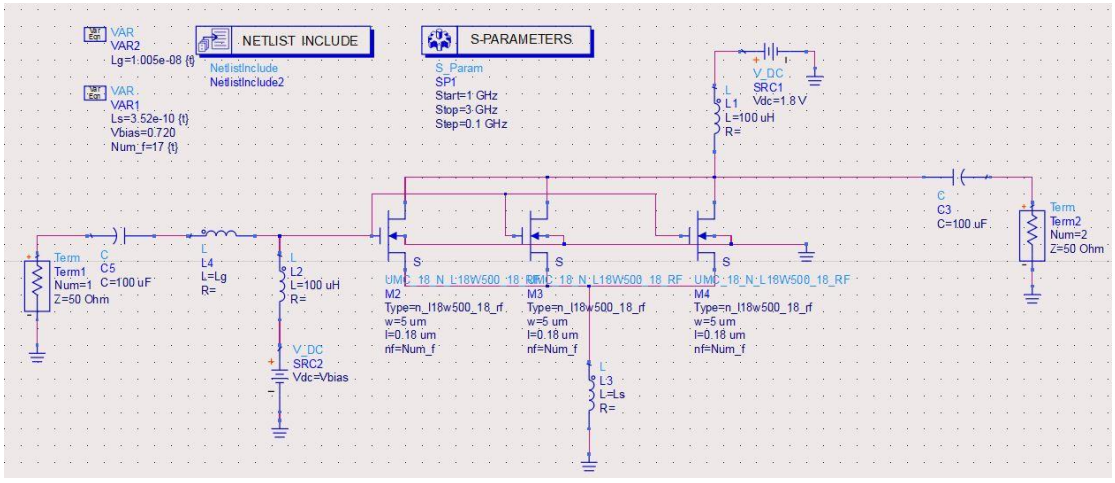

Figure 8 – Connecting the matching circuit to the amplifier

The imaginary part in certain cases cannot be matched, this leads to a non-zero reflection coefficient, such as in this case:

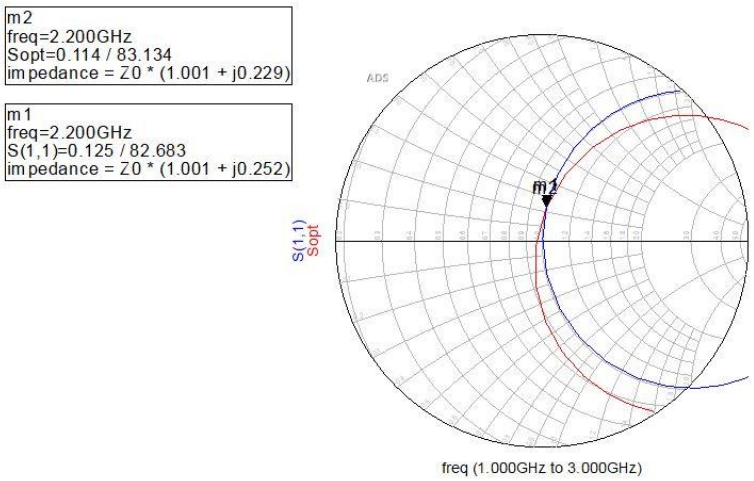

Figure 9 – Attempting to match the imaginary part

2.4 Gain, output impedance and output matching network

To obtain maximum gain and matching LNA at the output, it is necessary to add a load circuit and a circuit to our circuit matching as in figure 10. This circuit should consist of inductance Ld and capacitor C6, C7. It is worth to note that capacitor C7 is optional. The first turn it is necessary to determine the optimal value of the inductance Ld.

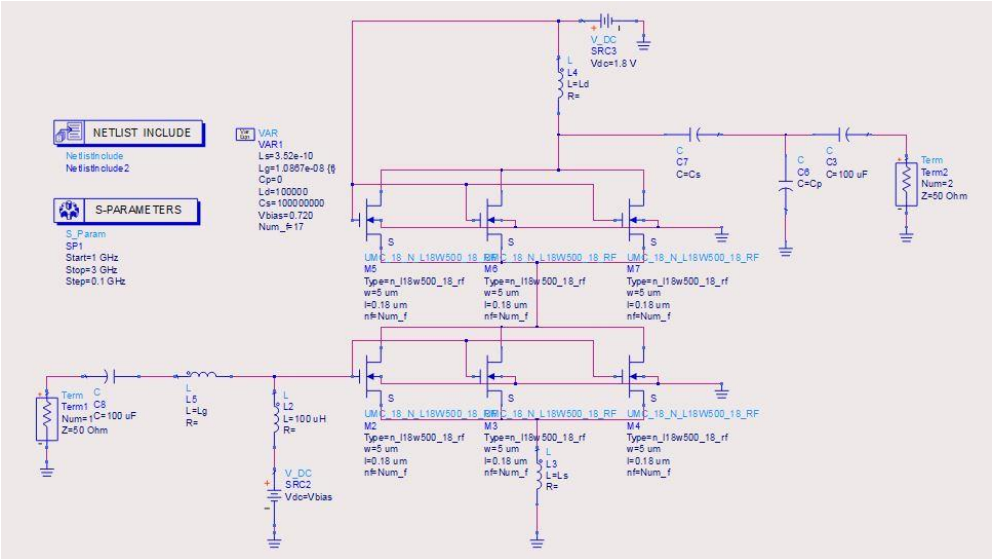

Figure 10 – LNA circuit with the load circuit

The figure below (figure 11) shows the results of simulation:

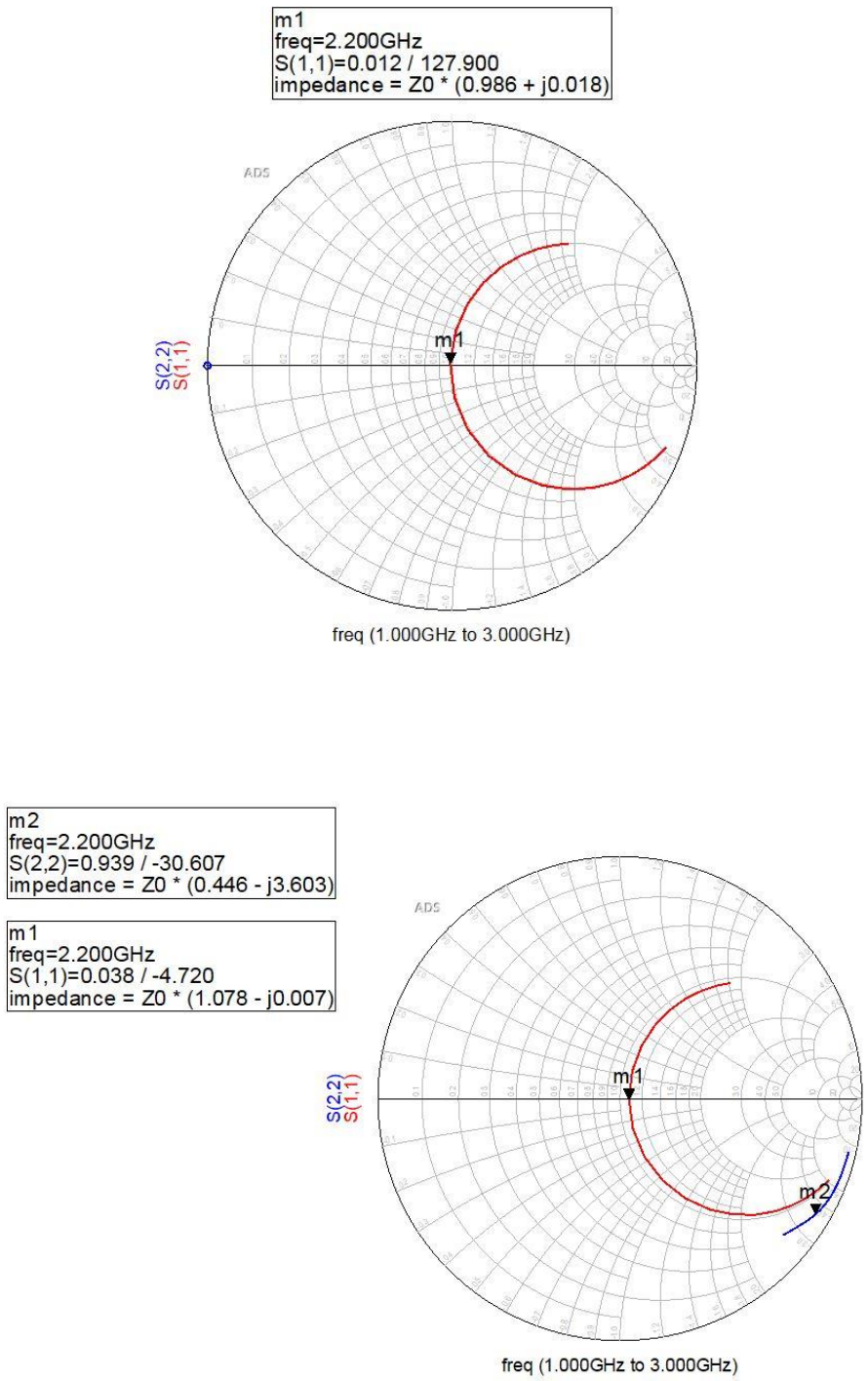

Figure 11 – Dependence of S11 when Ld=0 , Cs = ∞, Cp= 0, L_d = ∞, Cs= ∞, Cp=0, and S22 when L_d= ∞, Cs = ∞, Cp=0 on frequency.

It is necessary to compensate for this capacitance using planar inductance. But in this case, the planar inductance is made from crystal. This inductance is not ideal. As shown in figure 12.

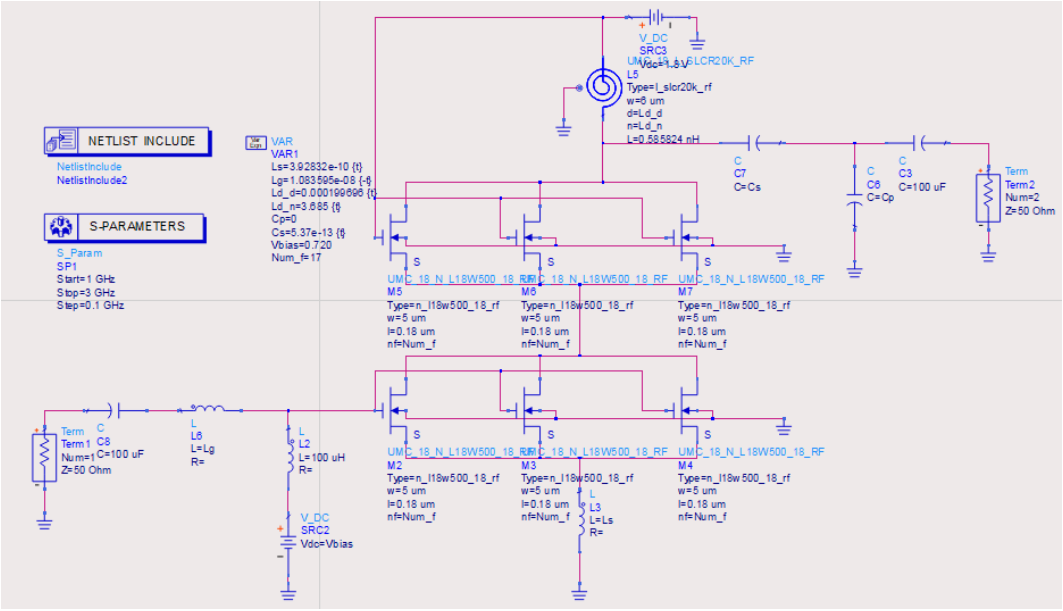

Figure 12 – LNA with planar inductor

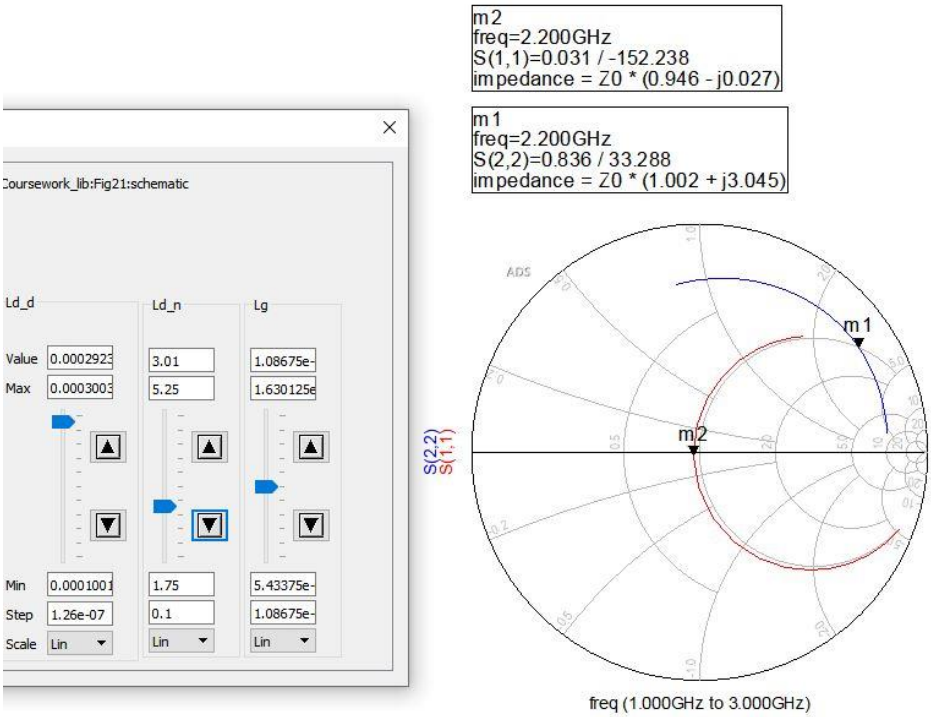

Figure 13 – S22 dependence on frequency when Cs = ∞, Cp = 0

The next step is to match the output of the amplifier. It can be done without the help of capacitor Cp. We do leave capacitor Cp with zero capacity.

By changing the capacitance Cs, we achieve that the output impedance of The LNA would be 50 ohms (S22 = 0). An approximate result is displayed in fig. 14.

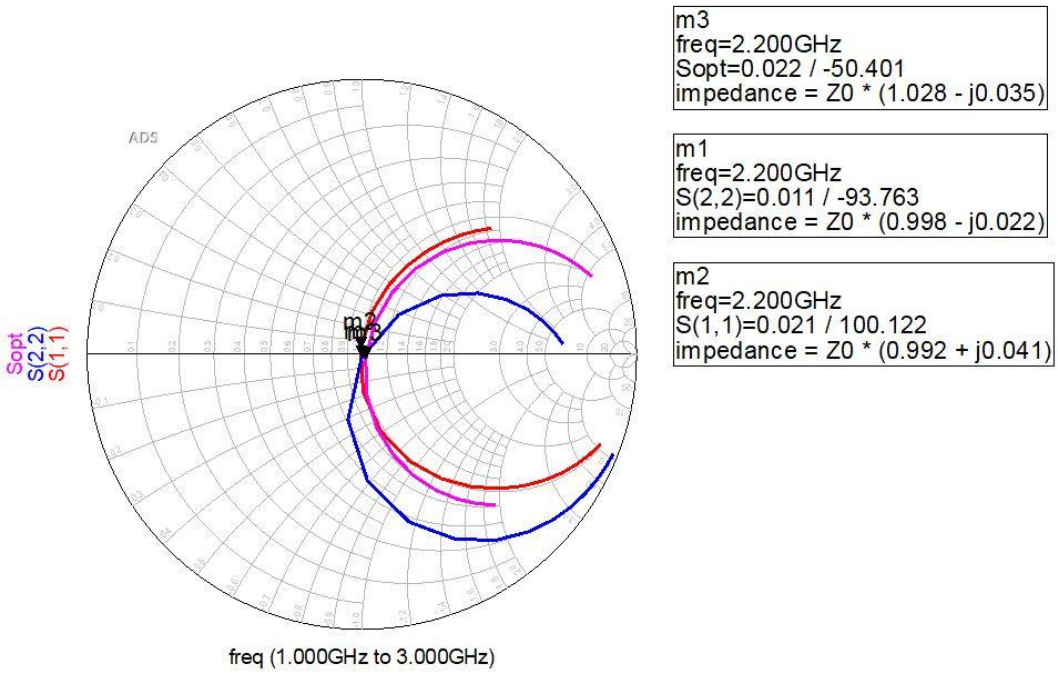

Figure 14 – S11, S22 and Sopt's dependence on frequency when Cp=0

At this stage, we reached complete matching (despite the fact that the imaginary part of the impedance is not exactly zero). But from those further analyses can be made as shown in the figures below and based on the obtained parameters the question of stability is taken into consideration. From the calculated values, the following results can be obtained:

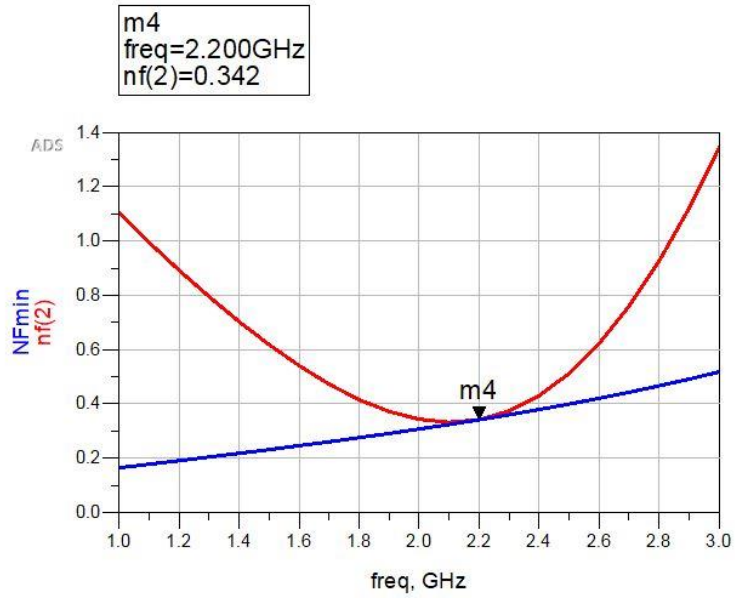

Figure 15 – NF and NFmin's dependency on frequency

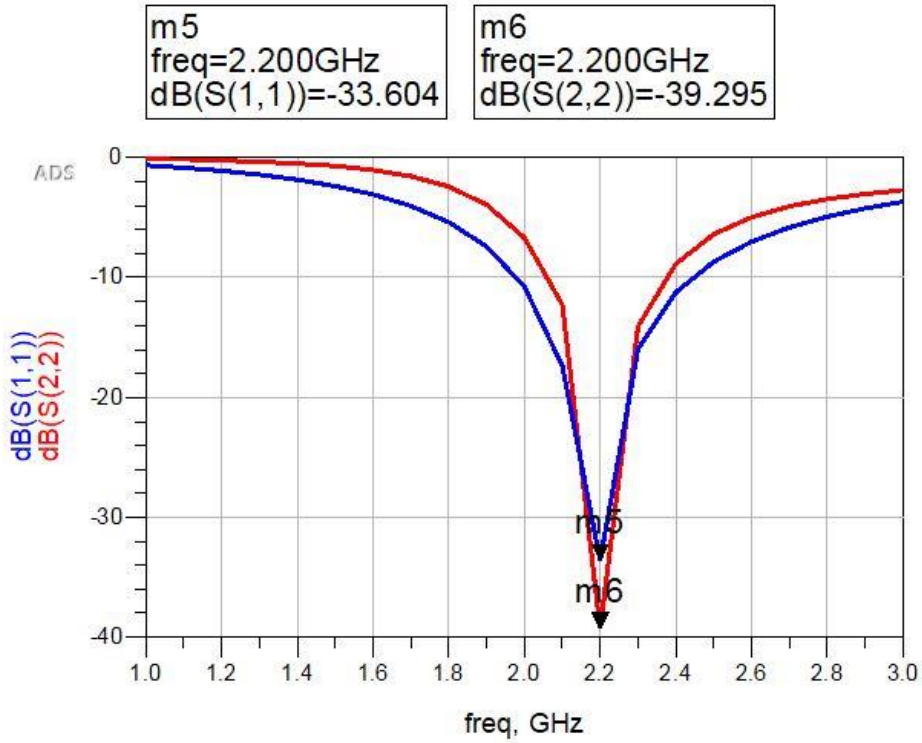

Figure 16 – S11 and S22's dependence on frequency

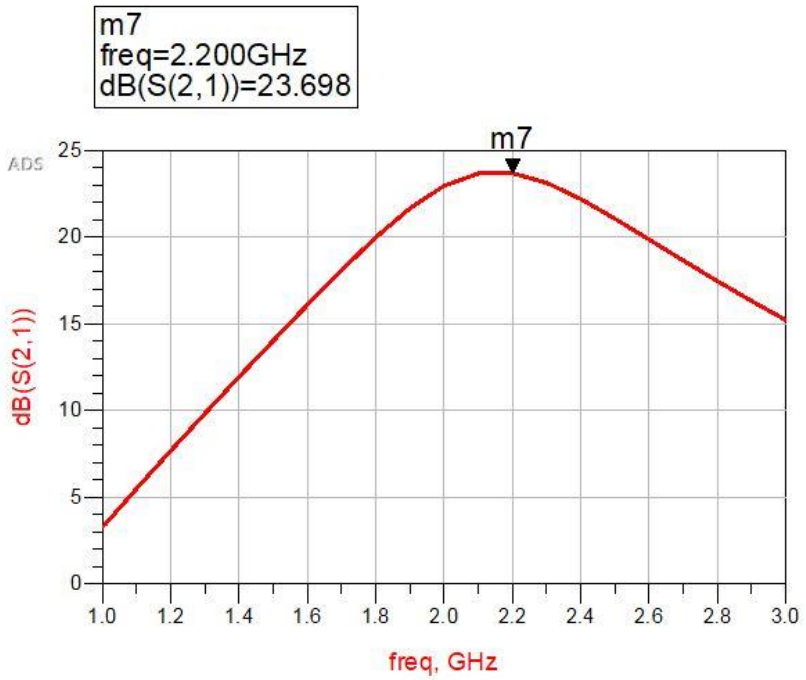

Figure 17 – S21's dependence on frequency

2.5 The full circuit of the LNA

Now that all parameters have been calculated, the complete scheme of the LNA can be configured, the scheme of the complete LNA is shown in figure 18 below:

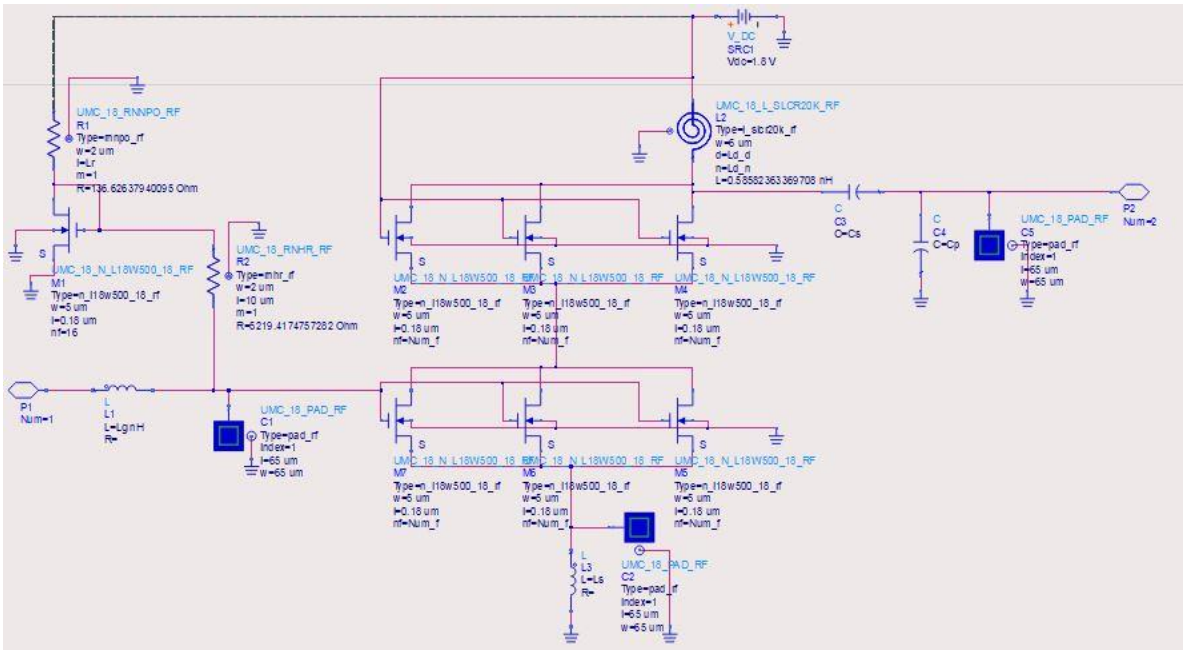

Figure 18 – Complete LNA circuit

From the complete LNA circuit, the following analysis can be made:

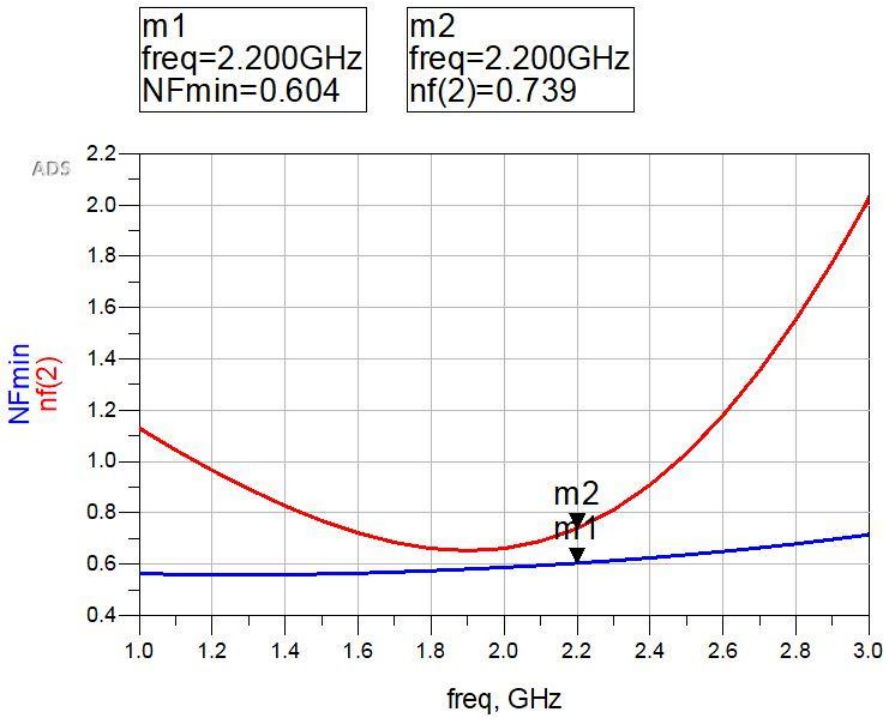

Figure 19 – NF and NFmin's dependency on frequency

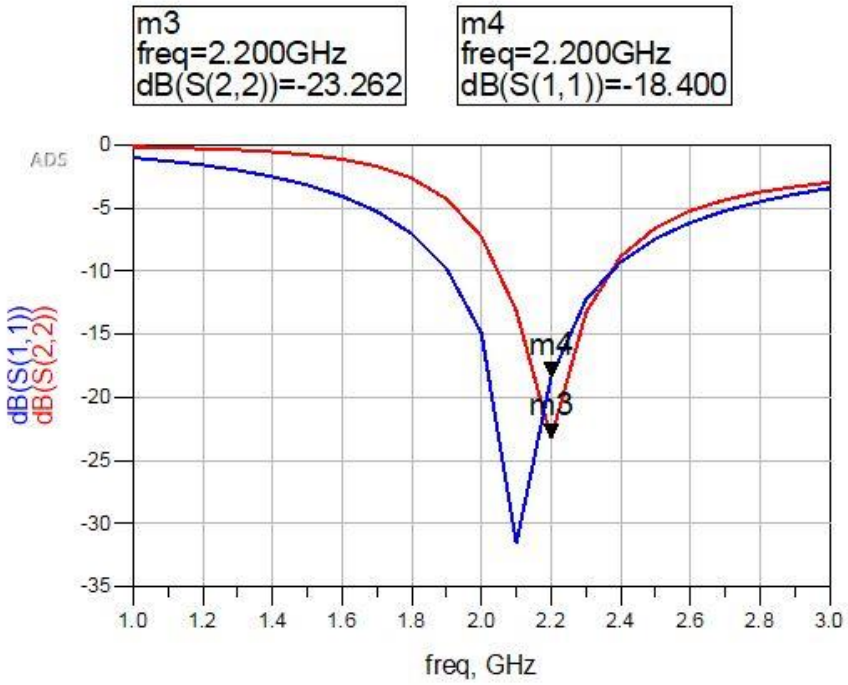

Figure 20 – S11 and S22's dependence on frequency

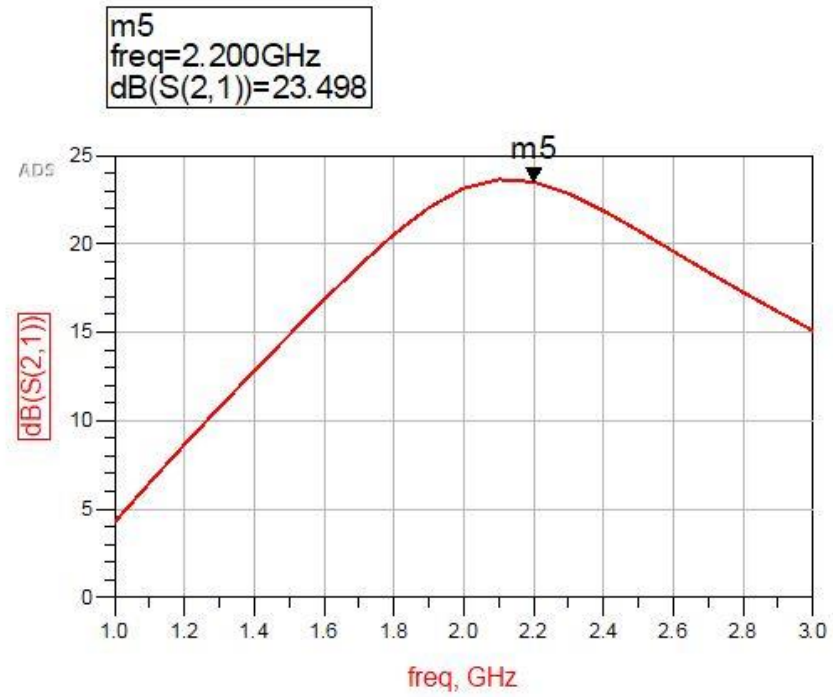

Figure 21 – S21's dependence on frequency

3. Stability

An important part of this coursework is dedicated to the analysis of stability of the LNA, to measure stability the following blocks are used:

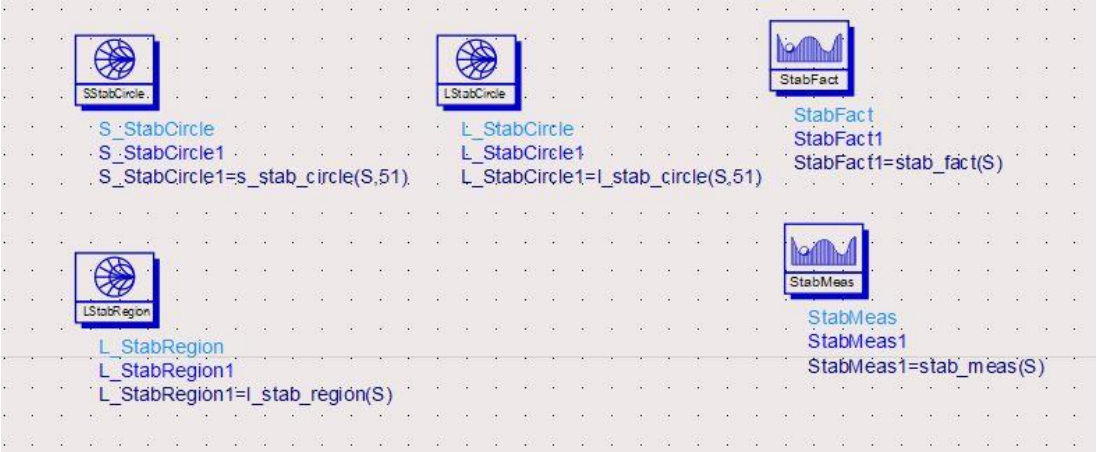

Figure 22 – The used scheme to determine stability

The frequency dependence of stability according to the general criterion is given in terms of s – parameters as shown below in figure 23:

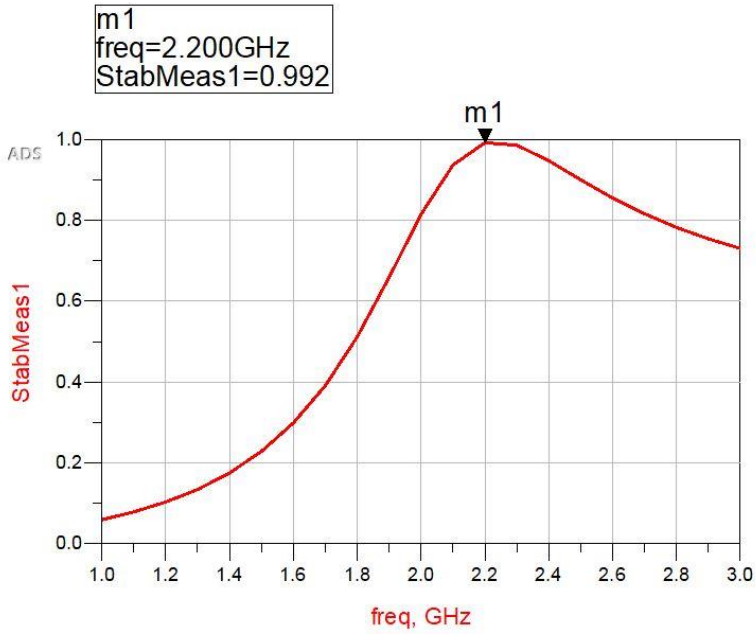

Figure 23 – General criterion for stability analysis

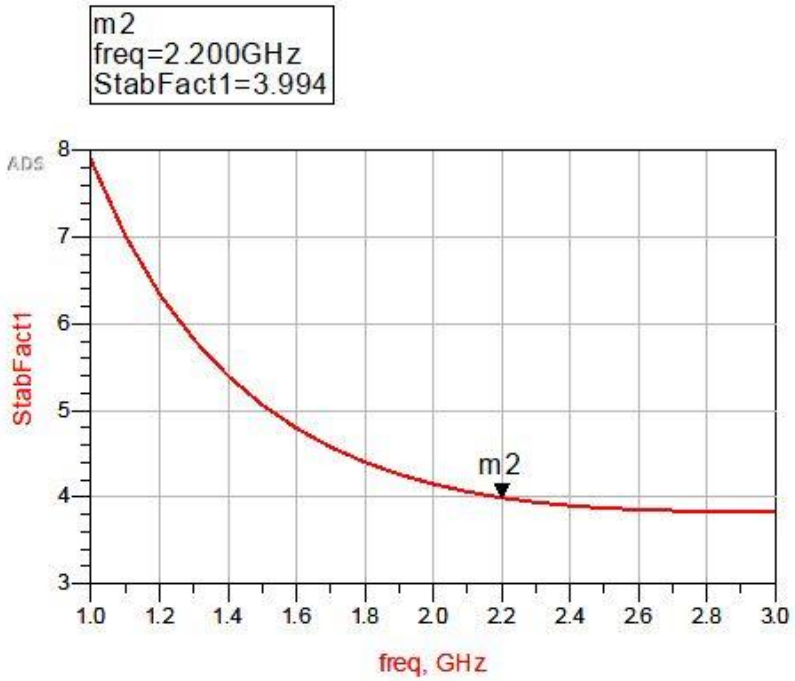

Figure 24 – Rollett stability factor

The LNA is not stable at all frequencies, the frequency obtained in the simulation below is 2.2GHz, and that is the frequency given in the task, this justifies the stability of the LNA:

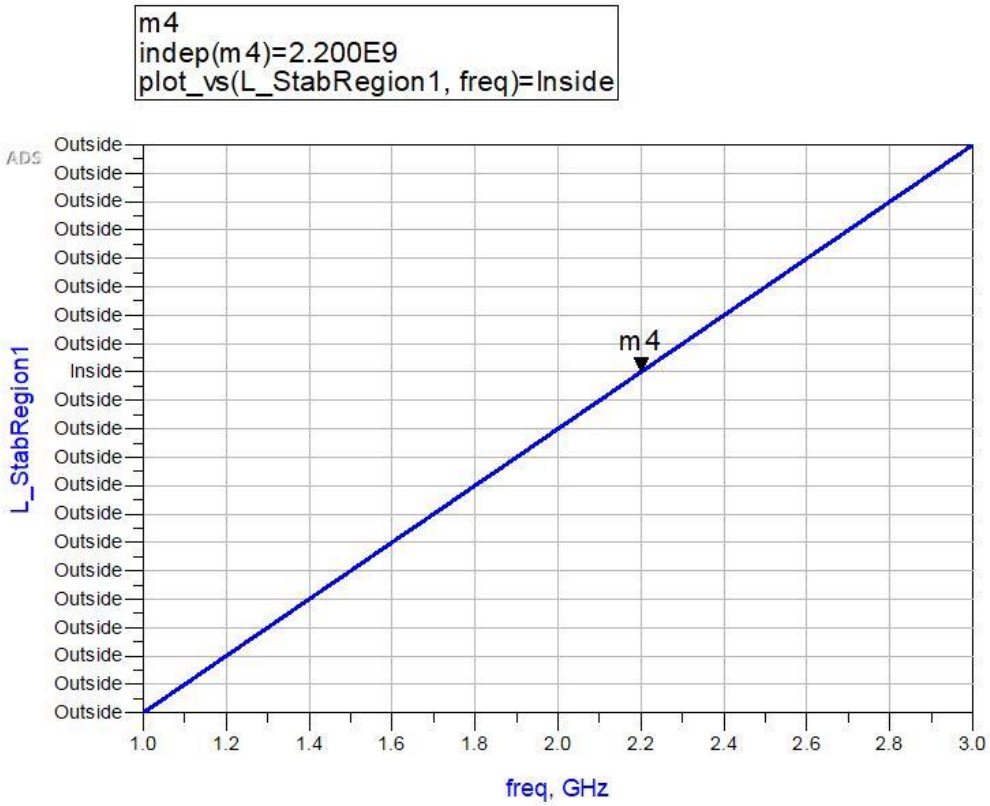

Figure 25 – Stability regions of the LNA

The stability region is also represented on smith chart (please refer to the next page, figure 26):

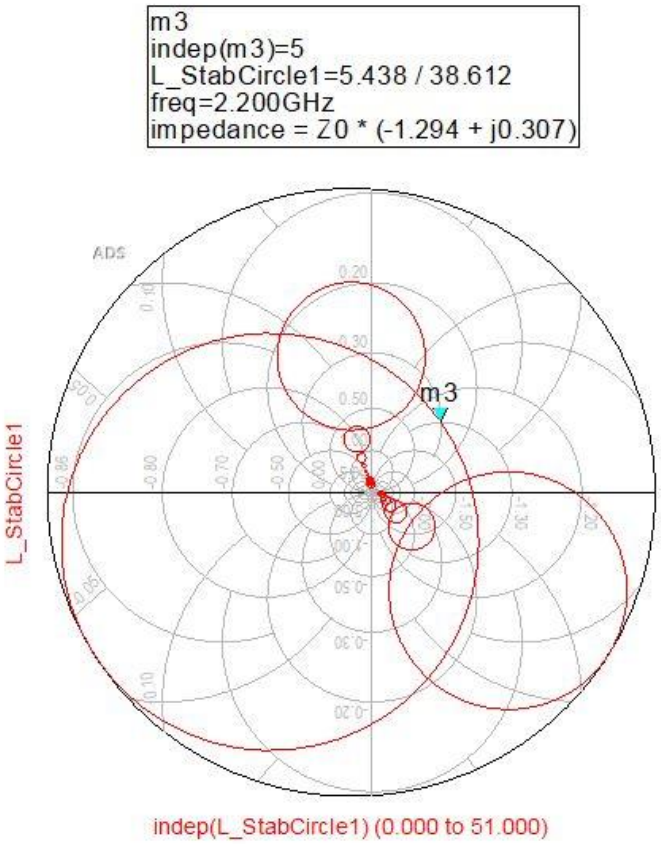

Figure 26 – Amplifier stability regions on Smith chart

The following stage is concerned with single tone analysis, the obtained results are provided below, determining CP1 dB:

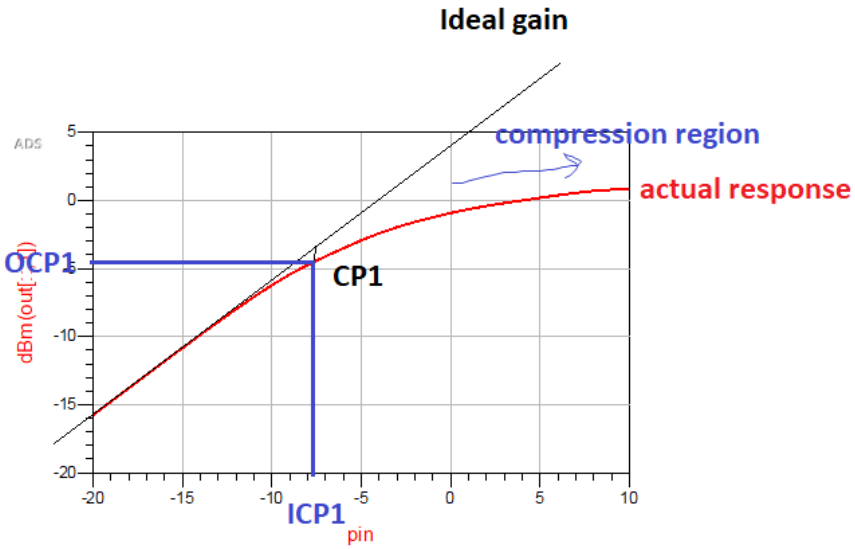

Figure 27 – Dependence of the fundamental harmonic power on the input signal power

The time domain signals are provided below:

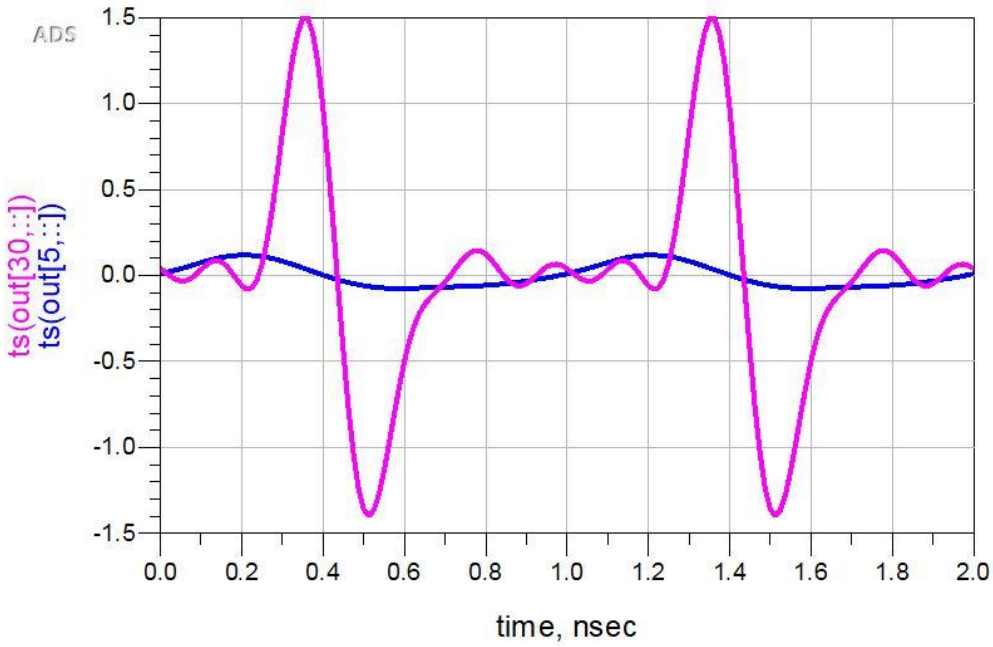

Figure 28 – Output signals in the time domain

Given results in the previous figures were for single tone input, we may conduct the same experiment for two tone input, for this purpose these components have been added to the schematic:

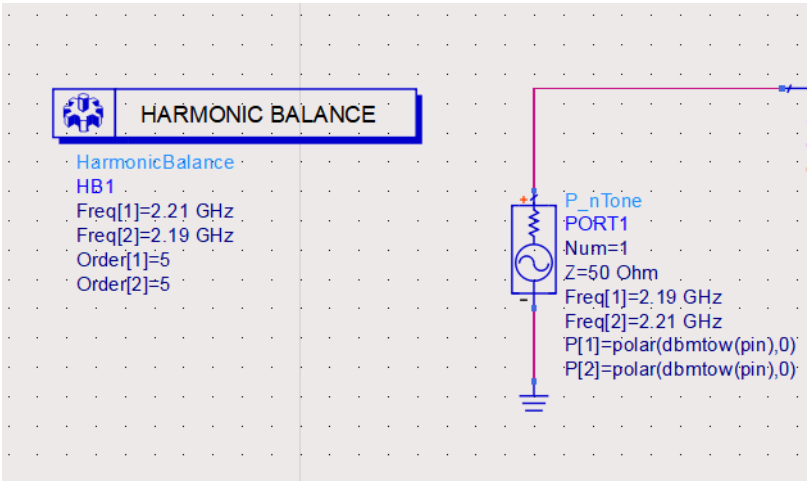

Figure 29 – Adding P_nTone component for two tone analysis

Running the simulation for the two-tone case, will give us the following signal at the output (in time-domain):

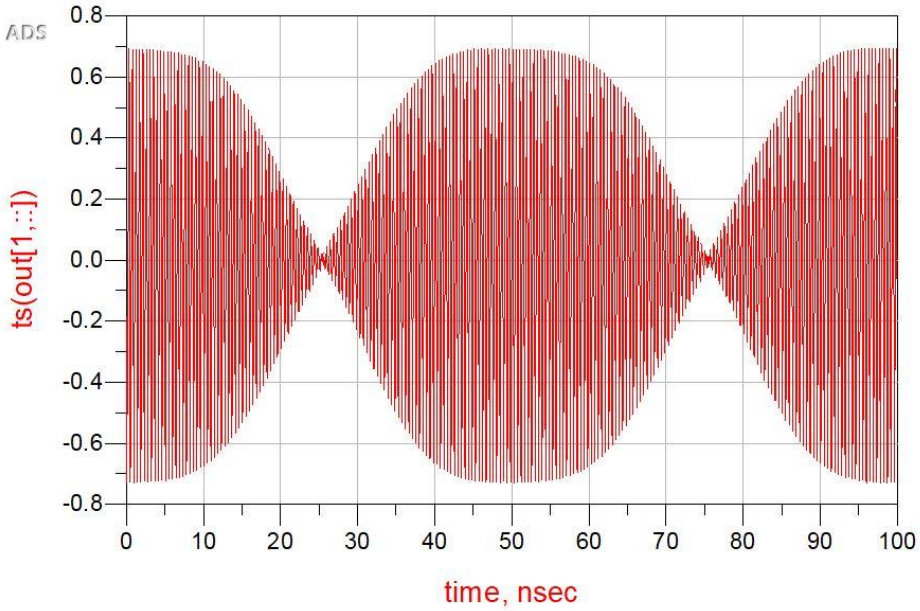

Figure 30 – Output signal in time domain (for double tone analysis)

Conclusion

In conclusion, after the completion of the given coursework, a complete CMOS low noise amplifier circuit was developed to operate at the frequency 2.2 GHz. The amplifier design has minimized the noise figure, the value achieved is (0.739 dB), in addition to that input and output matching has been accomplished. The values that lead to stability and matching are summarized in a table below:

Vbias (V)	Nf	Ls (pH)	Lg (nH)	Ld_d	Ld_n	Cs (pF)
0.720	17	352	10.05	0.0002923	3.01	0.537

Table 1 – The calculated parameters from the analyses

References

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