University of Salahaddin – Hawler College of Engineering Department of Electrical Engineering (4th Year)



Laboratory Manual for **Microelectronics**

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Download the lectures, lab manual & books here:



https://bit.ly/3R1UBXd

Installation guide

LTspice is a free software, it can be downloaded through this link.

https://www.analog.com/en/design-center/design-tools-andcalculators/ltspice-simulator.html

Choose the appropriate version according to your computer's specifications:



Run the installation wizard and follow the steps.

List of Experiments

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Experiment (1) Introduction to LTspice

Objectives:

Students will learn how to use the LTspice circuit simulator, including schematic entry, selecting and running different simulation types, and how to produce simulation output for reports. Example circuits will be simulated to demonstrate the capabilities of LTspice.

Introduction:

LTspice is a fast, free circuit simulator. Linear Technology, Inc. originally designed it for engineers to simulate circuits. It competes with expensive commercial products like Electronic Workbench and PSpice. Advantages of LTspice are that circuit sizes are unlimited, new models can be added, and the user can modify the simulator's behavior.

In this lab exercise you will:

- Get familiar with LTspice
- Enter a simple schematic
- Explore the LTspice component library
- Run simulations for Transient analysis (time-domain)

Procedure:

1. Open LTspice by clicking on this icon.



When it starts up, LTspice may ask if you would like to download an update. Do not do that now.



Fig. 1. LTspice startup window

2. Create new schematic by clicking on this icon



Fig. 2. Create new schematic

3. Left click on Tools > Control Panel > Drafting Options

Set Pen thickness to 5:

🧭 Control Panel			×
Coperation	🛱 Ha	cks!	Internet
Netlist Options	🔍 Sym. & Lil	b. Search Paths	Waveforms
💼 Compression	🕖 Save Defaults	T SPICE	Drafting Options
Allow direct compo Automatically Mark text justificati	nent pin shorts[*]	Font Prope	erties[*]
Mark u	nconnected pins 🗹	Size[*]:	28 ≑
Show schem Ortho	atic grid points[*]	Bold[*]	
Or	tho drag mode[*]		
Cut angled w	rires during drags 🗹	Color Sci	heme[*]
Un-do	history size: 500		
Pen th	ickness[*]: 5 🗸	Hot Ke	eys[*]
Sho	w Title Blocks[*] 🗹		
Reverse Mous	e Wheel Scroll[*]		
Cursor typ	oe[*]: Auto ∨		
[*] Setting rer	nembered between pro	ogram invocation	s.
	Reset to Default Val	ues	
		OK Ca	ancel Help

Fig. 3. Changing Pen thickness

Additionally, click on **Waveforms**, change **Data trace width** and **Cursor width** to 4, this will make schematics look better in reports.

🌮 Control Panel		×			
Operation	Hacks!	¥ Internet			
💼 Compression 🥖	Save Defaults 🛛 👕 SPIC	E Drafting Options			
Netlist Options	🔍 🛛 Sym. & Lib. Search P	aths 🖌 🔛 Waveforms			
Use radian m Font[Font point size]	Data trace width[*]: [Cursor width[*]: easure in waveform expression Mouse cursor type[*]: Auto]: Arial]: 10 🗣 🔽 Bold F	4 ~ 4 ~ s[*] □ ~ ~ Font[*]			
Color Scheme [*]	Open Plot Defe	Hot Keve[*]			
color ocheme[]	Open not beis	Hot Reyal 1			
Directory for .raw and .log) data files[*]				
Store .raw, .p	t and .log data files in a specific	: directory[*]			
		Browse			
[*] Setting remembered between program invocations.					
F	leset to Default Values				
	ОК	Cancel Help			

Fig. 4. Changing Data trace width and Cursor width

4. Add the element in Fig. 5., let us begin by adding an operational amplifier. Click on the AND symt to open the library of components. Insert "OP27" as shown in Fig. 6.



Fig. 5. Components library

🗗 Select Component Symbol				
Top Directory:	Directory: C:\Users\araas\OneDrive\Documents\LTspiceXVII\ib\sym			
F	+	Low Noise, Pre Operational Ar	ecision, High Speed nplifier	
*	1-	Open this ma	cromodel's example	circuit
C:\Users\ara	aas \OneDrive \Docum	ents\LTspiceXVII\i	ib\sym\OpAmps\	
MAX4436	OP1177	OP37	opamp2	Un
MAX4488	OP177A	OP413	RH101A	Un
MAX4489	OP 19 1	OP4177	RH1028	Un
MAX9636	OP213	OP491	RH1056A	Un
MAX9638	OP2177	OP492	RH1128	Un
MAX9914	OP227	OP495	RH1498	Un
MAX9915	OP27	OP727	RH1814	Un
MAX9916	OP284	OP747	RH27C	
MAX9917	OP291	OP77	RH37C	
OP07	OP292	OP777	RH6200	
OP113	OP296	opamp	SSM2141	
<				>
C	Cancel		ОК	

Fig. 6. Inserting an element

Add two resistors, click on resistor symbol as in Fig. 7.



Fig. 7. Resistor symbol

Set the value to 1K, by right-clicking on the resistor & setting the resistance to 1K.



Fig. 8. Changing resistance value

Add ground \checkmark and connect the components using wire \checkmark as shown in Fig. 9.



Fig. 9. Connecting the two resistors to negative pin of the op-amp

Insert a 10K resistor to the output of the amplifier as in Fig. 10.



Fig. 10. Adding load

Right click on the wire, click on Label Net, name this wire OUT as in Fig. 11.



Fig. 11. Labeling a wire

Add three voltage sources, as shown in Fig. 12.

Top Directory: C:\Users\araas\OneDrive\Documents\LTspiceXVII\\ib\sym Voltage Source, either DC, AC, PULSE, SINE, PWL, EXP, or SFFM Voltage Open this macromodel's example circuit voltage C:\Users\araas\OneDrive\Documents\LTspiceXVII\\ib\sym\ Image C:\Users\araas\OneDrive\Documents\LTspiceXVII\\ib\sym\ Image C:\Users\araas\OneDrive\Documents\LTspiceXVII\\ib\sym\ Image Image </th <th>🍠 Select Comp</th> <th>onent Symbol</th> <th>×</th>	🍠 Select Comp	onent Symbol	×
Voltage Source, either DC, AC, PULSE, SINE, PWL, EXP, or SFFM Open this macromodel's example circuit voltage C:\Users\araas\OneDrive\Documents\LTspiceXVIIVib\sym\ load npn4 SOAtherm-HeatSink load2 pif pnp pmos SOAtherm-NMOS lpnp pmos4 sw mesfet pnp nmos pnp4 varactor nmos4 polcap npn2 res2 npn3 schottky	Top Directory:	C: \Users\araas\Or	neDrive \Documents \LTspiceXVII \ib \sym ~
C:\Users\araas\OneDrive\Documents\LTspiceXVII\ib\sym\ load npn4 SOAtherm-HeatSink load2 pjf SOAtherm-NMOS lpnp pmos SOAtherm-PCB ltline pmos4 sw mesfet pnp tline nmos pnp4 varactor nmos4 polcap voltage npn1 res2 zener npn3 schottky >		ŧ	Voltage Source, either DC, AC, PULSE, SINE, PWL, EXP, or SFFM Open this macromodel's example circuit
load npn4 SOAtherm-HeatSink load2 pjf SOAtherm-NMOS lpnp pmos SOAtherm-PCB ltline pmos4 sw mesfet pnp tline njf pnp2 TVSdiode nmos pnp4 varactor nmos4 polcap voltage npn res zener npn3 schottky ✓	C:\Users\ara	aas \OneDrive \Docum	nents\LTspiceXVII\lib\sym\
	load load2 lpnp ltline mesfet njf nmos nmos4 npn npn2 npn3	npn4 pjf pmos pmos4 pnp pnp2 pnp4 polcap res res2 schottky	SOAtherm-HeatSink SOAtherm-NMOS SOAtherm-PCB sw tline TVSdiode varactor voltage zener
Cancel OK		Cancel	ОК

Fig. 12. Finding voltage source in the component library

Add wires and connect them to ground, as in Fig. 13. Right click on the voltage source to set their values, set V1 and V2 to 15 and -15. Click OK

1	1	1	😕 Voltage Source - V1	×
V1 V	v2	V3	DC value[V]: 15 Series Resistance[Ω]:	OK Cancel Advanced

Fig. 12. Three voltage sources

V1 and V2 are the DC sources, V3 is an AC source (sine signal),

right click on V3 > Advanced, you will see the window in Fig. 13. Click on **SINE**, set the values of **DC offset**, **Amplitude** and **Frequency to** 0, 1 and 10K as in Fig. 13.

💯 Independent Voltage Source - Vin	×
Functions (none) PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	DC Value:
 EXP(V1 V2 Td1 Tau1 Td2 Tau2) SFFM(Voff Vamp Fcar MDI Fsig) PWL(t1 v1 t2 v2) PWL FILE: 	Small signal AC analysis(.AC) AC Amplitude: AC Phase: Make this information visible on schematic: 🗹
DC offset[V]: 0 Amplitude[V]: 1 Freq[Hz]: 10K	Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: ☑
Tdelay[s]: Theta[1/s]: Phi[deg]: Ncycles:	
Additional PWL Points Make this information visible on schematic: 🗹	Cancel OK

Fig. 13. Three voltage sources

Label the voltage sources V1 & V2 to +V and -V, label the input voltage "IN" and connect the full schematic in Fig. 14. DON'T FORGET to label the positive terminal of the op-amp to +V and the negative terminal of the op-amp to -V.



Fig. 14. Non-inverting amplifier's full schematic

After completing the circuit connection in Fig. 14, you may now start running the simulation, click on the run symbol $\stackrel{>}{>}$ and set **Stop time** to 1 ms, then click OK.

▶ 🚄	; 🖬 😭	×.) 🗨	99	🎗 😫	<u>≩</u> L⊈	
N7	e 1.e e						
Edit	Simulation Com	imand					~
Transi	ent AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt		
	Perf	om a non-lin	ear, time	domain sim <u>ula</u>	tion.		
			<	Stop time:	1m		>
		Time	e to start	saving data:			
			Maximu	ım Timestep:			
	Start e	external DC s	upply vol	tages at OV: [
	Stop sim	ulating if stea	ady state	is detected: [
	Don't reset T	=0 when stea	ady state	is detected: [
		Step the	e load cui	rent source: [
	9	Skip initial op	erating p	oint solution: [
Syntax:	.tran <tstop> [<o< td=""><td>ption> (<opti< td=""><td>on>]]</td><td></td><td></td><td></td><td></td></opti<></td></o<></tstop>	ption> (<opti< td=""><td>on>]]</td><td></td><td></td><td></td><td></td></opti<>	on>]]				
.tran 1m	ı						
	Car	ncel		C)K		

Fig. 15. Transient analysis specifications

You will see a blank (Draft screen) as shown in Fig. 16:

🚰 Draft1 📫	Draft 1									
🚉 Draft1									_	
0.0ms	0.1ms	0.2ms	0.3ms	0.4ms	0.5ms	0.6ms	0.7ms	0.8ms	0.9ms	1.0ms
🕻 Draft1										
			v1 ↓15	↓ ^{V2} ↓-15	N Vin1 5 SINE(0 1 100	J2 OI DP27 ()	JT Rload 10K			

Fig. 16. Screen capture after running transient analysis

To obtain input and output waveforms, you need to click on the wires indicated in Fig. 17.



Fig. 17. Clickable wires

The results are provided in Fig. 18:





Report requirements:

1. Modify the circuit in this experiment into an inverting op-amp, amplify this signal: $0.5 \sin(2\pi, 100000t)$, set gain as 10.



- 2. Choose the *Stop time* carefully so only 5 periods will be shown.
- 3. Add all the screenshots and write a conclusion of your work in the report.
- 4. Why do we use LTspice? What are the advantages?

Experiment (2) AC and DC Analyses

Objectives:

Upon the completion of this experiment, students will be able to perform several types of SPICE simulation: DC Analysis, AC Analysis, Transient Analysis (covered in Experiment 1). This first part of this experiment is concerned with performing DC Analysis for a CMOS inverter, while the second part is on performing AC Analysis for an amplifier.

Introduction:

Nearly all SPICE-based simulators are capable of performing well known analysis functions.

Analysis Method	Function			
Transient Analysis	Gives time domain waveforms which are plots of voltage or			
	current versus time. (Oscilloscope)			
AC analysis	Gives the voltage or current versus frequency in a linearized			
	version of the circuit.			
DC analysis	Gives DC voltage or current, usually versus a stepped voltage or			
	current.			
Fourier analysis	Plot the frequency content of any waveform using Fourier			
	analysis			
Noise analysis	Noise analysis at measurement points.			
Monte Carlo	Simulations that reflect variation in circuit elements.			
S-parameter	High-frequency characteristic analysis.			

In this experiment you will run simulations for:

- 1. DC operating point.
- 2. AC small-signal frequency response

Procedure:

- 1. Open a new schematic file in LTspice.
- 2. Add a pmos4 transistor and a nmos4 transistor as shown in Fig. 1.
- 3. Place the PMOS transistor above the NMOS transistor as in Fig. 2.

🌮 Select Component Symbol 🛛 🕹				
Top Directory: C:\Users\araas\OneDrive\Documents\LTspiceXVII\ib\syn				\sim
		N-Channel M Open this n nmos	OSFET transistor	cuit
[SpecialFunctions] [Switches] bi bi2 bv cap csw current diode e e2	f FerriteBead FerriteBead2 g g2 h ind ind2 ISO 16750-2 ISO 7637-2 LED	load load2 lpnp ltline mesfet njf nmos nmos4 npn npn2 npn3	npn4 pjf pmos pmos4 pnp pnp2 pnp4 polcap res res2 schottky	
<				>
Ca	ancel		ОК	.:

Fig. 1. nmos transistor in component library



Fig. 2. PMOS and NMOS transistors

Right click on the PMOS transistor and **carefully** set the specifications as illustrated in Fig. 3:

Monolithic MOSFET - M4	4	×
Model Name:	P_50n	OK
Length(L):	50n	Cancel
Width(W):	1u	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		
P_50n I=50n w=1u		

Fig. 3. PMOS specifications

Right click on the NMOS transistor and **carefully** set the specifications as illustrated in Fig. 4:

Monolithic MOSFET - M	5	×
Model Name:	N_50n	ОК
Length(L):	50n	Cancel
Width(W):	500n	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		
N_50n I=50n w=500n		

Fig. 4. NMOS specifications

Add two voltage sources (VDD = 1) and (Vin = 0), then connect the circuit in Fig. 5:



Fig. 5. CMOS inverter (NOT gate)

The transistor specifications have to be inserted through a text document (cmos.txt), the file is given to you by the lecturer, put the schematic file in the same folder with the **cmos.txt** file. Click on the Spice directive symbol, type: **.include cmos.txt** as shown in Fig. 6:

🕑 Edit Text on the Schema	atic:	>
How to netlist this text Comment SPICE directive	Justification Left Vertical Text	Font Size OK i(default) V Cancel
.include cmos.txt		~

Fig. 6. Spice directive

Now we can run the DC analysis, click on Run *fig.*, choose DC sweep, set the specifications as in **Fig. 7**:

🔊 Edit Simulation Command 🛛 🕹 🗙
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt
Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.
1st Source 2nd Source 3rd Source
Name of 1st source to sweep: Vin
Type of sweep: Linear V
Start value: 0
Stop value: 1
Increment:
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<lncr>] [<source2>]</source2></lncr></stop></start></source1></oct,dec,lin>
.dc Vin U 1
Cancel OK

Fig. 7. DC operating point details



Click OK, then select Vout to plot, you should obtain a figure like the plot in Fig. 8.

Once you completed the first part of this experiment, please save the file, for the second part of the experiment, you will need to create a new schematic, configure the circuit provided in Fig. 9:



Fig. 9. Circuit diagram of the amplifier

run AC analysis, click on Run , choose **AC Analysis**, set the specifications as in **Fig. 10**:

🗗 Edit Sir	nulation Com	imand					×
Transient	AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt		
Compute	the small signa	I AC behavio	r of the c point.	ircuit linearized	about its D(C operating	
		Type of	sweep:	Decade	\sim		
	Number	of points per	decade:	100			
		Start fre	quency:	10MEG			
		Stop fre	quency:	100G			
Syntax: .a	c <oct, dec,="" lin:<="" td=""><td>> <npoints> <</npoints></td><td><startfre< td=""><td>q> <endfreq></endfreq></td><td></td><td></td><td></td></startfre<></td></oct,>	> <npoints> <</npoints>	<startfre< td=""><td>q> <endfreq></endfreq></td><td></td><td></td><td></td></startfre<>	q> <endfreq></endfreq>			
.ac dec 10	0 10MEG 1000	ì					
	Car	ncel		0	к		

Fig. 10. Details of the AC Analysis

Press OK, then select Vout to plot, the result is the frequency response of the amplifier as depicted in **Fig. 11**:



Report requirements:

1. For the CMOS inverter, replace the DC voltage source (Vin) to Pulse signal with these specifications, what does the output look like in time-domain? Does the DC operating point change? Add screenshots with your answers.

🝠 Independent Voltage Source - Vin								
Functions								
(none)								
PULSE(V1 V2 Tdelay Trise Tfall Ton Pe	eriod Nayal	es)						
◯ SINE(Voffset Vamp Freq Td Theta Phi I	Vcycles)							
O EXP(V1 V2 Td1 Tau1 Td2 Tau2)								
◯ SFFM(Voff Vamp Fcar MDI Fsig)								
O PWL(t1 v1 t2 v2)								
O PWL FILE:		Browse						
Vinitial[V]:	0							
Von[V]:	1							
Tdelay[s]:	0							
Trise[s]:	0.3m							
Tfall[s]:	0.3m							
Ton[s]:	15m							
Tperiod[s]:	30m							
Ncycles:	100							

2. How does an ideal amplifier's phase response look like? Show it on Fig. 11.

Experiment (3) Junction Field-Effect Transistor Characteristics

Objectives:

The students will learn how to plot transistor IV characteristics using DC sweep analysis in LTspice.

Introduction:

Junction field effect transistors are widely used devices in electronic circuits (amplifiers, switching circuits, oscillators, etc.), JFETs use a small voltage to control current flow, JFETs are unipolar devices which means the current that passes through the channel consists of either electrons (in an N-type JFET) or holes (in a P-type JFET).

Procedure:

1. Create a new schematic



2. Search for **njf** (N-channel JFET) as in Fig. 1.

🍠 Select Compo	onent Symbol			\times		
Top Directory:	C:\Users\araas\On	eDrive \Document	ts\LTspiceXVII\lib\sym	\sim		
		N-Channel JF	ΈT			
		Open this m	nacromodel's example c	ircuit		
C:\Users\araa						
C:\Users\araas\OneDrive\Documents\LTspiceXVII\\ib\sym\ [SpecialFunctions] f load npn4 [Switches] FerriteBead load2 pjf bi FerriteBead2 lpnp pmos bi2 g ltine pmos4 bv g2 mesfet pnp cap h njf pnp2 csw ind nmos4 polcap diode ISO16750-2 npn res e ISO7637-2 npn2 res2 e2 LED npn3 schottky						
Ca	ancel		ОК			

Fig. 1. N-Channel JFET

3. Right click on the transistor symbol then choose (Pick New JFET) as in Fig. 2.



Fig. 2. N-Channel JFET

Choose 2N5432 transistor in the list.

🗗 Select J	FET Transistor			×
			ок	[
			Cano	:el
Part No.	Manufacturer	Polarity	SPICE Model	^
2N3819	Vishay	njf	.model 2N3819 NJF(Beta=1.304m Betatce=5 Rd=1 Rs=1 L	an
2N5432	Fairchild	njf	.model 2N5432 NJF(Beta=9.109m Betatce=5 Rd=1 Rs=1 L	.an
2N5434	Vishay	njf	.model 2N5434 NJF(Beta=18m Betatce=5 Rd=1 Rs=1 Lam	bd
2N5484	Siliconix	njf	.model 2N5484 NJF(Is=.25p Alpha=1e-4 Vk=80 Vto=-1.5 Vto	tc
2N5485	Siliconix	njf	.model 2N5485 NJF(ls=.25p Alpha=1e-4 Vk=80 Vto=-2.0 Vto	tc
2N5486	Siliconix	njf	.model 2N5486 NJF(ls=.25p Alpha=1e-4 Vk=80 Vto=-4.0 Vto	tc
J111	Linear Systems	njf	.model J111 NJF(Beta=2.91m Betatce=-0.5 Vto=-4.047 Vtoto	;=- ∀
<				>

Fig. 3. 2N5432 by Fairchild

Connect the circuit in Fig. 4:



Fig. 4. NJFET testbench

4. Run the system *A*, choose **DC sweep**, pay attention that in this experiment there are two voltage sources. Set their specifications as shown in Fig. 5 and Fig. 6:

🛃 Edit Simulation Com	nmand				×	
Transient AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt		
Compute the DC operat treating capacitan	ing point of a ices as open (circuit w circuits a	hile stepping in Ind inductance	ndependent : es as short ci	sources and ircuits.	
1st Source	ce 2nd Sour	rce 3rd	Source			
Name of 1st source to sweep: VDS						
	Тур	near 🗸				
		0				
		Stop va	ilue:	10		
		Increm	ent:	1		
Syntax: .dc [<oct,dec,lin></oct,dec,lin>) <source1></source1>	<start> «</start>	<stop> [<incr></incr></stop>	•] [<source2></source2>]	
.dc VDS 0 10 1 VGS 0 -4	1					
Car	ncel		(ОК		

Fig. 5. DC analysis specifications for 1st source

<section-header> Edit Sim</section-header>	😕 Edit Simulation Command							
Transient	AC Analysis	Analysis DC sweep Noise DC Transfer DC op pnt						
Compute trea	the DC operat ting capacitan	ing point of a ices as open	circuit w circuits a	hile steppin and inducta	g independe nces as sho	ent source rt circuits.	s and	
	1st Source	ce 2nd Sour	rce 3rd	Source				
	Name	e of 2nd sourc	ce to swe	eep:	VGS			
		Тур	be of swe	eep:	Linear 🗸 🗸	·		
			Start va	alue:	0			
			Stop va	alue:	-4			
			Increm	ient:	1			
Syntax: .do	: [<oct,dec,lin></oct,dec,lin>] <source1></source1>	<start> <</start>	<stop> [<in< td=""><td>cr>] [<sourc< td=""><td>e2>]</td><td></td></sourc<></td></in<></stop>	cr>] [<sourc< td=""><td>e2>]</td><td></td></sourc<>	e2>]		
.dc VDS 0	10 1 VGS 0 -4	1						
	Car	ncel			ОК			

Fig. 6. DC analysis specifications for 2nd source



Place the mouse cursor on drain terminal of the transistor, and you will get the output characteristics of the NJFET, as in Fig. 7:

Now you may proceed to the second part of this experiment, repeat the steps but this time for a P-channel JFET. The steps are repeated in Fig. 8 and beyond.

🥙 Select Comp	onent Sym	ibol			×
Top Directory:	C:\Users\;	araas\OneDriv	e\Documents\	LTspiceXV	II \ib \sym ∨
		P	-Channel JFET Open this mad	r transistoi	r example circuit
f FerriteBead FerriteBead2 g g2 h ind ind2 ISO 16750-2 ISO 7637-2 LED <	load load2 lpnp ltline mesfet nmos nmos4 npn npn2 npn3	e (Documents (P P P P P P P P P S	pn4 ojf omos omos4 onp onp2 onp4 oolcap es es2 schottky	SOA SOA SOA SW tline TVS varz volt zene	Atherm-HeatSink Atherm-NMOS Atherm-PCB diode actor age er
C	ancel			OK	

Fig. 8. P-Channel JFET

🦅 Select J	FET Transistor				×
				ОК	
				Cancel	
Part No.	Manufacturer	Polarity	SPICE Model		^
2N5460	Siliconix	pjf	.model 2N5460 PJF(Is=1.5p Alpha=1e-4 Vk=300 V	/to=-3.4 Vtoto	
2N5461	Siliconix	pjf	.model 2N5461 PJF(ls=1.5p Alpha=1e-4 Vk=300 \	/to=-4.3 Vtoto	
2N5462	Siliconix	pjf	.model 2N5462 PJF(ls=1.5p Alpha=1e-4 Vk=300 V	/to=-5.4 Vtoto	
LSJ74A	Linear Systems	pjf	.model LSJ74A PJF(Beta=38m Betatce=-0.5 Vto=-	.38 Vtotc=-2.	.
LSJ74B	Linear Systems	pjf	.model LSJ74B PJF(Beta(=9m Betatce=-0.5 Vto=-0).84 Vtotc=-2	
LSJ74C	Linear Systems	pjf	.model LSJ74C PJF(Beta=10.6m Betatce=-0.5 Vto	=-1.3 Vtotc≕	.
LSJ74D	Linear Systems	pjf	.model LSJ74D PJF(Beta=9.4m Betatce=-0.5 Vto=	-1.76 Vtotc=	¥
<				>	

Fig. 9. 2N5461 by Siliconix



Fig. 10. PJFET testbench

😰 Edit Simulation Command 🛛 🕹 🗙								
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt								
Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.								
1st Source 2nd Source 3rd Source								
Name of 1st source to sweep: VDS								
Type of sweep: Linear \sim								
Start value: 0								
Stop value: -10								
Increment: 1								
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>								
.dc VDS 0 -10 1 VGS 0 4 1								
Cancel OK								

Fig. 11. DC analysis specifications for 1st source

😕 Edit Simulation Command	×				
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt					
Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.					
1st Source 2nd Source 3rd Source					
Name of 2nd source to sweep: VGS					
Type of sweep: Linear 🗸					
Start value: 0					
Stop value: 4					
Increment: 1					
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>					
.dc VDS 0 -10 1 VGS 0 4 1					
Cancel OK					

Fig. 12. DC analysis specifications for 2nd source

Note how the output characteristics of the P-channel JFET differs from the N-channel JFET, due to the different polarities.



Report requirements:

- 1. Describe the operation of JFET, add graphs and equations to support the statements.
- 2. Connect the circuit in Fig. 14, run transient analysis (set **Stop time** as **0.12m**).



Fig. 14.

Provide a screenshot of the output signal (**Out**), then answer the following questions:

- 1. Which category does this circuit belong to?
- 2. Mention some applications of these circuits.
- 3. Zoom the output signal to see **one period**, then calculate the frequency of the signal (approximately).

Experiment (4) MOSFET Characteristics

Objectives:

The students will analyze MOSFET's IV characteristics using DC sweep analysis in LTspice.

Introduction:

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a type of transistor, which is widely used for switching circuits and in amplifier circuits. MOSFETs are commonly used in integrated circuits, because they can be fabricated in a single chip due to their exceedingly small dimensions/sizes.

Procedure:

- 1. Create a new schematic
- 2. Search for **nmos4** (N-channel MOSFET) as in Fig. 1.

🔊 Select Component Symbol				
Top Directory:	C:\Users\araas\	OneDrive \Documents \		
N-Channel MOSFET transistor with explicit substrate connection(used for monolithic MOSFETS)				
C:\Users\ara	as\OneDrive\Doc	: uments\LTspiceXVII\ib	\sym\	
e e2 f FerriteBead FerriteBead2 g g2 h ind ind2 <	ISO 16750-2 ISO 7637-2 LED load load2 lpnp ltline mesfet njf nmos	nmos4 npn npn2 npn3 npn4 pjf pmos pmos4 pnp pnp2	pnp4 polcap res schottky SOAtherm SOAtherm SOAtherm sw tline	
Can	cel	ОК		

Fig. 1. N-MOSFET in components library

Press OK, right click on the transistor and set the Model Name, Length and Width as in Fig. 2:

Monolithic MOSFET - M1	×
Model Name: N_50	Dn OK
Length(L): 50n	Cancel
Width(W): 500	n
Drain Area(AD):	
Source Area(AS):	
Drain Perimeter(PD):	
Source Perimeter(PS):	
No. Parallel Devices(M):	
N_50n L=50n W=500n	

Fig. 2. Transistor Model Name and Sizes

Connect this circuit in Fig. 3 (this will be your testbench):



Fig. 3. N-MOSFET testbench

Click on SPICE directive "", insert: **.include cmos.txt** as in Fig. 4:

How to netlist this text Justification OK		×
Contribution Cancel Cancel	ext Justification	OK Cancel
O SPICE inc directive Vertical Text Open	Vertical Text	Open Browse

Fig. 4. Including cmos.txt

Run the circuit, set the DC sweep parameters in accordance with Fig. 5 and Fig. 6:

🗗 Edit Simulation Command 🛛 🕹					
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt					
Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.					
1st Source 2nd Source 3rd Source					
Name of 1st source to sweep: VDS					
Type of sweep: Linear ~					
Start value: 0					
Stop value: 1					
Increment:					
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>					
.dc VDS 0 1 VGS 0 1 250m					
Cancel OK					

Fig. 5. DC Analysis (1st Source)

<section-header> Edit Simula</section-header>	ation Command	×			
Transient AC	CAnalysis DC sweep Noise DC Transfer DC op pnt				
Compute the treating	DC operating point of a circuit while stepping independent sources and capacitances as open circuits and inductances as short circuits.				
	1st Source 2nd Source 3rd Source				
	Name of 2nd source to sweep: VGS				
	Type of sweep: Linear 🗸				
	Start value: 0				
	Stop value: 1				
	Increment: 250m				
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>					
.dc VDS 0 1 VGS 0 1 250m					
	Cancel OK				

Fig. 6. DC Analysis (2nd source)

Plot the drain current (Id), your results must look exactly like the curves in Fig. 7.



Now we will repeat the previous procedure for a P-MOSFET transistor, follow these steps carefully:

Search for **pmos4** (p-channel MOSFET) as in Fig. 8.

🍠 Select Comp	onent Symbol			×
Top Directory:	C:\Users\araas\On	eDrive\Docume	ents\LTspiceXVII\lib\sym	\sim
	 ~~	P-Channel M explicit subst monolithic MC	OSFET transistor with rate connection(used fo DSFETS)	r
ا لي		Open this ma	acromodel's example circ	uit
	•	pmos4		
💼 C:\Users\ara	aas\OneDrive\Docum	ents\LTspiceXV	II\ib\sym\	
e e2	ISO16750-2 ISO7637-2	nmos4 npn	pnp4 polcap	
T FerriteBead	load	npn2 npn3	res res2	
FerriteBead2	load2	npn4	schottky	
g 02	lpnp Itline	pj† pmos	SOAtherm-He SOAtherm-NM	ats IOS
h	mesfet	pmos4	SOAtherm-PC	B
ind	njf	pnp	SW	
ind2	nmos	pnp2	tine	
<				>
Ca	ancel		OK	

Fig. 8. P-MOSFET in components library

Press OK, right click on the transistor and set the Model Name, Length and Width as in Fig. 9:

Monolithic MOSFET - M2	2	×
Model Name:	P_1u	ОК
Length(L):	1 u	Cancel
Width(W):	10u	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		
P_1u L=1u W=10u		

Fig. 9. Transistor Model Name and Sizes

Connect this circuit in Fig. 10 (this will be your testbench):



Fig. 10. P-MOSFET testbench

Click on SPICE directive "", insert: .include cmos.txt as in Fig. 11:

Iib/.inc Editor		×
How to netlist this text Comment SPICE Jib directive SPICE inc directive	Justification Left ~ Vertical Text	OK Cancel Open
include cmos.txt		Browse

Fig. 11. Including cmos.txt

Run the circuit, set the DC sweep parameters in accordance with Fig. 12 and Fig. 13:

😕 Edit Simulation Command	×				
Transient AC Analysis DC sweep Noise D	C Transfer DC op pnt				
Compute the DC operating point of a circuit while treating capacitances as open circuits and	stepping independent sources and inductances as short circuits.				
1st Source 2nd Source 3rd So	ource				
Name of 1st source to sweep	v: VSD				
Type of sweep	: Linear V				
Start value					
Stop value	e 5				
Increment					
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>					
.dc VSD 0 5 VSG 0 5 1					
Cancel	ОК				

Fig. 12. DC Analysis (1st Source)

<section-header> Edit Simula</section-header>	tion Comm	and				×	
Transient AC	C Analysis	C sweep No	ise DC	Transfer	DC op pn	t	
Compute the treating	Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.						
	1st Source	2nd Source	3rd Sour	ce		_	
	Name o	f 2nd source to	sweep:	VS	G		
	Type of sweep: Linear V						
Start value: 0							
		Sto	p value:	5	j		
		In	crement:	1			
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>							
.dc VSD 0 5 VSG 0 5 1							
	Cance	el		0	K		

Fig. 13. DC Analysis (2nd source)

Plot the **source current (Is)**, your results must look exactly like the curves in Fig. 14.



Report requirements:

- 1. Describe the operation of MOSFET, include graphs and equations.
- 2. Plot drain current (Id) for the circuit in Fig. 10, how does it differ from the graph in Fig. 14?
- 3. How does the drain current (Id) behave in the body-effect bias circuit in Fig. 15:



Fig. 15. Body-effect bias

Experiment (5) Common Source Amplifier

Objectives:

To understand and experiment the performance of common source amplifier (utilizing a voltage-divider bias).

Introduction:

Common source amplifiers are the most widely used amplifiers due to their highperformance characteristics, compared to other amplifier configurations like common drain (source follower) and common gate. They provide a remarkably high power gain, medium input and output resistance, medium current and voltage gain.

They are called common source because the source terminal is common between the input and the output (the input signal is applied at the gate terminal of the transistor and the output is taken from the drain terminal). The output of common source amplifier is 180° out of phase with the input signal.

Procedure:

- 1. Create a new schematic
- 2. Search for **njf** (N-channel JFET) as in Fig. 1.



Fig. 1. njf in component library

3. Right click on the transistor, pick **Pick New JFET**, then choose the following transistor model 2N5434 as illustrated in Fig. 2.

🍠 Select J	IFET Transistor			×
				OK
				Cancel
Part No.	Manufacturer	Polarity	SPICE Model	^
2N3819	Vishay	njf	.model 2N3819 NJF(Beta=1.304m Betatce=5 Rd	=1 Rs=1 Larr
2N5432	Fairchild	njf	.model 2N5432 NJF(Beta=9.109m Betatce=5 Rd	=1 Rs=1 Larr
2N5434	Vishay	njf	.model 2N5434 NJF(Beta=18m Betatce=5 Rd=1	Rs=1 Lambd
2N5484	Siliconix	njf	.model 2N5484 NJF(ls=.25p Alpha=1e-4 Vk=80 Vt	o=-1.5 Vtotc
2N5485	Siliconix	njf	.model 2N5485 NJF(ls=.25p Alpha=1e-4 Vk=80 Vt	o=-2.0 Vtotc
2N5486	Siliconix	njf	.model 2N5486 NJF(ls=.25p Alpha=1e-4 Vk=80 Vt	o=-4.0 Vtotc
J111	Linear Systems	njf	.model J111 NJF(Beta=2.91m Betatce=-0.5 Vto=-4	.047 Vtotc=- 🗸
<				>

Fig. 2. JFET transistor model

4. Assemble the amplifier circuit in Fig. 3.



Fig. 3. JFET Common Source Amplifier

5. Set the input voltage signal (Vin) parameters in accordance with the specifications mentioned in Fig. 4:

🌮 Independent Voltage Source - Vin	×
Functions (none) PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	DC Value DC value:
EXP(V1 V2 Td1 Tau1 Td2 Tau2) SFFM(Voff Vamp Fcar MDI Fsig) PWL(t1 v1 t2 v2) PWL FILE: Browse	Small signal AC analysis(.AC) AC Amplitude: AC Phase: Make this information visible on schematic: 🗹
DC offset[V]: 0 Amplitude[V]: 0.1 Freq[Hz]: 1k Tdelay[s]: Theta[1/s]: Phi[deg]:	Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: ☑
Ncycles: Additional PWL Points Make this information visible on schematic:	Cancel OK

Fig. 4. JFET Common Source Amplifier

6. Run the circuit by clicking on $\overset{\checkmark}{\sim}$, choose **Transient**, set Stop time: 10m, click OK, then plot the input and output voltage signals.



Report requirements:

- 1. What are the advantages of common source amplifiers over common drain & common gate amplifiers?
- 2. Where are common source amplifiers used? Mention 5 of their applications.
- 3. Plot the frequency response of the amplifier in this experiment (refer to the two figures below), do not forget to set the AC Amplitude as 1.

Include the plot in your report, how much is the gain & phase shift at 10 kHz?

🍠 Independent Voltage Source - Vin	×
Functions (none) PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	DC Value DC value: Make this information visible on schematic: 🗹
O EXP(V1 V2 Td1 Tau1 Td2 Tau2) O SFFM(Voff Vamp Fcar MDI Fsig) O PWL(t1 v1 t2 v2) O PWL FIL F: Browse	Small signal AC analysis(.AC) AC Amplitude: 1 AC Phase: Make this information visible on schematic: 🗹
DC offset[V]: 0 Amplitude[V]: 0.1 Freq[Hz]: 1k	Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: 🗹

Fig. 6. AC Amplitude

Transient	AC Analysis	DC sweep	Noise	DC Transfer	DC op pnt
Compute	the small signal	I AC behavio	r of the c point.	ircuit linearized	about its DC operating
		Type of	sweep:	Decade	\sim
	Number of	of points per (decade:	100	
		Start fre	quency:	1K	
		Stop fre	quency:	1G	

Fig. 7. AC Analysis specifications

Experiment (6) Current Sources

Objectives:

To understand the working principle of current sources and implement a practical current source circuit.

Introduction:

A current source is a circuit that supplies a constant current flow regardless of the impedance that it is driving, the difference between an ideal and a practical current source is illustrated below:



Ideal Current Source

Practical Current Source

Procedure:

1. Search for **nmos** (N-channel MOSFET) as in Fig. 1.



Fig. 1. NMOS transistor

2. Assemble this circuit in Fig. 2, run transient analysis (set Stop time to 1).



Fig. 2. Voltage–Controlled Current Source

Change the input VS source's voltage according to this table and record the current across the load resistor (R_load).

VS	I _{R_load} (mA)	What can you conclude?
0		
0.1		
0.25		
0.5		
0.75		
1		

Report Questions:

- 1. Write some applications of current sources.
- 2. Can current sources be connected in series? Or in parallel? Prove your answer using some circuit diagrams.
- 3. Does the current of a **practical** current source change as load impedance increases? Prove your answer with graphs/equations.

Experiment (7) Current Mirrors

Objectives:

Students will learn how to design basic current mirrors for various applications.

Introduction:

Current mirror is a circuit that copies the current in a device and controls the current in another device by maintaining the output current stable. Current mirrors function as a more practical current source, they are widely used to bias currents to circuits. They come in different forms and complexities, the simplest current mirror circuit uses only two transistors (BJT or FET), as shown below:



Procedure:

1. Add two **nmos4** transistors, mirror the transistor on the left as in Fig. 1.



Fig. 1. NMOS4 transistors

2. Click on SPICE directive "", write: **.include cmos.txt** as in Fig. 2:

Iib/.inc Editor		×
How to netlist this text Comment SPICE Jib directive SPICE inc directive	Justification Left ~ Vertical Text	OK Cancel Open
include cmos.txt		Browse

Fig. 2. Including cmos.txt

- 3. Right click on each of the transistors, set their parameters as illustrated in Fig.
 - 3.

Model Name:	N_1u	OK
Length(L):	2u	Cancel
Width(W):	10u	
Drain Area(AD):		
Source Area(AS):		
Drain Perimeter(PD):		
Source Perimeter(PS):		
No. Parallel Devices(M):		
N_1u I=2u w=10u		



4. Connect the current mirror circuit in Fig. 4:



Fig. 4. A simple MOS current mirror

5. Run DC sweep analysis with the specifications in Fig. 5:

1st Source	2nd Source	3rd Source	æ	
Name of 1st source to sweep:		vo		
	Type of sweep:		Linear	\sim
Start value:		rt value:	100m	
Stop value:		p value:	5	
	Inc	crement:		

Fig. 5. DC analysis



Plot drain currents of both transistors:

The second part of this experiment is about Wilson Current Mirror which is an enhanced circuit configuration designed to provide a more constant current source. Refer to Fig. 7, connect the circuit using the same transistors and voltage sources (you may create copies of them).



Fig. 7. Wilson Current Mirror

Run this circuit with the exact same DC sweep parameters as in the first circuit, Fig. 8 depicts how the drain currents overlay each other (unlike in the previous current mirror).



Report Questions:

- 1. What are some applications of current mirrors?
- 2. Why does Wilson current mirror perform better than a simple current mirror?
- 3. Plot collector currents (IC1 & IC2) of both BJT transistors in the current mirror in Fig. 9, use DC sweep analysis (**Vo** source) from **100m to 5**.



Fig. 9. BJT current mirror

4. For the circuit in Fig. 9, plot the algebraic expression: Ic(Q2) - Ic(Q1)

😕 Expression Editor			×
Default Color: (default) ~	Attached Cursor:	(none)	~ ОК
Enter an algebraic expression to plot:			Cancel
lc(Q2)-lc(Q1)			^
			~
	Delete this Trace		.:

Experiment (8) Differential Amplifiers

Objectives:

To analyze and design simple differential amplifiers.

Introduction:

A differential amplifier (also known as a difference amplifier) is a type of amplifier that has two inputs, it amplifies the difference between two input voltages and rejects any common voltage value to the two inputs. The output voltage of a simple differential amplifier can be expressed as:

 $V_{out} = A \left(V_1 - V_2 \right)$

Where A is the gain of the amplifier.

Differential amplifier is one of the most widely used building blocks in analog integrated-circuit design. It is the input stage of every Operational Amplifier. Two simple differential amplifiers are provided below:



Procedure:

- 1. Add 2 pmos4 transistors and 4 nmos4 transistors.
- 2. Click on SPICE directive ^{.op}, write: **.include cmos.txt** as in Fig. 1:

🗗 .lib/.inc Editor		×
How to netlist this text Comment SPICE .lib directive SPICE .inc directive	Justification Left ~ Vertical Text	OK Cancel Open
include cmos.txt		Browse

Fig. 1. Including cmos.txt

3. Connect the circuit in Fig. 2:



Fig. 2. CMOS Differential Amplifier

Set the transistor parameters as in Fig.3:

Model Name: P_50n	OK	Model Name: N_50n	OK
Length(L): 100n	Cancel	Length(L): 100n	Cancel
Width(W): 5u		Width(W): 2.5u	

Fig. 3. PMOS and NMOS specifications

The lower two transistors (M5 & M6) have a width of 5u instead of 2.5u:

Model Name:	N_50n	OK
Length(L):	100n	Cancel
Width(W):	5u	

Fig. 4. M5 & M6 transistors' specifications

Right click on the voltage sources Vin1 & Vin2, click (Advanced), set their parameters as in Fig. 5 & Fig. 6:

Functions					
(none)	O (none)				
O PULSE(V1 V2 Tdelay Trise Tfall Ton Pe	eriod Ncyc	les)			
● SINE(Voffset Vamp Freq Td Theta Phi I	Ncycles)				
O EXP(V1 V2 Td1 Tau1 Td2 Tau2)					
O SFFM(Voff Vamp Fcar MDI Fsig)					
O PWL(t1 v1 t2 v2)					
O PWL FILE:		Browse			
DC offset[V]:	500m				
Amplitude[V]:	5m				
Freq[Hz]: 1k					
Tdelay[s]:					
Theta[1/s]:					
Phi[deg]:					
Ncycles:					

Fig. 5. Input voltage (Vin1)

Functions					
O (none)					
O PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)					
SINE(Voffset Vamp Freq Td Theta Phi Ncycles)					
O EXP(V1 V2 Td1 Tau1 Td2 Tau2)					
◯ SFFM(Voff Vamp Fcar MDI Fsig)					
O PWL(t1 v1 t2 v2)					
O PWL FILE: Browse					
DC offset[V]:	500m				
Amplitude[V]:	5m				
Freq[Hz]:	1k				
Tdelay[s]:	0				
Theta[1/s]: 0					
Phi[deg]: 180					
Ncycles:					

Fig. 6. Input voltage (Vin2)

Note that the signals are out of phase by 180 degrees.

Run transient analysis, set Stop time (10m), plot **Vin1**, **Vin2** & **Vout** as illustrated in Fig. 7:



Report Questions:

- 1. Where are differential amplifiers used?
- 2. Modify the input voltages, set their phases to zero, what does the output voltage look like? Include its plot in the report.
- 3. Run DC sweep analysis (refer to Fig. 8) for the output voltage (Vout), include the plot in the report.

🗗 Edit Simulation Command 🛛 🕹 🗙					
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt					
Compute the DC operating point of a circuit while stepping independent sources and treating capacitances as open circuits and inductances as short circuits.					
1st Source 2nd Source 3rd Source					
Name of 1st source to sweep: Vin1					
Type of sweep: Linear ~					
Start value: 0					
Stop value: 1					
Increment: 0.05					
Syntax: .dc [<oct,dec,lin>] <source1> <start> <stop> [<incr>] [<source2>]</source2></incr></stop></start></source1></oct,dec,lin>					
.dc Vin1 0 1 0.05					
Cancel OK					

Fig. 8. DC sweep parameters

Experiment (9) Power Amplifiers

Objectives:

To study the major aspects of class C power amplifier and learn how to plot FFT of signals in LTspice.

Introduction:

A power amplifier is an electronic amplifier designed to increase the magnitude of power of a given input signal. The power of the input signal is increased to a level high enough to drive loads of output devices like speakers, headphones, RF transmitters etc. Unlike voltage and current amplifiers, a power amplifier is designed to drive loads directly and is used as a final block in an amplifier chain.

Procedure:

1. Insert one BJT (npn) transistor, as in Fig. 1.

🌮 Select Component Symbol 🛛 🕹 🗙				
Top Directory:	C:\Users\araas\OneDrive\Documents' ~			
	Bipolar NPN transistor			
۳,		ו this macromodel's example c		
C: \Users \araas \OneDrive \Documents \LTspiceXVII \ib \syi				
ISO16750-2	Itline	npn2		
ISO/63/-2	mestet	npn3		
load	nmos	pif		
load2	nmos4	pmos		
lpnp	npn	pmos4		
<		>		
Cancel		ОК		

Fig. 1. npn transistor

2. Right click on the transistor, choose (2N3055) model as shown in Fig. 2:

🌮 Select Bipolar Transistor 🛛 🕹					
					ОК
					Cancel
Part No.	Manufacturer	Polarity	Vceo[V]	Ic[mA]	SPICE Model
2N4401	Fairchild	npn	40.0	600	.model 2N4401 NPN(ls=26.03
2N5550	Fairchild	npn	150.0	600	.model 2N5550 NPN(ls=2.511
2N2369	NXP	npn	15.0	200	.model 2N2369 NPN(ls=44.14
2N5769	Fairchild	npn	15.0	200	.model 2N5769 NPN(ls=44.14
2N3055	STMicro	npn	60.0	10000	.model 2N3055 NPN(Bf=73 B
BCW60A	Rohm	npn	32.0	200	.model BCW60A NPN(IS=20f
BCW60B	Rohm	npn	32.0	200	.model BCW60B NPN(IS=20f
<	.		22.0	200	

Fig. 2. Picking the power transistor model

3. Connect the class C power amplifier in Fig. 3:



Fig. 3. Class C power amplifier circuit

The resonant frequency of the given class C amplifier is determined by the inductor (L) and capacitor's (C) values, the parallel LC circuit is commonly known as the tank circuit (see Fig. 4).



Fig. 4. The tank circuit

Class C amplifiers only amplify the signals that have a frequency equal to the resonant frequency, they attenuate other signals having different frequencies. In our case, the resonant frequency is equal to 5.03 KHz which is calculated by the following formula:

$$F_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.001 * 0.000001}} = 5.03 \text{ KHz}$$

Set the VCC voltage value as 30, and Vin voltage in accordance with the specifications mentioned in Fig. 5, label the input and output pins.

📁 Independent Voltage Source - Vin	×
Functions (none) PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles)	DC value:
 O EXP(V1 V2 Td1 Tau1 Td2 Tau2) O SFFM(Voff Vamp Fcar MDI Fsig) O PWL(t1 v1 t2 v2) O PWL FILE: 	Small signal AC analysis(.AC) AC Amplitude: AC Phase: Make this information visible on schematic: 🗹
DC offset[V]: 0 Amplitude[V]: 3 Freq[Hz]: 5.03K Tdelay[s]: Theta[1/s]: Phi[deg]: Ncycles:	Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: ☑
Additional PWL Points Make this information visible on schematic:	Cancel OK

Fig. 5. Vin (sine wave) parameters

Run transient analysis, set stop time as 5m, plot the input and output signals as illustrated in Fig. 6:



4. Right click on the Vin, set the frequency to **0.5 KHz**, run the simulation again to see the output, you will observe that the output is less than the input as seen in Fig. 7, because the amplifier attenuates the signal as the frequency of the input signal is not equal to resonant frequency (5.03 KHz).



For the part two of this experiment, add two other sine wave sources, connect them in series, as shown in Fig. 8:



Fig. 8. Voltage sources in series

Set their values in accordance with the table below,

Source name	Amplitude (V)	Frequency
Vin	3	ЗК
Vin1	5	7K
Vin2	7	5.03K

Run transient analysis, set stop time as 5m, plot the input and output signals as in Fig. 9:



The output signal in Fig. 9 has a frequency of 5.03 KHz, the other two signals with frequencies of 3 KHz and 7 KHz are omitted, this can be seen more clearly by taking the Fast Fourier Transform (FFT) of the input and output signals, this can be done easily by **right clicking** on the plot then selecting **view > FFT > Click OK** (see Fig. 10).





Fig. 11 shows the FFT of the input and the output signal, the FFT of the input signal has 3 main beams (at 3 KHz, 5 KHz and 7 KHz), while the FFT of the output signal has only one main beam at 5 KHz, this indicates that the class C amplifier neglects other signals with frequencies different than the resonant frequency.



Fig. 11. FFT of the input and the output signal

Report Questions:

- 1. What does 2N3055 transistor look like? Add its picture and explain why we used this transistor for this experiment?
- 2. What is a heat sink? What is it used for?
- 3. A tuned class C amplifier has a resonant frequency of 1 MHz, the capacitor is 10 uF, an inductor of which value should be used?

Experiment (10) Operational Amplifiers

Objectives:

To study the fundamental structure of CMOS operational amplifiers.

Introduction:

An operational amplifier (op-amp) is a type of amplifier that amplifies the voltage difference between the two input pins, op-amps usually have three terminals: two high-impedance inputs and a low-impedance output (although some op-amps have an additional differential output). The inverting input is denoted with a minus (-) sign, and the non-inverting input denoted with a positive (+) sign. Operational amplifiers have an extremely high gain, they are used in various analog circuits including mixers, filters, sensors, buffers, etc.



Most op amps are used for voltage amplification, however there are four categories of op-amps:

- 1. Voltage amplifiers (voltage input, voltage output)
- 2. Current amplifiers (current input, current output)
- 3. Transconductance amplifiers convert a voltage input to a current output.
- 4. Transimpedance amplifiers convert a current input to a voltage output.

Procedure:

- 1. Add 3 pmos4 transistors and 6 nmos4 transistors.
- 2. Click on SPICE directive ^{.op} , write: **.include cmos.txt**

3. Connect the op-amp circuit in Fig. 1:



Fig. 1. CMOS operational amplifier

- 4. Carefully modify the transistors' widths and lengths according to the circuit diagram in Fig. 1, do not forget to connect Grounds and VDDs.
- 5. The input voltage source (Vin) has such parameters:

O (none)						
O PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles)						
 SINE(Voffset Vamp Freq Td Theta Phi Ncycles) 						
O EXP(V1 V2 Td1 Tau1 Td2 Tau2)						
◯ SFFM(Voff Vamp Fcar MDI Fsig)						
O PWL(t1 v1 t2 v2)						
O PWL FILE: Browse						
DC offset[V]:	500m					
Amplitude[V]:	1m					
Freq[Hz]:	1k					
Tdelay[s]:						
Theta[1/s]:						
Phi[deg]:						
Ncycles:						

Fig. 2. Vin parameters

- 6. Add three DC voltage sources, label them as VDD, Bias1 and Bias2 as shown in Fig. 3. Their values are as following:
 - VB2 = 361 m
 - VB1 = 543 m
 - VDD = 1



Fig. 3. Bias voltages and VDD

7. Run transient analysis (Stop time = 10m).



- 8. We can also plot the frequency response of the op-amp, close the waveform, then change the parameters of the input voltage source (Vin) as in Fig. 5.
- 9. Press OK.
- 10.Run AC analysis for the output voltage (Vout) in accordance with the specifications mentioned in Fig. 6.

🌮 Independent Voltage Source - Vin	×
Functions Image: PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles) EXP(V1 V2 Td1 Tau1 Td2 Tau2) SFFM(Voff Vamp Fcar MDI Fsig) PWL(t1 v1 t2 v2) PWL FILE:	DC Value DC value: 500m Make this information visible on schematic: ✓ Small signal AC analysis(.AC) AC Amplitude: 1 AC Phase: Make this information visible on schematic: ✓ Parasitic Properties Series Resistance[O]:
Additional PWL Points Make this information visible on schematic:	Parallel Capacitance[F]: Make this information visible on schematic:

Fig. 5. Adjusting input voltage source for the AC analysis

<section-header> Edit Simulation Command</section-header>				×
Transient AC Analysis DC sweep	Noise	DC Transfer	DC op pnt	
Compute the small signal AC behavior of the circuit linearized about its DC operating point.				
Туре	of sweep:	Decade	\sim	
Number of points pe	r decade:	100		
Start fr	equency:	1k		
Stop fr	equency:	1G		
Syntax: .ac <oct, dec,="" lin=""> <npoints> <startfreq> <endfreq></endfreq></startfreq></npoints></oct,>				
.ac dec 100 1k 1G				
Cancel		0	К	

Fig. 6. AC analysis command



Report Requirements:

- 1. Calculate the voltage gain of the op-amp at 1 kHz frequency.
- 2. At which frequency does the op-amp has a unity gain?
- 3. Plot the input and output voltage signals when the input signal has the following parameters, what do you notice?

SINE(Voffset Vamp Freq Td Theta Phi I	Vcycles)				
○ EXP(V1 V2 Td1 Tau1 Td2 Tau2)					
◯ SFFM(Voff Vamp Fcar MDI Fsig)					
○ PWL(t1 v1 t2 v2)					
O PWL FILE:		Browse			
DC offset[V]:	500m]			
Amplitude[V]:	1m]			
Freq[Hz]:	400MEG]			
Tdelay[s]:]			
Theta[1/s]:]			
Phi[deg]:					
Ncycles:					

4. Repeat the previous step for these parameters, what will the output signal look like and why?

