Comparative Analysis of Neuromorphic Vision Chips: Future Prospects for Reconfigurable 3D LSI Technology

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***Abstract*—The following article provides an overview of the advancements made in the research of neuromorphic vision processors over the past few decades. It mainly focuses on two types of vision processors: frame-based (FB) and event-based (EB) vision processors. These two types differ in system architecture, image sensing techniques, image coding, image processing algorithms, and design methodologies. Neuromorphic vision processors have the ability to overcome the processing and transmission bottlenecks that limit traditional image processing systems. They can perform high-speed image capture and real-time image processing operations. This review paper introduces two representative vision processors, one from each category, to explain their architectures, image sensing schemes, image processing processors, and system operations. The FB neuromorphic reconfigurable vision processor includes a high-speed image sensor, a processing element array, and a self-organizing map neural network. The FB vision processor has advantages in high-resolution imaging, static object detection, time-multiplex image processing, and a smaller chip area. The EB neuromorphic vision processor system utilizes an event-driven multi-kernel convolution network and an address-event-representation image sensor. The EB vision processor has advantages in fast sensing, low communication bandwidth, brain-inspired processing, and high energy efficiency. Finally, this article discusses the architecture and challenges of future neuromorphic vision processors, highlighting the trend towards developing reconfigurable vision processors that integrate left- and right-brain functions using three-dimensional large-scale integrated circuit (LSI) technology.**

I. Introduction

We provide an overview of the advancements made in the research of neuromorphic vision processors over the past few decades. It mainly focuses on two types of vision processors: frame-based (FB) and event-based (EB) vision processors. These two types differ in system architecture, image sensing techniques, image coding, image processing algorithms, and design methodologies. Neuromorphic vision processors have the ability to overcome the processing and transmission bottlenecks that limit traditional image processing systems. They can perform high-speed image capture and real-time image processing operations. This review paper introduces two representative vision processors, one from each category, to explain their architectures, image sensing schemes, image processing processors, and system operations. The FB neuromorphic reconfigurable vision processor includes a high-speed image sensor, a processing element array, and a self-organizing map neural network. The FB vision processor has advantages in high-resolution imaging, static object detection, time-multiplex image processing, and a smaller chip area. The EB neuromorphic vision processor system utilizes an event-driven multi-kernel convolution network and an address-event-representation image sensor. The EB vision processor has advantages in fast sensing, low communication bandwidth, brain-inspired processing, and high energy efficiency. Finally, this article discusses the architecture and challenges of future neuromorphic vision processors, highlighting the trend towards developing reconfigurable vision processors that integrate left- and right-brain functions using three-dimensional large-scale integrated circuit (LSI) technology. The concept of neuromorphic vision chips involves integrating an image sensor and brain-inspired parallel processors on a single silicon die. The system mimics the human visual system by having the image sensor act as the retina and the processors function as the brain's visual cortex. The image sensor captures the image data, while the processors perform intelligent image processing in parallel and output the result. Compared to traditional image processing systems, neuromorphic vision chips overcome serial data transmission and processing bottlenecks. They can perform image processing at high speeds of over 1000 frames per second, making them ideal for edge-computing applications that require quick response times and reduced communications bandwidth.

This technology has many potential applications, including security monitoring, blind navigation, robotic vision, industry automation, visual object tracking, entertainment, and virtual reality/augmented reality. Using a single vision chip, the combination of an image sensor, transmission line, and powerful computer can be replaced, thereby reducing power consumption, size, and cost. Researchers have been focused on developing neuromorphic vision chips for nearly two decades, making significant progress. However, there are still research challenges to overcome, such as chip architecture, photonic/microelectronic hybrid design, high-speed brain-inspired neural networks, fabrication technology, and online training algorithms. This review paper will summarize recent progress and research challenges related to both frame-driven (FD) and event-driven (ED) neuromorphic vision chips. Section 2 provides a brief summary of the research progress on both FD and ED vision chips, followed by examples of typical research results of FD and ED vision chips in Sections 3 and 4,

respectively. Finally, Section 5 discusses the architecture and challenges of future neuromorphic vision chips.

The convolution kernels on the chips are well tuned through Researchers have been working on neuromorphic vision chips for about 20 years and have achieved significant progress. These chips integrate an image sensor and brain-inspired processors on a single silicon die, with the sensor acting as the retina and the processors as the visual cortex. The processors perform intelligent image processing in parallel, enabling image processing at a speed of over 1000 frames per second and reducing the need for communications bandwidth between the sensor and central data center. As a result, the power consumption, size, and cost of the visual system are significantly reduced, making it suitable for various applications, such as security monitoring, blind navigation, robotic vision, industry automation, visual object tracking, entertainment, and virtual reality/augmented reality.

However, there are still many research challenges in chip architecture, photonic/microelectronic hybrid design, high-speed brain-inspired neural networks, fabrication technology, and online training algorithms. For example, the reported chips only implement a single-kernel convolution and feature extraction, making it difficult to carry out object recognition. Moreover, they suffer from device mismatch and low computing precision due to weighted event integration by analog charge packet integration on pixel capacitors and computing circuits.

To address these issues, a fully-digital convolutional neural network chip was developed for event-driven vision sensing and processing systems. This chip can perform the operation of kernels with arbitrary programmable shape and size up to 32x32, handle the forgetting mechanism, and distinguish between multiple simultaneous input flows. An intermediate solution involves training a frame-driven convolutional neural network using an image frame database and applying the learned parameters to an event-driven network. Another approach involves using a leaky integrate-and-fire spiking neural network to extract cortex-like features and classify different patterns. A multi-kernel convolution processing module chip was also proposed, which can handle the leak/forgetting mechanism and process different kernel convolutions in parallel for multiple input flows. These modules can be assembled to set up a hierarchical feed-forward convolutional neural network for complete event-driven vision processing. Additionally, an event-driven image recognition system with a multiple-orientation detector for objects was proposed, which can extract features, track objects, and recognize patterns with arbitrary motion orientation.

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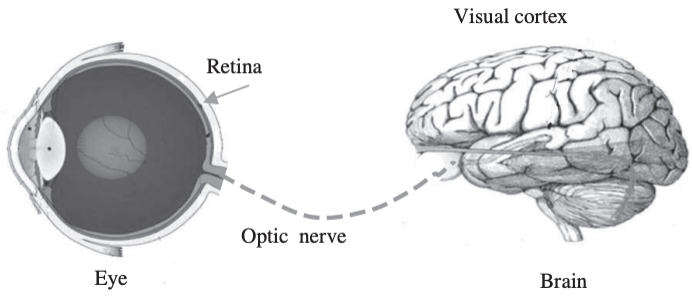

Fig. 1: Schematic figure of the Visual System.

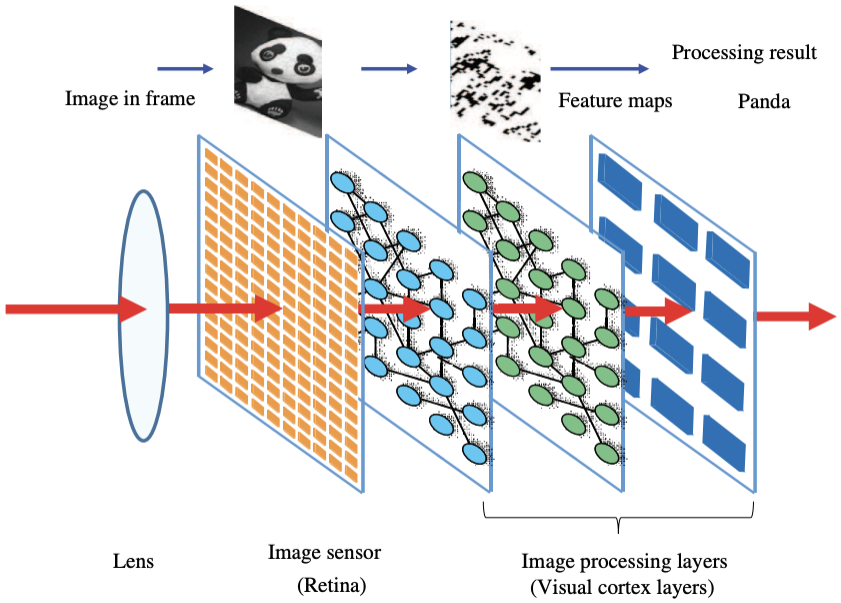

Fig. 2: FD vision chip.

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To achieve this, a novel vision chip architecture with left and right brain-inspired functions can be developed. The architecture comprises processors for left-brain and right-brain functions, where the former consists of an array of von Neumann-type processing cores and the latter is a neural network processor. The two processors can be reconfigured using circuit techniques. The novel vision chip can recognize visual features and estimate visual feature information for various

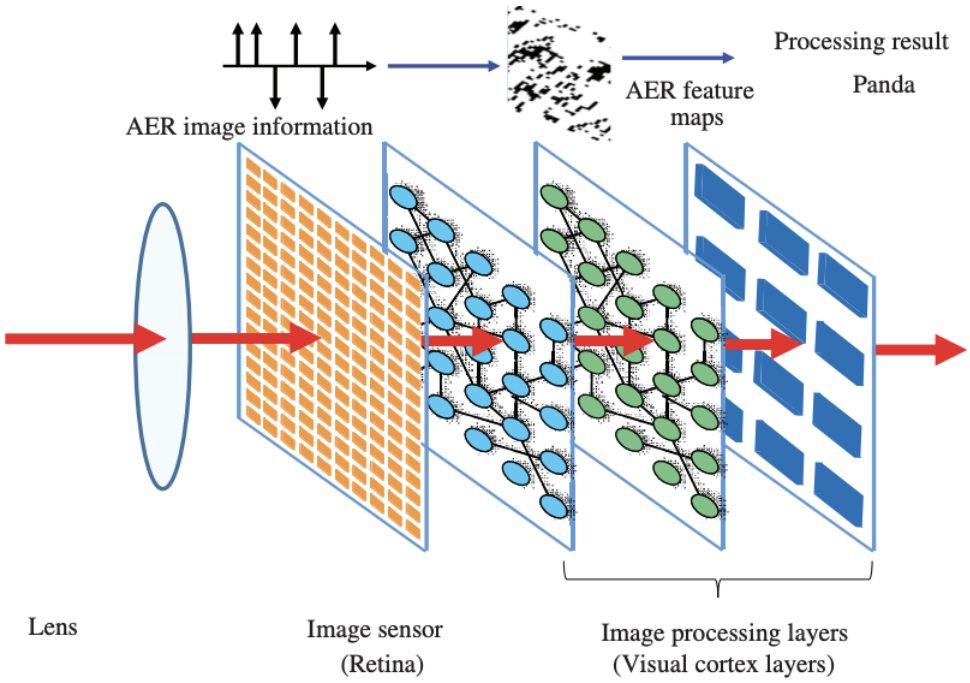

Fig. 3: ED Vision Chip.

applications using the left and right brain processors, respectively. However, integrating the imager and image processor on a single Silicon die in conventional 2D LSI technology is difficult due to the mismatch in process nodes. Hence, a 3D integrated circuit chip with different layers implemented using different semiconductor processes can be used. The trend in neuromorphic vision chip research is towards 3D integrated circuits.

II. Conclusion

The neuromorphic vision chip is an edge-computing device that processes data near the source, leading to improved performance and data security due to reduced network transfers. Unlike data center-oriented neuromorphic computing chips, it must be smaller, consume less power, and be cost-effective. Its application is limited to specific scenes, but it can be retrained for new ones. Developing a real-time, large-scale brain-inspired processor with high processing speed and energy efficiency is a significant challenge in future neuromorphic vision chip technology.

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References

[1] C. Zamarre˜no-Ramos, L.A. Camu˜nas-Mesa, J.A. P´erez-Carrasco, T. Masquelier, T. SerranoGotarredona, and B. Linares-Barranco. On spike-timing-dependent-plasticity, memristive devices, and building a self-learning visual cortex. Frontiers in neuroscience, 5, 2011. 4, 7

[2] K. Rajitha, et al. "Estimation of the Cardiac Pulse from Facial Video in Realistic Conditions," ICAART, 2019.

[3] Park, H.L., Kim, M.H., Kim, M.H. and Lee, S.H., 2020. Reliable organic memristors for neuromorphic computing by predefining a localized ion-migration path in crosslinkable polymer. Nanoscale, 12(44), pp.22502-22510.

[4] Subramaniam, A. and Sharma, A., 2019. N2NSkip: Learning Highly Sparse Networks using Neuron-to-Neuron Skip Connections.

[5] Rajamani, V., Kim, H., & Chua, L. O. (2018). Morris-Lecar model of third-order barnacle muscle fiber is made of volatile memristors. Sci. China Inf. Sci., 61(6), 060426-1.

[6] Fouda, M.E., Kurdahi, F., Eltawil, A. and Neftci, E., 2020. Spiking neural networks for inference and learning: A memristor-based design perspective. Memristive Devices for Brain-Inspired Computing, pp.499-530.

[7] Yang K, Joshua Yang J, Huang R, Yang Y. Nonlinearity in Memristors for Neuromorphic Dynamic Systems. Small Science. 2022 Jan;2(1):2100049.

[8] Rajitha, et al. (2019, September). Spectral reflectance based heart rate measurement from facial video. In 2019 IEEE International Conference on Image Processing (ICIP) (pp. 3362-3366). IEEE.

[9] Liu C, Hu M, Strachan JP, Li H. Rescuing memristor-based neuromorphic design with high defects. In2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC) 2017 Jun 18 (pp. 1-6). IEEE.

[10] Subramaniam, Arvind. "A neuromorphic approach to image processing and machine vision," 2017 Fourth International Conference on Image Information Processing (ICIIP). IEEE, 2017

[11] Martins, Raquel Azevedo, Emanuel Carlos, Jonas Deuermeier, Maria Elias Pereira, Rodrigo Martins, Elvira Fortunato, and Asal Kiazadeh. "Emergent solution based IGZO memristor towards neuromorphic applications." Journal of Materials Chemistry C 10, no. 6 (2022): 1991-1998.