Percolation Nature of Threshold Switching: An Experimental Verification

Suman Devkota, Brendan M Kuzior, Victor Karpov, Daniel Georgiev, Frank Li, and Vamsi Borra

Abstract— **This paper details the process involved to create an interconnect in a conductivity system, such as amorphous and polycrystalline semiconductors. Moreover, an experimental verification on the plasticity, that support the percolation conduction mechanism, was detailed. The plasticity observed in the sample could be harnessed in the development of new electronic devices that require flexibility and adaptability, such as wearable electronics and bendable screens. Overall, the TEM characterization, in combination with SAED analysis, revealed a highly oriented crystalline structure in the sample. In addition, the results of this study may have implications for the design of new memory devices that are based on percolation conduction mechanisms, which could potentially lead to the development of more efficient and reliable non-volatile storage technologies.**

I. Introduction

Interconnection plays an important role in the Very Large-Scale Integration (VLSI) [1] by enabling different systems to influence each other. The conductive path enables the interconnection of nodes. However, the conventional artificial interconnection technique has shortcomings such as degradation and high cost, attempts have been made to address such issues. Recent findings [2] introduced a novel architecture, with a potential for gigantic multi-valued memory systems, that may be applicable to neuromorphic computing. This is achieved through percolation conductivity systems, such as amorphous and polycrystalline semiconductors, metal oxides, or granular metals. These architectures do not require conventional memory cells and interconnects. They have suggested that percolation conduction is efficient to establish interconnection in between dielectric gaps, as it creates conductive filament due to electric bias.

The primary mechanism underlying this phenomenon is understood to be the processes of non-ohmic percolation conduction in classical non-crystalline materials. According to the original proposal[3], the Poole-Frenkel percolation non-ohmicity is caused by modifications of exponentially random microscopic resistors forming the bonds of a percolation cluster induced by bias. This principal understanding was recently reaffirmed [4]. Our recent findings also suggest that the threshold switching method [5]–[8], which is a subset of percolation conduction, can help establish interconnection in thin-film photovoltaics by creating a conductive pathway[9]. Additionally, in older generation materials, microscopic resistors could be fully recovered after the bias-induced modifications were removed. However, recent studies[4], [5], [10]–[13] have introduced a significant new finding by highlighting the existence of enduring resistor modifications that can serve as non-volatile records in materials with plasticity. These materials include modern non-volatile storages like RRAM and PCRAM, which rely on such modifications to store data.

As the theory suggests, percolation conduction is achieved using disordered materials such as doped semiconductors of P and N-type used in our study [14], [15]. Such conducting materials should also exhibit plasticity. For instance, metal oxide, like transparent metal oxide used in our study, that uses resistive random-access memory (RRAM) and phase change memory (PCM) [16]. The dielectric gap can be bridged using conductive filament, which is a commonly recognized mechanism for plasticity. The creation of conductive filament is achieved by the response of electric bias [9]. Thus, our study uses material that can exhibit percolation conduction and plasticity.

II. Methodology

Here, in this study we attempt to further validate the percolation conduction theory, by substantiating with experimental verification and analytical characterization techniques, that confirm the formation of interconnection, which we attribute to percolation conduction. A potential to generate conductive filament that in turn forms direct connectivity between bond-forming microscopic resistors could possibly eliminate the need of artificial interconnects.

The Current-Voltage (IV) Characterization experiments were performed using a micromanipulator probe station. This probe station was used to apply DC voltage to the sample, the setup is illustrated in Figure 1. The DC Power Supply's positive terminal was connected to the sample via the micromanipulator probe. For this case, we utilized a thin-film Cadmium Telluride (CdTe) for the experiment.

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The probe was connected to the front electrode of the sample, which is connected to the P-Type CdTe. The back electrode is connected to the N-Type CdS material. From here, the sample was then connected to a Digital Multimeter (DMM) in series to measure the current. The DMM was then connected to the DC Power Supply's negative terminal. With this setup, the IV curves of the sample could be measured to determine the characteristics. The sample preparation can be found in our prior publication [3].

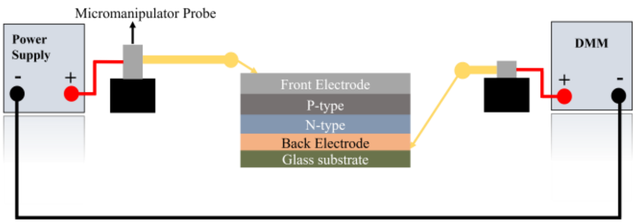

Figure 1. Experimental setup of the test station.

Following the electrical testing, the samples underwent analytical characterization. The characterization was performed in two folds. First, a JOEL Scanning Electron Microscope (SEM) with Focal-Ion Beam (FIB) was used to prepare a lamella. Then, the lamella was studied under a JOEL Transmission Electron Microscope (TEM).

Figure 2(a) shows the Carbon protective layer (shown with red arrow) deposited by the FIB induced deposition (FIBID) technique to protect the sample under study. In addition, two deep rectangular trenches are visible next to the protective layer that assist with the lift-out process. In addition, Fig. 2(a) shows an in-situ nano-manipulator, an omni probe with nominal thickness of 35 µm and nominal post downset of 5 µm, that assists in sample liftoff and attaching it to the TEM grid.

In Figure 2 (b), a side view of the sample attached to the TEM grid is shown. In this image, the top protective carbon layer and the undamaged sample is shown. The FIB thinning process was then carried out on the sample to make it electron transparent for TEM analysis. We have thinned the specimen to ~100nm, as shown in Fig. 2(c). After thinning, different layers in the sample are clearly visible in Fig. 2(c). Also, in Fig. 2(c), the stack consisting of Cadmium telluride (CdTe), Cadmium Sulfide (CdS), transparent conducting oxide (TCO), and glass substrate are labelled. In addition, as expected for this particular sample, a thin layer of Chromium (Cr) is found on top of CdTe and below the protective Carbon layer. The thickness of each layer was recorded during the characterization process.

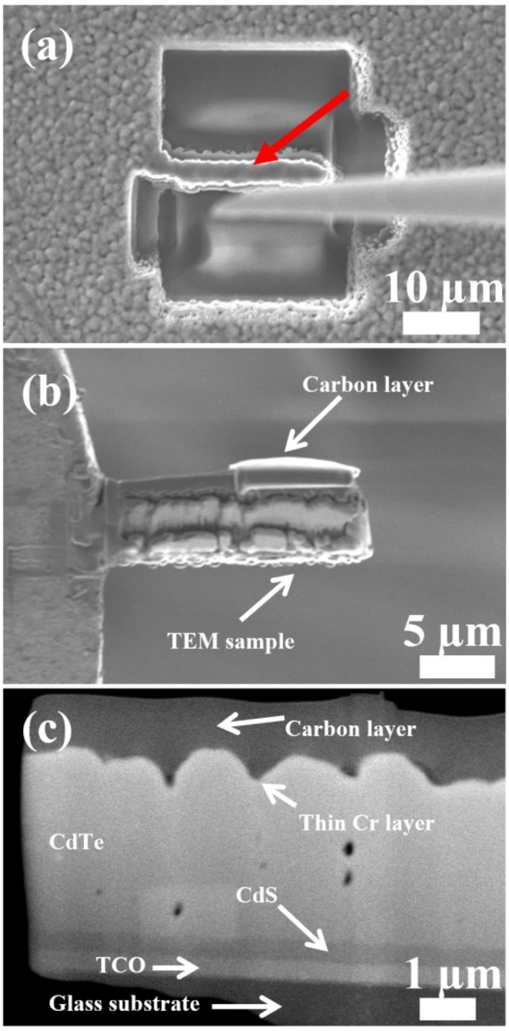

Figure 2. SEM-FIB to prepare sectional sample.(a) Sample during the liftoff process. (b) Side view of the sample attached to TEM grid (befire thinning). (c) Side view of the sample after thinning to ~100nm thickness.

III. Results

This section will detail the I-V characteristics and TEM studies, along with Selected-Area Electron Diffraction (SAED).

A. *I-V characteristics*

The overall I-V characteristics of the sample under study resulted in a non ohmic measurements, which align with the fundamental mechanism the explain the processes of non-ohmic percolation conduction. It is worth noting that even voltages in the range of 6–8 V can create an extremely strong electric field in a nano-sized region over time, which ultimately overcomes the conductivity barrier and leads to non-ohmic behavior. Our study, which observes the I-V characteristics curve over time, provides evidence of a conducting path that has been created through the stack of thin-film layers. The non-ohmic characteristics changed into ohmic, which suggests that a conducting path, with plasticity, was created across the sample. Figure 3 shows the characteristics curve observed at the same point after 2, 4, 6, 12, and 24 hours. Initially, a rapid change in current was observed after crossing 6 V and a current of 0.1 A was recorded at 7 V. All the experimental readings taken at the same point after several hours resulted in ohmic characteristic curve, as shown in Figure 3, which imply the creation of a conducting path after exceeding the threshold voltage. We attribute the formation of the percolation conduction to the polycrystalline semiconductor, which was verified by the TEM analysis for our samples. Moreover, the time-lapse I-V curves indicate the presence of a commonly recognized plasticity mechanism in the sample.

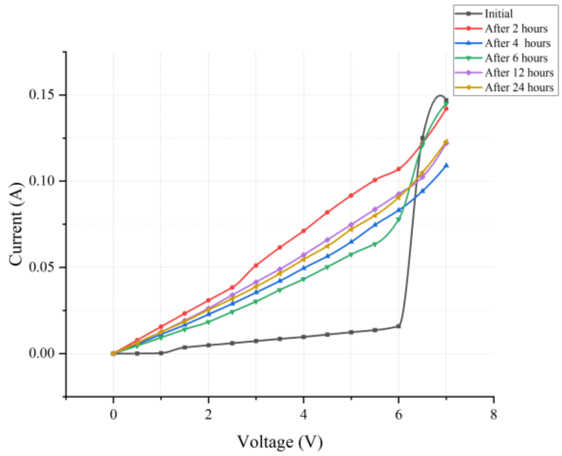

Figure 3. I-V Characteristics observed over a period.

Table I shows the experimental data of the I-V characterization experiments recorded at a sample spot for several iterations. The graphical image shown in Figure 3 represents the data displayed in the table.

As observed from Table I, the initially recorded data show the non-ohmic nature of the characteristic curve of the sample. However, the data recorded at the same point after the initial current ramp at 6.5 V indicates the formation of a conducting path, which changes the non-ohmic nature of the characteristic curve to ohmic, as represented by almost a linear line, as shown in the figure. All the subsequent time-lapse I-V curves validate the plasticity nature of the sample as shown in Figure 3. It is important to note that all of the subsequent time-lapse I-V curves demonstrate the plasticity nature of the sample, as can be seen in Figure 3. This provides further evidence that the percolation conduction observed in our study is indeed due to the polycrystalline nature of the sample. As noted, plasticity mechanism is a phenomenon where the material exhibits a time-dependent change in its resistance under a constant voltage or current. This is usually attributed to the rearrangement of the material's microstructure, such as the movement of dislocations, vacancies or other defects, resulting in a change in the material's electrical properties. The plasticity observed in our samples further supports the percolation conduction mechanism proposed in our study.

B. *Transmission Electron Microscopy*

Figures 4(a) and 4(b) demonstrate that the TEM analysis revealed a polycrystalline structure of the sample. The CdTe layer, which was measured to be approximately 5 µm, exhibited large grains throughout the sample. Furthermore, the SAED analysis shown in Fig. 4(d) indicates a polycrystalline structure consisting of relatively well-aligned crystalline grains. These findings strongly suggest that the sample is crystalline or polycrystalline in nature. Furthermore, the 0.3 µm CdS layer was found to be polycrystalline in nature, as observed in the magnified images shown in Figure 4(c) and 4(d). Figure 4(c) also highlights the well-oriented CdS grains stacked on TCO, which is deposited on a glass substrate.

TABLE I. I-V CHARACTERISTICS OF A SAMPLE USED

Voltag e (V)	**Current in Ampere**					
	Initial	***2 hours***	***4 hours***	***6 hours***	***12 hours***	***24 hours***
0	0	0	0	0	0	0
0.5	3.28E-05	7.79E-03	4.91E-03	4.50E-03	4.70E-03	2.67E-03
1	2.37E-04	1.56E-02	9.93E-03	9.22E-03	9.57E-03	5.54E-03
1.5	3.58E-03	2.32E-02	1.51E-02	1.41E-02	1.45E-02	8.65E-03
2	4.80E-03	3.09E-02	2.04E-02	1.84E-02	1.99E-02	1.20E-02
2.5	6.03E-03	3.83E-02	2.59E-02	2.42E-02	2.54E-02	1.54E-02
3	7.28E-03	5.11E-02	3.17E-02	3.02E-02	3.13E-02	1.90E-02
3.5	8.50E-03	6.15E-02	3.75E-02	3.69E-02	3.74E-02	2.35E-02
4	9.64E-03	7.12E-02	4.31E-02	4.32E-02	4.39E-02	2.73E-02
4.5	1.10E-02	8.18E-02	4.95E-02	5.02E-02	5.04E-02	3.20E-02
5	1.24E-02	9.16E-02	8.18E-02	5.74E-02	5.77E-02	3.82E-02
5.5	1.36E-02	1.01E-01	9.28E-02	6.35E-02	6.40E-02	4.68E-02
6	1.59E-02	1.07E-01	1.01E-01	7.78E-02	7.25E-02	1.06E-01
6.5	1.25E-01	1.22E-01	1.25E-01	1.21E-01	1.02E-01	1.23E-01
7	1.47E-01	1.42E-01	1.33E-01	1.45E-01	1.27E-01	1.47E-01

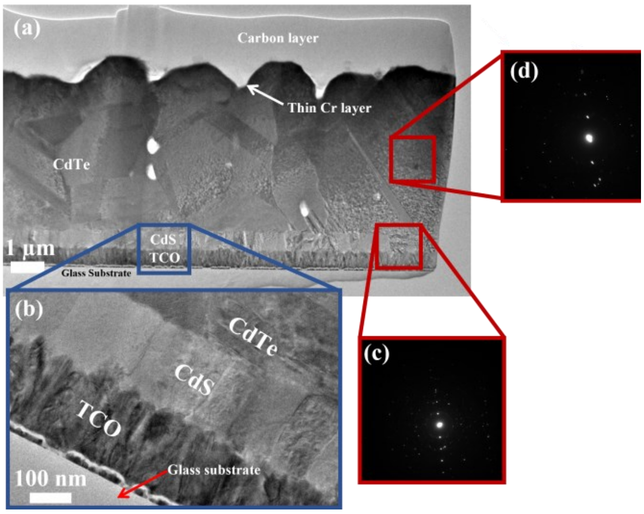

Figure 4. a) TEM image of a sample representing different layers. b) Magnified image of the n-type material followed by TCO. c) SAED pattern confirming highly oriented crystalline structure.

Figure 5 is a representative image of the electrically conductive percolation path formed across the sample, which connects the two leads. As described previously, this conductive path allows the electric current to flow in the percolation cluster, which exhibit natural random connectivity. While this appears to contradict the standard paradigm of chain-like or more sophisticated regular wiring patterns found in existing architectures, it should be noted that artificial randomly wired neural networks have recently gained interest for their ability to outperform their regularly wired counterparts[17].

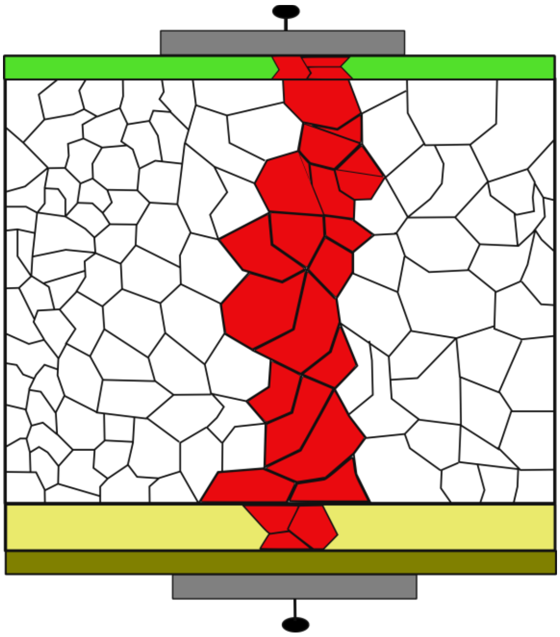

Figure 5. Representation of the electrical conductive path (red grains) of percolation nature formed across the sample.

IV. Conclusion

A sample consisting of a thin Chromium layer, P-type CdS, N-type CdTe semiconductors and Transparent Conductive Oxide (TCO) stack was found to exhibit plasticity nature upon voltage bias, which could be attributed to the threshold switching and electrically conductive path formation mechanisms. The plasticity was supported by time-lapse I-V analysis, which also confirmed the percolation conduction mechanism. Furthermore, the TEM characterization, complemented with SAED analysis, revealed a highly oriented crystalline structure for this particular sample, suggesting that the crystalline/polycrystalline semiconductor was the key factor contributing to the formation of the conductive path. Overall, these findings provide valuable insights into the behavior of semiconductor materials under voltage bias, which could inform the design and development of novel non-volatile storages devices.

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