Design and Simulation of High Gain LNA Using 28nm Technology

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***Abstract*—This research paper details the development of a cutting-edge Low Noise Amplifier (LNA) using advanced 28nm (TSMC) CMOS technology. The study focuses on achieving optimal performance in high-frequency wireless communication systems. The LNA design showcases a significant gain of 40.39 dB at 6.31 GHz and an impressive noise figure of 6.68 dB at 6.31 GHz. The methodology includes the utilization of a common-source stage LNA configuration with inductive source degeneration and cascade structures to enhance gain and noise performance. Special emphasis was placed on impedance matching, with a meticulous design of input and output networks to minimize signal loss and noise addition. The paper also explores key aspects of LNA design such as transistor sizing, stability, and linearity. Stability is rigorously analyzed using S-parameters, ensuring the LNA's resistance to self-oscillations.**

***Index Terms*—GPDK, Degeneration, LNA, Stability, Gain, Impedance, IIP3, 28nm**

I. Introduction

Over the recent year, there has been a notable trend in the miniaturization of transistors. As transistors shrink, microchips follow the trend while maintaining their capabilities. For instance, TSMC recently introduced a 3nm transistor, utilized in Apple's A18 microchip, and is evidently progressing towards 2nm technology. In this context, our study focuses on designing a low-noise amplifier (LNA) using TSMC's 28nm technology, which is currently a widely accessible option in the industry. In the realm of communications, new standards have been established to cater to various applications across different frequency bands. Modern wireless technology, driven by global trends, aims at creating low-cost, multifunctional transceivers. A critical component in such receivers is the LNA, which plays a significant role in the system's noise figure [1]. The design and optimization of the LNA, focusing on noise figure, gain, and power efficiency, are vital in the field of millimeter-wave Integrated Circuits. Traditional approaches often use a common-source configuration, but balancing the maximum small signal gain with a minimal noise figure is challenging. Inductive source degeneration structures [2] have been introduced to address this issue. However, at millimeter-wave frequencies, single-stage common-source LNAs often fail to provide high gain [3]. In another study [4], the cascaded design is essential for achieving high gain in a CMOS LNA. This high gain is achieved through positive feedback, optimal transistor biasing, and leveraging the benefits of a multi-stage amplification approach.

The evolution of communication technologies has continually spurred the development of more efficient and faster electronic components. Among these, Low Noise Amplifiers (LNAs) stand as crucial elements in modern communication systems, especially in applications like wireless and satellite communications, where the integrity of the received signal is paramount. This paper presents a novel LNA design using 28nm Complementary Metal-Oxide-Semiconductor (CMOS) technology, which balances performance metrics with power consumption and cost-effectiveness. In this context, the 28nm CMOS technology represents a significant step forward. It offers the potential for further miniaturization, reduced power consumption, and enhanced performance – aligning with the ever-increasing demands of modern communication systems. This paper aims to build upon the existing body of research, addressing some lingering challenges in LNA design, such as stability and scalability while pushing the boundaries of achievable frequency range and power efficiency using 28nm CMOS technology.

Our approach is grounded in a comprehensive understanding of the current state of LNA research, and the technological possibilities afforded by advanced CMOS processes. By integrating theoretical insights with practical design considerations, we propose an LNA design that not only meets but exceeds the current performance benchmarks, setting a new standard for future LNA developments. Nguyen, Trung-Kien, et al. provide the different techniques for the Low noise amplifier using the CMOS transistor [5]. This study analyzes and compares four optimization techniques for designing LNAs using CMOS technology - classical noise matching (CNM), simultaneous noise and input matching (SNIM), power-constrained noise optimization (PCNO), and power-constrained simultaneous noise and input matching (PCSNIM). The authors derive simple noise parameter equations to evaluate the performance of the SNIM and PCSNIM techniques. They highlight that while SNIM allows noise and input matching, it is not suitable for low-power designs. The PCSNIM technique overcomes this limitation by adding

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an extra capacitor and enables simultaneous noise and input matching even at low power levels. As a demonstration, the authors implement a 1.6 mA 900 MHz folded-cascode CMOS LNA using the PCSNIM technique. The LNA achieves a noise figure of 1.35 dB and a power gain of 12 dB from a 1.25 V supply, validating the promised performance.

In their study on LNA design, Toteva and Andonova [6] demonstrate the impacts of Electrostatic Discharge (ESD) structures on the performance of Low Noise Amplifiers in UHF application. Their work, which includes simulations in both 0.35µm and 0.18µm CMOS technologies, offers insights into how smaller CMOS technologies can improve LNA design, particularly in terms of power consumption and RF application performance, achieving over 20dB gain in the 2.2 to 2.7GHz frequency range. Ehrampoosh et al [7], emphasize the one-stage cascode amplifier with source inductive degeneration. It obtained the transmission coefficient gain of 17.62 at 18.49 GHz. Key features include a power supply of 1.2 volts, a current draw of 12 mA, and a noise figure (NF) of 1.8 dB across a 3 dB bandwidth of 16.33-18.93 GHz. Table 1 below some other study is included.

TABLE I
PERFORMANCE OF LNA FOR WIRELESS RECEIVER

	Frequency (GHz)	Technology	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
This work	6.31	TSMC 28nm	40	-12.11	- 13.62	6.68
[8]	5.25	ATF36163	7.8	-15.98	-17	4.69
[9]	5.2	CMOS	10.06	-13.56	-	- 3.73
[10]	5.25	BFP640	12	-21	-19.2	1.6
[11]	5	0.15um	15	-7	–	2
[12]	27.1	45 nm	27.1	-	-	3.3
[13]	28	22 nm	12	-	-	1.46
[14]	28	22nm	12.6	-	-	1.35

II. METHODOLOGY

In this study, various methods are used to increase gain and reduce noise in low noise amplifiers (LNAs). This investigation focuses on aspects such as impedance matching, transistor size, quantity, and S-parameters. The Common Source (CS) stage LNA, renowned for its high gain and low noise characteristics, is a prevalent approach [7]. The LNA configuration, as illustrated in Fig. 1(a), adopts a common source structure complemented by degenerative inductors. This design integrates four stages, as indicated in the figure. The primary stage concentrates on input matching, utilizing capacitors $C_1, C_2,$ and C_3, and inductors L_g and L_s. Here, L_g functions as the degenerative inductor. A resistor $R1$ is strategically placed to attain specific input reflection coefficients (S11) at a designated frequency. Due to its significant value, resistor Rb is disregarded in input impedance considerations. The capacitance and inductance values at both input and output are calculated based on the required gain and noise figure for the LNA's intended application.

The input signal traverses through the gate of the first transistor (M1) and then proceeds to the gate of the second transistor (M2). An active component assembly consisting of inductors L_3 and L_4, capacitors C_4 and C_5, and resistor R_2 establishes the reference voltage at M2's gate, ensuring operation within the saturation region. This configuration isolates the output nodes from the input by employing M1 as a common source amplifier and M2 in a common gate arrangement [15]. The inductor L_2 serves as a series-peaking inductor. The output matching phase involves inductors L_4, L_5, and capacitors C_6 and C_7.

Small signal analysis of the circuit yields the input impedance:

$$Z_{\text{in}} = \frac{1}{sC_{gs}} + sL_G + \frac{g_m L_s}{C_{gs}} \tag{1}$$

The equation's real part is adjusted to $g_m L_s/C_{gs} = 50\Omega$ for matching purposes. Selecting an appropriate L_s value, in this case, 2nH facilitates determination of frequency w_t using $R_s = L_s \cdot w_t$. Given the source resistance $R_s = 50$ ohm, w_t can be computed. The amplifier's conductance, crucial for gain and noise figure requirements, is subsequently ascertained. Once conductance is established, the gate-to-source capacitance can be determined. Utilizing Cadence Virtuoso, transistor model parameters such as oxide capacitance C_{ox} and transconductance parameter K' are obtained. The design of the input side inductor, L_g, relies on the resonance frequency concept, given the known values of gate capacitance and source inductor. The selection of inductor and gate capacitance values enables additional capacitance incorporation in the circuit, enhancing stability and reducing noise. The LNA circuit was designed in Cadence Virtuoso using the 28nm TSMC library.The drain voltage is 0.6V. DC analysis of the transistor reveals a threshold voltage of 0.531V. The interplay between transconductance (g_m), saturation voltage, and threshold voltage guided the application of the input gate voltage.

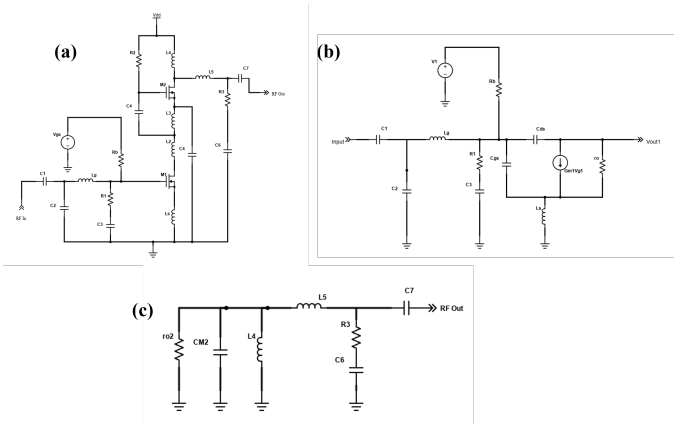

Fig. 1. (a) Cascade LNA Circuit. (b) Input Impedance Matching Circuit. (c) Output Impedance Matching Circuit.

This LNA design strategy employing degenerative inductors presents multiple benefits, including enhanced input matching, improved signal integrity, and reduced distortion. Through precise component specification in each stage, optimal performance in terms of gain, noise figure, linearity, and impedance

matching are achievable. Consequently, this LNA design substantially contributes to the development of low-power, high-performance communication systems, facilitating effective signal amplification and overall system efficiency.

TABLE II
COMPONENT AND VALUES USED IN CASCADE LNA

Components	Value	Components	Value
C1	2pF	L5	720pH
C2	100fF	Lg	3.5pH
C3	1fF	Ls	1fH
C4	340fF	R1	100Ω
C5	350fF	R2	500Ω
C6	1fF	R3	50Ω
C7	1fF	Rb	5KΩ
L2	500pH	Vdd	1.2V
L3	10nH	Vgs	600mV
L4	720pH	W1	1.3uM
		W2	2.7uM

A. Input Impedance Matching

The impedance matching is crucial in determining the desirable noise figure and gain in CMOS LNAs, particularly in receiver applications [16]. Additionally, it is also influencing the overall performance and stability of the LNA [17]. The design of an effective impedance-matching circuit is pivotal in reducing signal loss and mitigating noise within the circuit [3]. Fig. 1(b) depicts the impedance circuit designed for input impedance matching, to maximize signal reception from the antenna while minimizing loss. Component values within this circuit are determined based on calculations related to a fixed gain value, noise figure, and S-parameter.

B. Output Impedance Matching

Output impedance matching in an LNA (see Fig. 1(c)) is used to maximize power transfer and minimize signal reflections [18] [19]. This is crucial for maintaining signal integrity and overall system performance.it involves designing the LNA's output network to align with the load impedance, often using techniques like impedance transformation. Effective output impedance matching is key to achieving optimal functionality in RF and microwave systems and to send the signal from LNA to the mixture and then to the signal processor.

C. Size and Number of Transistors

The study utilized the TSMC 28nm process, a widely accessible and prevalent technology in semiconductor foundries worldwide. The length of the transistor is invariably fixed at 28nm.The parametric analysis and mathematical computations were employed to ascertain the transistors' number and dimensions. In terms of design specifics, each transistor incorporates 10 fingers. Regarding dimensions, the common source transistor is sized at 1.3 µm, while the common gate transistor measures 2.7 µm.

D. Stability

Stability in the LNA refers to the ability of the amplifier to operate without self-oscillation or producing undesired signals. An unstable amplifier can generate oscillations, leading to performance issues like signal distortion or interference with other circuit elements. This involves careful design considerations to ensure the LNA remains stable over its entire operating range, including the selection of components, circuit topology, and feedback mechanisms. To determine the stability of this LNA, the S-parameter was analyzed, along with other parameters such as the stability factor and criterion. In the above circuit Fig, 1(a) the second transistor M_2 helps to isolate the input and output ports, reducing the risk of oscillations. Additionally, the inductive degeneration further enhances the stability by introducing a positive feedback path from the output to the input. The positive feedback helps to counteract the destabilizing effects of the transistor's parasitic capacitance. The B_{1f} and K_f were examined to assess the circuit's stability. For the circuit to be considered stable, B_{1f} should be below 1 and K_f should be above one [20]. In the case of our LNA, we determined that the stability factor K_f exceeds 1, while the alternate stability factor B_{1f} is below 1, i.e., 0.89, confirming that our LNA is unconditionally stable.

E. Linearity

Linearity in LNA design refers to the amplifier's ability to output a signal that is a linear representation of its input, without distortion. This is crucial in communication systems, as non-linearities can lead to signal degradation, inter-modulation products, and distortion, all impairing the transmitted information's quality and integrity. High linearity in an LNA ensures that the amplified signal remains true to the original, this is especially important in systems like 5G, where maintaining signal fidelity at higher frequencies and over wide bandwidths is essential [21]. Achieving high linearity in LNAs is therefore a key focus in modern communication system design. To obtain the linearity in the circuit, we employed different techniques; we used the cascade configuration with the common source and common gate amplifier using the series peaking inductor. We employed the biasing technique with the common stage amplifier to obtain proper linearity. The input and output matching technique also plays an important role in the circuit's linearity. We used the third-order intercept point to measure the linearity of the circuit.

The Third-Order Input Intercept Point (IIP3) is used in amplifiers, like LNAs, to quantify non-linear distortion. It is a theoretical point where the power of the third-order inter-modulation product (a type of distortion generated by the amplifier when processing multi-tone signals) equals the power of the fundamental tone. In practice, IIP3 is used to predict how an amplifier will behave with strong input signals and to assess its linearity. A higher IIP3 value indicates better linearity, meaning the amplifier can handle stronger signals without significant distortion.

1-dB compression point (P1dB) and the third-order intercept point (IP3) are key metrics for assessing device non-linearity.

A useful method to estimate the Input Third-Order Intercept Point (IIP3) from the 1-dB compression point is given by adding 10 dB to P1dB. In receiver design, it's important to consider the nonlinearity of all components, especially since the received signal is often weak. The overall IIP3 for cascaded receiver blocks can be calculated using a specific formula, considering each component's contributions to the total nonlinearity.

$$\frac{1}{\text{IIP}_3} = \frac{1}{\text{IIP3}_1} + \frac{G_1}{\text{IIP3}_2} + \frac{G_1 G_2}{\text{IIP3}_3} + \cdots + \frac{(G_1 G_2 \ldots G_N)}{\text{IIP3}_N} \quad (2)$$

F. Gain

Gain, in the context of electronic amplifiers like LNAs, refers to the amplifier's ability to increase the power of a signal. It's calculated as the ratio of the output power to the input power, typically measured in decibels (dB) [6].The design of the amplifier must carefully balance gain with other performance factors like noise figure, bandwidth, and linearity [6]. Achieving the right gain is crucial because it directly affects the signal's strength and quality for effective communication [18]. Too much gain can lead to signal distortion, while too little can result in a signal too weak for practical use [21].

G. Noise Figure

The noise figure is a measure of degradation in the signal-to-noise ratio caused by a system. The noise figure indicates how much additional noise is introduced by a device or circuit compared to an ideal noiseless device. To find the noise figure of the cascade LNA noise figure of each transistor should be found. A noise figure of 6.68 dB is obtained at the frequency of 6.31 GHz. The noise figure of LNA is influenced by its intrinsic noise parameters, such as the noise figure of the transistor itself, the gate resistance, channel noise resistance, and gate capacitance. The size of the transistor also can affect the noise figure. Optimizing the transistor size and biasing conditions can help to achieve better noise performance. Proper selection of biasing points and operating regions can help to minimize the noise in the circuit. Other factors that affect the noise figure are parasitic capacitance inductor and supply voltage [22].

H. S Parameter

The purpose of analyzing S-parameters in an LNA is to understand its behavior and evaluate its performance in terms of gain, reflection, and stability. S-parameters provide valuable information about how the LNA interacts with the input and output signals at different frequencies. S-parameters quantify the amount of power reflected from the LNA's input and output ports, as well as the amount of power transmitted through the LNA [17].

III. Results

A. Gain

The voltage gain of the proposed LNA using the small signal analysis is shown in Fig. 2(a). The graph reveals that the LNA operates with increasing efficiency up to a frequency of 6.31 GHz, where it reaches its maximum gain—slightly above 40 dB. The steepness of the gain curve at and around the peak suggests that the LNA has been designed to work within a narrow frequency range, providing high selectivity for signals around the 6.31 GHz mark. This is characteristic of LNAs that are intended for specific applications, such as satellite communication or certain radar systems, where signal integrity at a particular frequency is crucial. The graph also allows us to infer the bandwidth over which the LNA maintains a gain close to its peak value. This bandwidth is crucial for applications that require a certain range of frequencies to be amplified without significant loss of signal strength. The sharpness of the peak can also imply a higher quality factor (Q factor), which is a measure of the resonator's bandwidth relative to its center frequency and indicates a more selective filter.

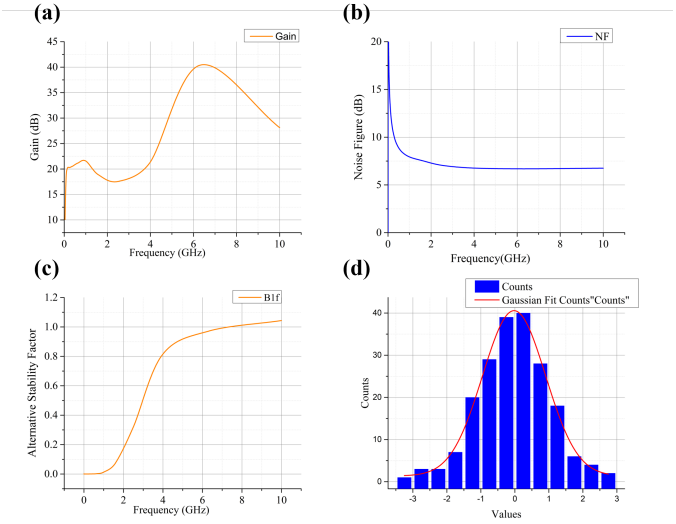

Fig. 2. (a) Gain 40.39 dB at frequency of 6.31 GHz. (b) Noise Figure 6.68 dB at Frequency 6.31 GHz. (c) B1f at Different Frequency. (d) Monte Carlo Simulation.

B. Noise Figure

The noise figure (NF) graph for the LNA provides a detailed view of the noise performance across the frequency spectrum. Specifically, at the frequency of interest, 6.31 GHz, the NF is recorded at 6.68 dB (see Fig. 2(b)). This particular value is a critical indicator of the LNA's quality, as the noise figure represents the degradation of the signal-to-noise ratio (SNR) as the signal passes through the amplifier. The graph itself shows a rapidly descending NF as frequency increases from 0 GHz, leveling off to a relatively flat response beyond 2 GHz. The point of interest at 6.31 GHz lies well within this flat region, indicating a stable noise performance across this high-frequency operational range. This flatness is desirable in practical applications because it suggests that the LNA can reliably amplify signals without significantly adding to the noise across its working bandwidth, which, in this case, includes the 6.31 GHz frequency.

C. Stability

The stability of the proposed LNA across the operational frequency spectrum is critically assessed through the $B1f$ stability factor. As illustrated in Fig. 2(c), the $B1f$ parameter, which serves as an indicator of potential self-oscillation, remains well below the critical value of 1 up to approximately 8 GHz. This suggests that the LNA operates within a stable regime, free from unwanted oscillatory behavior over this frequency range. At the design's focal operational frequency of 6.31 GHz, the $B1f$ value is observed to be 0.89, reinforcing the LNA's stable operation.

Beyond 8 GHz, the $B1f$ parameter incrementally surpasses the unity mark, where the stability of the LNA can no longer be guaranteed. This upward trend in the stability factor suggests an onset of potential instabilities, likely attributable to the amplifier's internal feedback mechanisms.

The Monte Carlo simulation results for the LNA gain are presented as a histogram overlaid with a Gaussian fit (Fig. 2(d)). The histogram illustrates the distribution of gain values from the simulation, showing a normal distribution around a central mean value. This is indicated by the bell-shaped pattern of the blue bars, with most values clustered around this central peak. The Gaussian fit, depicted by the red curve, aligns closely with the histogram, suggesting that the gain values are consistent with a normal distribution, indicative of a stable LNA design. The spread of the gain values, represented by the width of the Gaussian fit, quantifies the standard deviation, providing insight into the variability of the LNA gain. A relatively narrow spread implies low variability, which denotes that the LNA is likely to perform reliably under varied operational conditions as modeled by the simulation.

D. S Parameter

An integral aspect of the LNA performance assessment is the analysis of the return loss, quantified by the S11 parameter.In Our LNA design examined that input reflection coefficient S11 is -12.11dB (Fig. 3 (a)) which indicates seamless input matching to the proposed LNA. At the operational frequency of 6.31 GHz, the S11 parameter reaches a value of -12 dB, indicating a substantial reduction in power reflection at the input of the amplifier. This level of return loss signifies that approximately 94% of the incident power is being accepted by the LNA, with only about 6% reflected to the source. Such a measure of impedance matching is considered satisfactory in many practical applications.

The S12 parameter quantifies the reverse isolation, reflecting the signal's magnitude from the output port back to the input port. At the designated frequency of 6.31 GHz, the measured S12 value is a remarkable -51 dB (Fig. 3(b)). This metric emphasizes the LNA's exceptional ability to prevent the reverse transmission of signals, allowing only a negligible fraction of the output power, approximately 3.16×10^{-6} of the input power, to be fed back into the input. Such a small value of reverse isolation is pivotal in safeguarding the amplifier against self-oscillation and ensuring the fidelity of the signal amplification process.

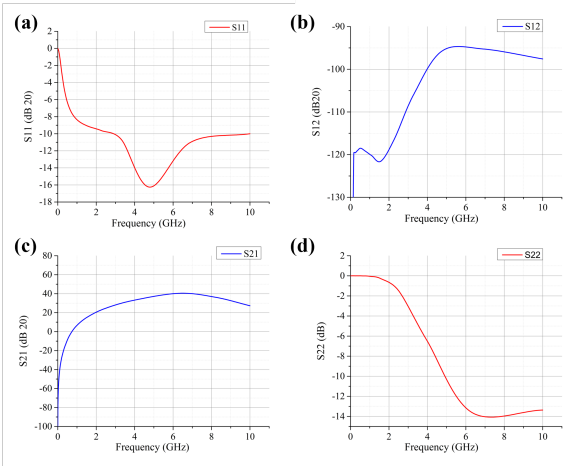

Fig. 3. (a)Input Reflection Coefficient (S11) at 6.31 GHz. (b)Reverse Volage Gain (S12) at Frequency 6.31 GHz. (c)Forward Voltage Gain (S21) at 6.31 GHz. (d)Output Reflection Coefficient (S22) at 6.31 GHz.

The behavior of the S21 parameter, indicative of the forward gain of the LNA, is captured in Fig.3(c). Our observations confirm that the LNA achieves a strong gain of 40 dB at a frequency of 6.31 GHz.A high degree of amplification at 6.31 GHz is particularly beneficial for applications within this frequency band, as it ensures that signals are sufficiently strengthened to counteract losses encountered during transmission or in subsequent stages of reception.

The graph delineates a smooth rise in gain with increasing frequency, peaking precisely at 6.31 GHz, followed by a modest descent in gain as the frequency continues to increase. This pattern indicates not only the substantial amplifying power of the LNA but also its operational stability over the assessed frequency range.

The output return loss, depicted by the S22 parameter, in Fig.3(d) delineates the behavior of the S22 parameter throughout frequencies ranging from 0 to 10 GHz. A noteworthy observation is made at the frequency of 6.31 GHz, where the S22 value registers at -13.62 dB. This value conveys that the output matching is not absolute but is sufficiently effective, with approximately 4.6% of the signal's power being reflected from the load.

E. Linearity

When the input signal is weak with a strong interfering signal in proximity, linear operation is important. There is the possibility for unwanted intermodulation distortion such as blocking and cross modulation. Third-order intercept (IP3) and 1-dB compression point (P_{1dB}) are two measures of linearity. IP3 shows at what power level the third-order intermodulation product is equal to the power of the first-order output. P_{1dB} shows at what power level the output power drops 1dB. By knowing either IP3 or P_{1dB} the other can be found using the following rule of thumb formula [20].

$$\text{IP3} = P_{1dB} + 10\text{dB} \tag{3}$$

IV. Layout

The LNA layout was created using Cadence Virtuoso (see Fig. 4), applying TSMC's 28nm CMOS technology. This layout incorporates critical design features such as multi-layered construction to reduce parasitic effects and maintain signal integrity at the target frequency of 6.31 GHz. Using planar inductors and careful component placement contributes to the LNA's high gain and low noise figure.The core area of the LNA layout is 0.48mm x 0.32mm.

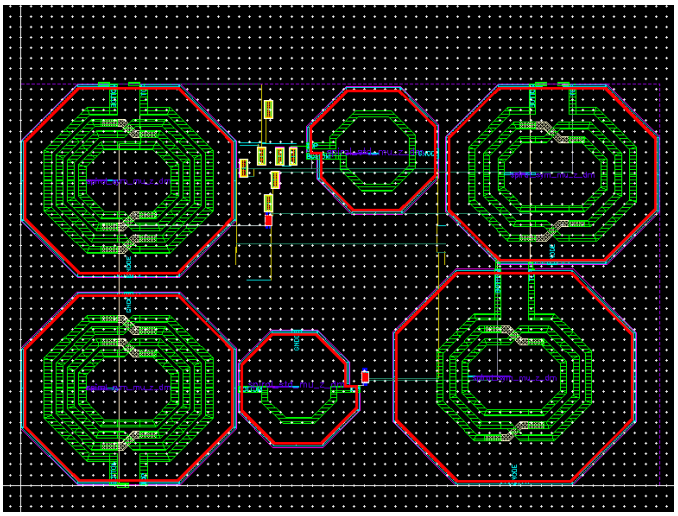

Fig. 4. Layout Design of LNA

V. Discussion

In examining LNA characteristics, particularly at the operational frequency of 6.31 GHz, several key aspects emerge that are pertinent to the discussion. The gain graph elucidates the LNA's performance, prominently featuring its high-gain and high-selectivity attributes centered around this frequency. Such characteristics are crucial for users in applications where frequency specificity is critical. Furthermore, the Noise Figure (NF) value at 6.31 GHz offers a quantifiable metric for evaluating the LNA's performance. This parameter suggests the addition of noise by the LNA, albeit within acceptable thresholds for numerous high-frequency applications. Notably, the graph implies an optimization in the LNA's design aimed at maintaining a steady noise performance over an extensive frequency range. This characteristic is instrumental for ensuring consistent and reliable performance in communication systems. The $B1f$ value at the specified frequency falls within a range indicative of substantial stability, a factor crucial for an amplifier's reliable functioning. This attribute underscores that the LNA does not contribute to system instability, thereby maintaining the integrity of signal amplification and preventing the introduction of oscillations or other undesirable effects. Consequently, this stability criterion at 6.31 GHz signifies a robust and reliable design suitable for practical applications requiring stable operation at this frequency. The S11 parameter at 6.31 GHz also reveals efficient impedance matching at this frequency. This match presumably aligns with the operation frequency for the intended application, ensuring effective signal transfer and amplification. The S12 value at 6.31 GHz, being -51 dB, indicates a well-designed LNA capable of providing stable and reliable performance in high-frequency applications such as radar or communication systems, where reverse isolation is critical. Moreover, the 40 dB forward gain at 6.31 GHz highlights the LNA's strong amplification characteristics at this frequency, rendering it suitable for high-frequency applications that necessitate such a level of signal enhancement without requiring multi-stage amplification. The analysis of the amplifier's performance plot indicates that the amplifier is optimally tuned to provide maximum gain at 6.31 GHz, capable of robust and stable amplification in the frequency range leading up to this peak. Lastly, the S22 value of -13.62 dB at 6.31 GHz implies that the LNA's output impedance is reasonably well-matched with the expected load impedance at this frequency. This matching is essential for efficient signal transfer. It minimizes potential issues related to signal reflections, such as standing waves or power losses, thereby maintaining the integrity of the amplified signal as it transitions from the LNA to subsequent stages in the signal chain.

VI. Conclusion

The proposed Low Noise Amplifier, based on 28nm CMOS technology, has several noteworthy achievements.. The LNA design successfully addresses the critical challenges of high gain, low noise figure, and stability in high-frequency applications. Achieving a gain of 40.39 dB at 6.31 GHz and a noise figure of 6.68 dB at 6.31 GHz, the design sets new benchmarks in LNA performance. The use of a common-source stage with inductive source degeneration and cascade structures effectively enhances both gain and noise characteristics. Additionally, the comprehensive approach to impedance matching, stability analysis using S-parameters, and linearity considerations, as evidenced by the stability analysis, collectively contribute to the LNA's robust performance. This research demonstrates significant advancements in LNA design and lays the groundwork for future innovations in high-frequency communication technologies, catering to the evolving demands of wireless and satellite communication systems.

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