A Comprehensive Literature Review on Voltage Reference Circuits: Analysis and Comparison of State-of-the-Art Designs

Guray Ozgur

***Abstract*—This paper presents a comprehensive literature review and comparative analysis of voltage reference circuits, examining 30 state-of-the-art designs published during the 2010s. Voltage references are critical building blocks in analog and mixed-signal integrated circuits, providing stable reference voltages independent of process, voltage, and temperature variations. The surveyed circuits are systematically categorized into eight distinct groups based on their primary design objectives: ultra-low power (ULP), ultra-low voltage (ULV), high power supply rejection ratio (PSRR), high precision, low-voltage low-power, low temperature coefficient, harsh environment operation, and small die area implementations. For each category, detailed performance comparisons are provided, including key metrics such as temperature coefficient, line regulation, power consumption, chip area, and PSRR. The paper also provides a thorough background on voltage reference fundamentals, performance metrics, and advanced design techniques, including temperature compensation methods, sub-1V operation, higher-order curvature correction, and resistorless CMOS implementations. This comprehensive survey serves as a valuable reference for researchers and designers working on voltage reference circuits, offering insights into design trade-offs and identifying research trends in the field. The analysis reveals that while significant advances have been made in ultra-low power and sub-1V operation, challenges remain in simultaneously achieving multiple performance objectives, highlighting opportunities for future research.**

***Index Terms*—Voltage references, analog integrated circuits, CMOS, bandgap references, PTAT, CTAT, ultra-low power, sub-1V operation, temperature compensation, literature review**

I. INTRODUCTION

VOLTAGE reference circuits are fundamental building blocks in analog and mixed-signal integrated circuits, providing stable and precise reference voltages that are ideally independent of process variations, supply voltage fluctuations, and temperature changes. These circuits play a crucial role in numerous applications including analog-to-digital converters (ADCs), digital-to-analog converters (DACs), switching regulators, and precision analog circuits. The demand for voltage references with diverse characteristics has grown significantly due to the proliferation of applications in radio frequency (RF), Internet of Things (IoT), system-on-chip (SoC), biomedical devices, and space systems, each requiring distinct performance specifications.

Modern applications impose varying and often conflicting requirements on voltage reference designs. For instance, IoT devices demand ultra-low power consumption to extend battery life, while precision instrumentation requires exceptional accuracy and low temperature drift. Similarly, portable devices benefit from sub-1V operation for compatibility with scaled CMOS technologies, whereas harsh environment applications prioritize radiation tolerance and wide temperature range operation. This diversity in requirements has led to specialized design techniques and trade-offs, making the comparison and selection of appropriate voltage reference architectures a complex task.

This comprehensive literature review examines 30 state-of-the-art voltage reference circuits published during the 2010s, providing designers and researchers with a systematic analysis of design approaches, performance metrics, and trade-offs. The selected circuits represent significant contributions across eight key application domains: ultra-low power, ultra-low voltage, high power supply rejection ratio (PSRR), high precision, low-voltage low-power, low temperature coefficient, harsh environment operation, and small die area implementations.

This paper is organized as follows: performance measures such as line regulation, temperature coefficient, power supply rejection ratio, quiescent current, noise, circuit size, and power dissipation are explained in Section II. Under the Section III, temperature compensation techniques, in Section III-A, sub-1V voltage references, in Section III-B, high order curvature correction, in Section III-C, and resistorless CMOS voltage references, in Section III-D are considered in an informative manner. 30 state-of-the-art voltage references are categorized and summarized in Section IV, whereas in Section V, these voltage references are compared in a compact way.

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II. PERFORMANCE MEASURES

A reliable, precise reference voltage is always needed for different kinds of circuits. It should not depend on supply voltage, temperature differences, transient changes in the circuit, or load. Hence, the voltage reference circuits should deliver an outstanding performance, both static and dynamic. A bad static performance occurs due to manufacturing, mismatches, channel length modulation, etc. It can be improved with trimming, while a dynamic performance is affected by the temperature coefficient (TC) , the line regulation, the power supply rejection ratio ($PSRR$), and the output noise. Before going into details, one must understand the following performance parameters. Otherwise, there would be no point in comparing the state of the art voltage references.

A. Line Regulation

The line regulation states how much change occurs in the nominal reference voltage, which is the output voltage of the reference circuit, with respect to the variation in input voltage at the nominal temperature. To measure the line regulation, we need a measuring environment, for example R_{LOAD} or C_{LOAD}, and I_{OUT}. Thus, not only line regulation should be specified but also the measuring environment. Line regulation, $\mathcal{S}_{LR,T_{nom}}$ is shown in Equation 1 [1].

$$\mathcal{S}_{LR,T_{nom}} = \frac{\Delta V_{REF,T_{nom}}}{\Delta V_{IN}} (\mu \mathrm{V/V}) \tag{1}$$

Moreover, here we can define a parameter called the dropout voltage, V_{DROP}, which is the difference between the input and output voltage. An important parameter about the dropout voltage is $V_{DROP(\min)} = V_{IN(\min)} - V_{REF(nom)}$. A low $V_{DROP(\min)}$ is generally related with higher power efficiency and higher voltage range.

B. Temperature Coefficient

Many characteristics of the physical devices change with the temperature which they are operating, thus voltage reference is surely affected by the temperature. Temperature coefficient, TC, or also called the temperature sensitivity $\mathcal{S}_{TC}$ is defined as in Equation 2.

$$\mathcal{S}_{TC,V_{IN(nom)}} = \frac{\Delta V_{REF,V_{INinom}}}{\Delta T \cdot V_{REF(nom)}} \times 10^6 \, (\mathrm{ppm/^\circ C}) \tag{2}$$

Again, it is measured under specific load, whose characteristics should be specified together with the temperature coefficient. Moreover, it is quite hard to alter TC, since by changing a single design parameter, not only TC is affected but also the other performance parameters are affected. Most importantly, it is a crucial parameter in the design as the accuracy of the circuit requires a precise reference voltage, which is not the case when it is temperature dependent. To illustrate, an analog to digital converter requires a reference voltage, and if this reference voltage was highly temperature dependent, the digital signal probably would not represent the analog signal [1].

C. Power Supply Rejection Ratio

In real applications, power line on the chip picks up some noise such as clock signal glitches, or maybe there are some variations on the supply because of the outside world. So, we also see some small unwanted signal at the power supply. Power supply rejection ratio, $PSRR$, is a function of frequency and represented as in Equation 3 [1].

$$PSRR(f) = 20 \log \frac{V_{REF,AC}(f)}{V_{IN,AC}(f)} (dB) \tag{3}$$

D. Quiescent Current

The quiescent current, I_q, or the supply current, is the needed current to run the voltage reference at quiescent state. In other words, there is no resistive load, and in nominal conditions, $V_{IN(nom)} \times I_{q(nom)}$ gives the steady state power consumption of the voltage reference. Low quiescent current is desired, as it indicates lower power consumption and less self-heating [1].

E. Output Noise

Output noise, like $PSRR$, is a frequency dependent parameter. Output noise is generally originated from thermal noise, which is the random movement of free electrons due to heat. Peak-to-peak voltage is specified for the measurement of output noise, and found approximately by multiplying 6 with the RMS value [1].

F. Other Design Considerations

In addition to the above parameters, the designer has to consider other design limitations while finalizing the product. Although the cost is a huge limitation to the final product, it will not be discussed, as it does not contribute much to a literature review. What is considered briefly is as follows:

1) Circuit size: By considering that thermal noise depends on the total size and pink noise depends on the area of the gate, one can obtain gigantic circuit areas unexpectedly in order to reduce the noise. Moreover, there can be area limitations considering the applications such as space or biomedical applications.

2) Power dissipation: As mentioned before, power dissipation is related with the supply current, i.e. quiescent current. Again, by considering that thermal noise depends on the quiescent current, to reduce the noise for instance, designer could consider very large currents, which is not possible. There is always a trade-off. In some way, designer tries to find ways to reduce the quiescent current to reduce the power dissipation. Power dissipation is a especially significant design parameter for circuits powered with a battery because it has a limited life.

3) Device mismatch: A voltage reference should not be sensitive to mismatches since a small difference can potentially degrade the performance of the reference and affect the precise voltage value. In order to design a good voltage reference, designer should use device matching techniques such as systematic variation and circuit trimming.

4) Ease of output trimming: Trimming is a procedure that increases cost by adding extra steps to the manufacturing process. In addition to that, trimmed structures use a relatively large area, which also adds additional noise component decreasing the performance of the voltage reference and additional cost.

TABLE I
SUMMARY OF DESIGN PARAMETERS

Parameters	Desired
Line Regulation	↓
Temperature Coefficient	↓
Power Supply Rejection Ratio	↑
Quiescent Current	↓
Output Noise	↓
Circuit Size	↓
Power Dissipation	↓
Device Mismatch	↓
Cost	↓

III. ADVANCED VOLTAGE REFERENCES

Before going in depths of the subject, and introducing 30 state-of-the-art voltage reference circuits, theory and the ideas accepted by the majority are presented in this section, including Temperature Compensation Techniques, in Section III-A, Sub-1V Voltage Reference Circuits, in Section III-B, High Order Curvature Correction, in Section III-C, and CMOS Voltage Reference without Resistors, in Section III-D.

A. Temperature Compensation Techniques

The underlying opinion of a bandgap voltage reference is to obtain a zero TC by adding PTAT and CTAT terms accordingly, shown in Equation 4.

$$V_{sum}(T) = m_1 V_{PTAT}(T) + m_2 V_{CTAT}(T) \tag{4}$$

To obtain a zero TC, m_1 and m_2 should be chosen carefully like in Equation 5.

$$\frac{\partial V_{sum}(T)}{\partial T} = m_1 \frac{\partial V_{PTAT}(T)}{\partial T} + m_2 \frac{\partial V_{CTAT}(T)}{\partial T} = 0 \tag{5}$$

For example, reference voltage for a Widlar bandgap voltage reference, shown in Figure 1, or opamp based β-multiplier bandgap voltage reference, shown in Figure 2, is given as in Equation 6.

$$V_{REF}(T) = V_{BE}(T) + MV_T(T) \tag{6}$$

By differentiating both sides, M can be adjusted approximately to a zero TC for a temperature interval around the nominal temperature value.

For opamp based β-multiplier bandgap voltage reference, shown in 2, we have

$$\Delta V_{BE_{1,2}} = V_T \ln(N) = IR_1 \tag{7}$$

$$I = V_T \frac{\ln(N)}{R_1} \tag{8}$$

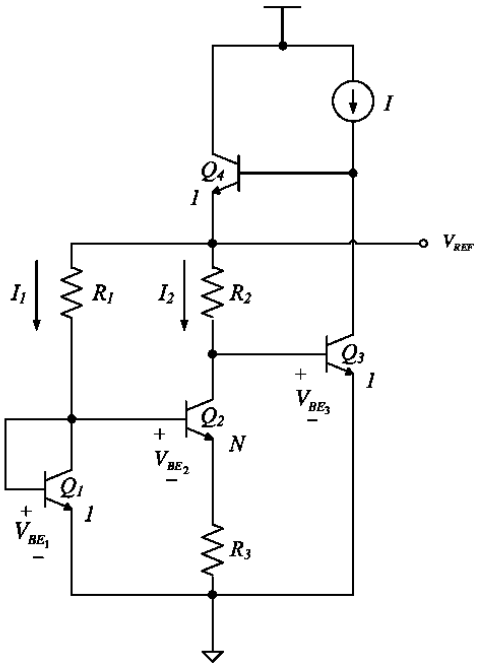

Fig. 1. Widlar BGR

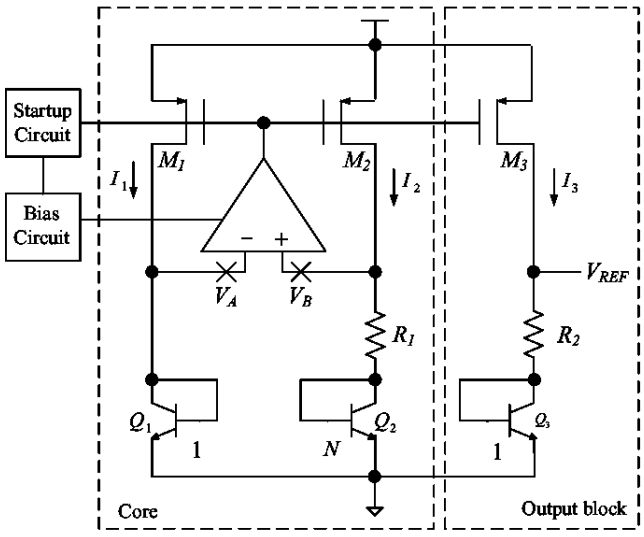

Fig. 2. Opamp Based β-Multiplier Bandgap Voltage Reference Circuit

$$\begin{aligned} V_{REF} &= IR_2 + V_{BE_3} \\ &= \frac{R_2}{R_1}\Delta V_{BE_{1,2}} + V_{BE_3} \\ &= \frac{R_2 \ln(N)}{R_1} V_T + V_{BE_3} \end{aligned} \tag{9}$$

Major circuit elements are operational amplifiers, current mirrors, startup circuits, resistor networks and bipolar transistors. One should note that it is important to be aware of input common mode voltage and loop gain for the operational amplifier design while designing. Non-ideal opamps, current mirror mismatches, size and β variations for BJTs, resistor and power supply variations are the main error sources in bandgap

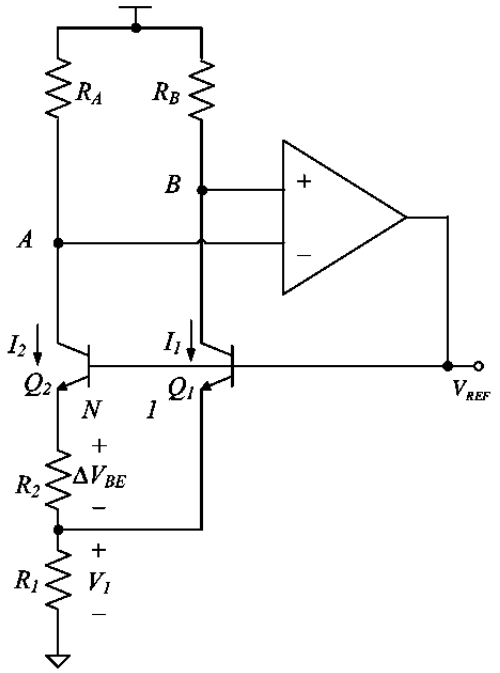

Fig. 3. Brokaw BGR

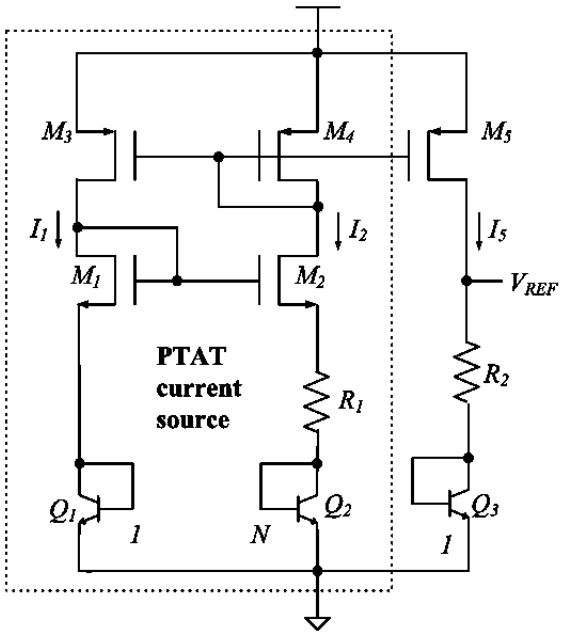

Fig. 4. β-Multiplier Based $V_{BE} - \Delta V_{BE}$ BGR

reference circuits. Input offset voltage, limited gain and PSRR should be taken into account for an opamp. Channel length modulation compensation, and cascode current mirrors can be utilized by the circuit for a better performance.

For Widlar bandgap voltage reference, shown in 1, we have

$$I_2 = \frac{\Delta V_{BE_{1,2}}}{R_3} = \frac{V_T \ln(N)}{R_3} \tag{10}$$

$$\begin{aligned} V_{REF} &= V_{BE_3} + I_2 R_2 \\ &= V_{BE_3} + \frac{R_2}{R_3} V_T \ln(N) \end{aligned} \tag{11}$$

There is an assumption made here, which is there is no difference between I_1 and I_2. Since there is large difference in emitter sizes of BJTs, our assumption is not that negligible. Also, β is not that large in CMOS processes, which contradicts the assumption of base current is negligible, which depends on the temperature as in β. So, it is important to have $I_1 = I_2$.

What Brakow did was to get an opamp into use to satisfy $I_1 = I_2$. Unlike Widlar BGR, it is easy to obtain a higher performance by implementing trimming and it has a larger output driving power, which unfortunately makes Brakow BGR hard to use for low power applications. The schematic of Brokaw BGR is presented in Figure 3.

For Brokaw bandgap voltage reference, shown in 3, we have

$$\begin{aligned} V_1 &= 2IR_1 \\ &= 2R_1 \frac{\Delta V_{BE_{1,2}}}{R_2} \\ &= \frac{2R_1}{R_2} \ln(N) V_T \end{aligned} \tag{12}$$

$$\begin{aligned} V_{REF} &= V_{BE_1} + V_1 \\ &= V_{BE_1} + \frac{2R_1 \ln N}{R_2} V_T \end{aligned} \tag{13}$$

There are other ways to keep the currents at the same value, one notable circuit is β-multiplier circuit, which do not use an operational amplifier. Its design and analysis is given in Figure 4 and Equations 14 and 15, respectively. For β-multiplier based $V_{BE} - \Delta V_{BE}$ bandgap voltage reference, shown in 4, we have

$$I_1 = I_2 = I_5 = \frac{\Delta V_{BE_{1,2}}}{R_1} = \frac{V_T \ln N}{R_1} \tag{14}$$

$$V_{REF} = I_5 R_2 + V_{BE_3} = \frac{R_2}{R_1} V_T \ln N + V_{BE_3} \tag{15}$$

One can also use only MOSFETs, BJT-free, to obtain PTAT and CTAT currents and sum the current in an output stage, shown in Figure 5, in sub-threshold region. Circuit is governed by the Equations 16, 17, and 18, where ζ is the sub-threshold conduction.

$$\begin{aligned} V_{GS_6} &= V_{th,n} + \sqrt{\frac{2I_{DS_6}}{\mu_n C_{ox,n} S_6}} \\ V_{GS_6} &\approx V_{th,n} \end{aligned} \tag{16}$$

$$I_{SD_7} = I_{DS_6} = \frac{V_{GS_6}}{R_2} \approx \frac{V_{th,n}}{R_2} \tag{17}$$

$$\begin{aligned} V_{REF} &= \frac{R_3}{R_1} \frac{S_{10}}{S_4} \zeta \ln(N) V_T + \frac{R_3}{R_2} \frac{S_9}{S_7} V_{th,n} \\ &= \frac{R_3}{R_2} \frac{S_9}{S_7} \left(\frac{R_2}{R_1} \frac{S_7}{S_9} \frac{S_{10}}{S_4} \zeta \ln(N) V_T + V_{th,n} \right) \end{aligned} \tag{18}$$

In short, either in voltage form or current form, basic idea is to create temperature dependent factors, and to compensate those factors by adding or subtracting. In other words, it is needed PTAT/CTAT current (or voltage) sources and a mechanism to combine those [1].

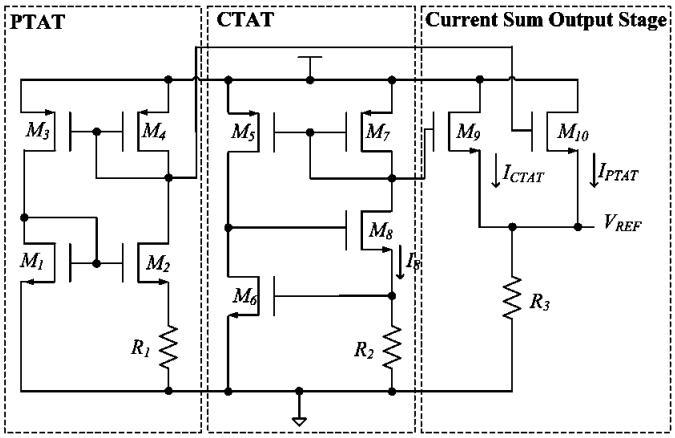

Fig. 5. V_{GS} based CTAT Current Source, and associated $V_{GS} - \Delta V_{GS}$ Compensation

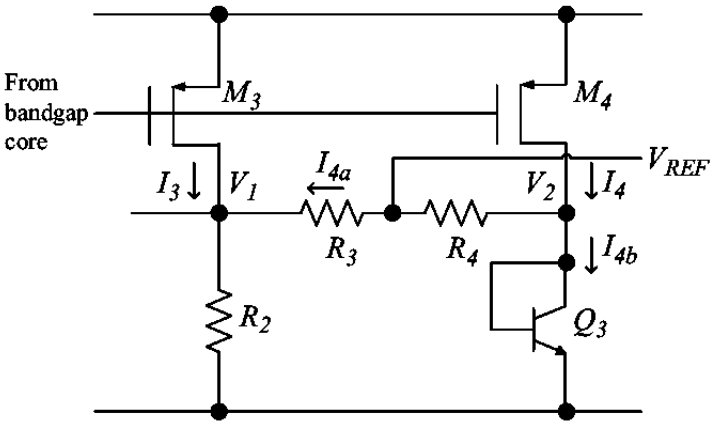

Fig. 6. Resistive V_{BE} Sub-division for β-Multiplier BGR

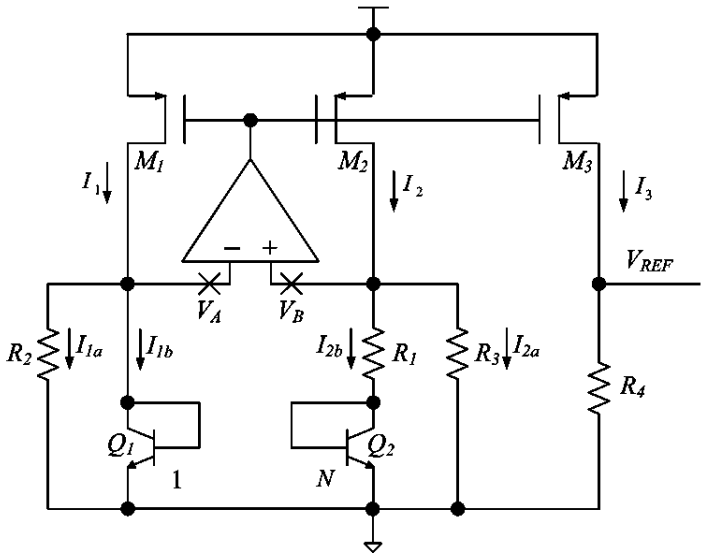

Fig. 7. Sub-1V β-Multiplier BGR using Resistive Division

B. Sub-1V Voltage Reference Circuit

With the increasing trend of smaller circuits using low voltage values to reduce the power dissipation and boost the speed of the circuit, voltage references creating a reference below 1V became an essential and its design is not an easy task with low supply voltage. The most challenging task for a sub-1V voltage reference circuit is to satisfy the threshold voltage for MOSFET, which can be solved by using depletion mode transistor, an n-channel MOSFET with negative threshold and a p-channel MOSFET with positive threshold. However, it is not possible for the most of the CMOS processes. There are some techniques such as floating-gate and bulk-driven, but they bring some other disadvantages. That's why, most of the time the subthreshold region is chosen for the operating region for MOSFET.

One of the simplest ways of obtaining a sub-1V is to use resistive division to scale the reference voltage to a low voltage, which is done with adding an output stage. In this way, we do not deal with the output noise and load problems. An additional stage to β-multiplier BGR is shown in Figure 6, and reference voltage is obtained as in Equation 19 with a scaling factor $(R_2 + R_3)/(R_2 + R_3 + R_4)$.

$$\begin{aligned} V_{REF} &= (V_{BE_3} - V_{REF}) \frac{R_3 + R_2}{R_4} + I_3 R_2 \\ &= \frac{R_2 + R_3}{R_2 + R_3 + R_4} V_{BE_3} + \frac{R_2 R_4}{R_2 + R_3 + R_4} I_3 \\ &= \left(\frac{R_2 + R_3}{R_2 + R_3 + R_4} \right) \left(V_{BE_3} + \frac{R_2 R_4}{R_1 (R_2 + R_3)} \ln N V_T \right) \end{aligned} \tag{19}$$

By using conventional opamp based β-multiplier bandgap voltage reference circuit, and by adding two resistors, namely R_1 and R_2 as shown in Figure 7, resistive division can be applied and a low voltage reference can be obtained. Its scaling factor is given in Equation 20 as R_4/R_3. Its performance is comparible with the conventional opamp based β-multiplier bandgap voltage reference circuit, and it needs a sufficient supply voltage. It is not compatible with low supply voltages, thus it is performance is not much different from an opamp based β-multiplier BGR [1].

$$\begin{aligned} V_{REF} &= I_3 R_4 \\ &= (I_{2a} + I_{2b}) R_4 \\ &= \left(\frac{V_{BE_1}}{R_3} + \frac{\Delta V_{BE_{1,2}}}{R_1} \right) R_4 \\ &= \frac{R_4}{R_3} \left(V_{BE_1} + \frac{R_3}{R_1} V_T \ln N \right) \end{aligned} \tag{20}$$

C. High Order Curvature Correction

We can, in theory, have a zero TC by compensating PTAT and CTAT correctly. We know that negative temperature coefficient is referred to as CTAT (Complementary To Absolute Temperature), and positive temperature coefficient is referred to as PTAT (Proportional To Absolute Temperature). However, CTAT and PTAT usually are not linearly proportional to

temperature. Thus, we can write the Taylor Series Expansions at $T = T_{(nom)}$ as

$$\begin{aligned} V_{CTAT}(T) &= a_0 + a_1\left(T - T_{(nom)}\right) + a_2\left(T - T_{(nom)}\right)^2 + \cdots \\ V_{PTAT}(T) &= b_0 + b_1\left(T - T_{(nom)}\right) + b_2\left(T - T_{(nom)}\right)^2 + \cdots \end{aligned} \tag{21}$$

$$V_{REF}(T) = m(T)V_{CTAT}(T) + n(T)V_{PTAT}(T) \tag{22}$$

To get a zero TC, we need

$$m(T)a_i + n(T)b_i = 0, \quad 0 \le i \le \infty \tag{23}$$

which is not possible of course. So, we use different compensations such as

1) First order temperature compensation
   $(a_i, b_i = 0, \quad 2 \le i \le \infty)$ By solving for m and n, we get
   $$\begin{aligned} m(T) &= 1 \\ n(T) &= -\frac{a_1}{b_1} \end{aligned} \tag{24}$$
   Voltage references presented in Section III-A are mostly this type.
2) Second order temperature compensation
   $(a_i, b_i = 0, \quad 3 \le i \le \infty)$ Then, we can write V_{REF} as
   $$V_{REF}(T) = mV_{CTAT}(T) + nV_{PTAT}(T) + s\left(T - T_{(nom)}\right)^2 \tag{25}$$
3) Piece-wise linear compensation
   For this compensation, we define linear functions for V_{CTAT} and V_{PTAT} in selected temperature intervals.

Current subtraction or addition circuits can be implemented to introduce second order dependency. An example is shown in Figure 8. At some temperature, M_N will draw current, and by reducing current density of Q_2, it will reduce V_B. Since it will arise a difference between nodes A and B. Thus, the current of M_2 will increase to compensate the difference. This increase will affect M_3, and thus V_{REF}. By creating a positive loop through M_4, a high order temperature compensation is achieved [1].

D. CMOS Voltage Reference without Resistors

A resistance can be implemented by use of MOSFETs in two ways. One is the inverse function technique, which uses voltage-to-current conversion and current-to-voltage conversion consecutively. The other is negative impedance converter technique, which is a block with a negative relation in the input and output impedances. Implementations of inverse function technique and negative impedance converter are given in Figures 9 and 10. In Figure 11, a resistorless voltage source using inverse function technique, and in Figure 12, a resistorless current source using negative impedance converter technique are given, which can be adopted in voltage references. Voltage references adopting these techniques are shown in Figures 13 and 14, respectively. By taken $V_3 = 0$, there is a relation between V_O and $V_2 - V_1$ such as

$$V_O = \sqrt{\frac{AG}{C}}\left(V_2 - V_1\right) \tag{26}$$

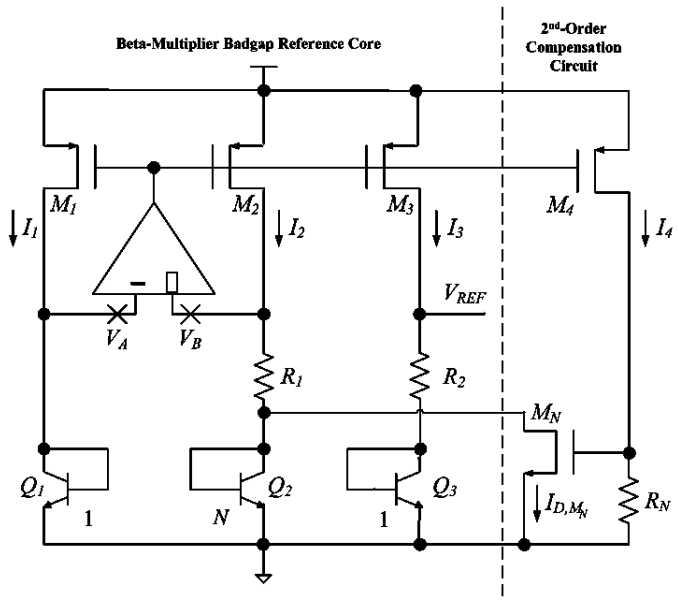

Fig. 8. Second Order Compensated Voltage Reference

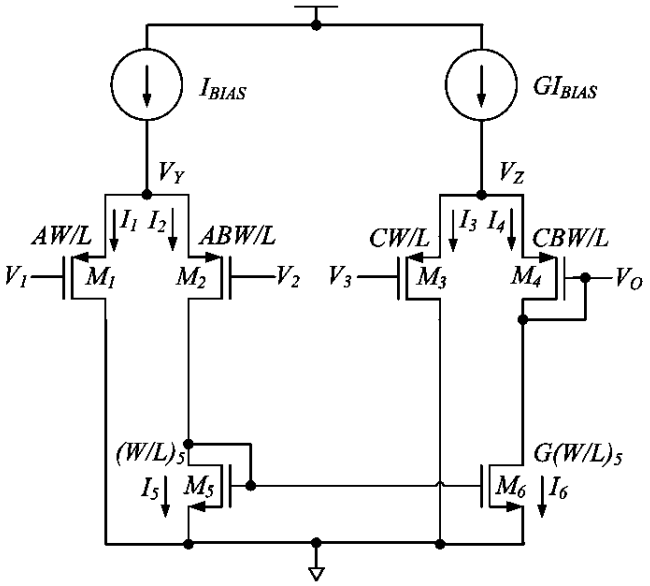

Fig. 9. Inverse Function Technique

which is obtained through a cancellation of terms like threshold voltages and mobilities, indicating that it is a fully linear relation.

For the resistorless voltage source using inverse function, Figure 11, we note that from Equation 27, V_{OUT} is a multiple of V_T, indicating that V_{OUT} is a $PTAT$ voltage.

$$\begin{aligned} V_{OUT} &= \sqrt{\frac{AG}{C}}\left(V_{BE_2} - V_{BE_1}\right) \\ &= \sqrt{\frac{AG}{C}}\ln\left(\frac{I_{BE_2}}{I_{BE_1}}\right)V_T \\ &= MV_T \end{aligned} \tag{27}$$

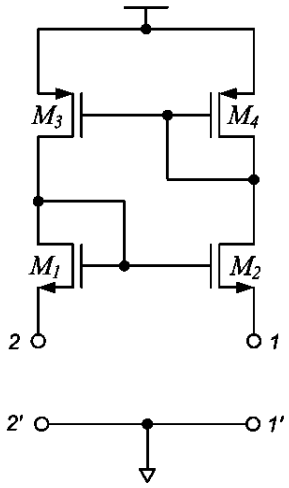

Fig. 10. Negative Impedance Converter

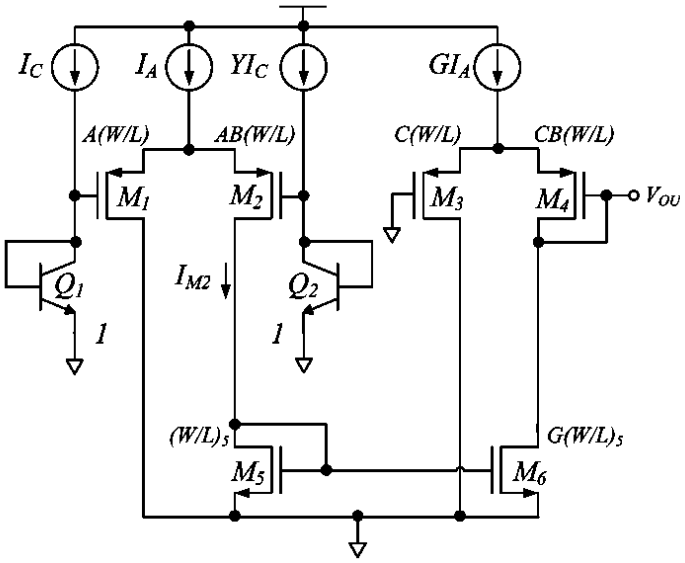

Fig. 11. Resistorless Voltage Source using Inverse Function

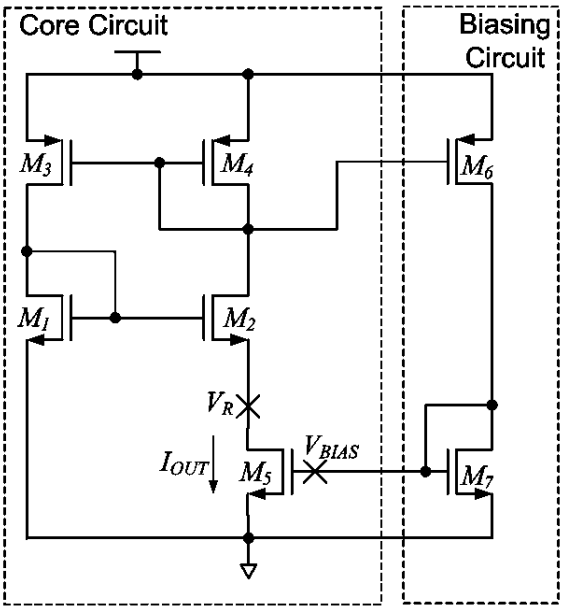

Fig. 12. Resistorless Current Source using NIC

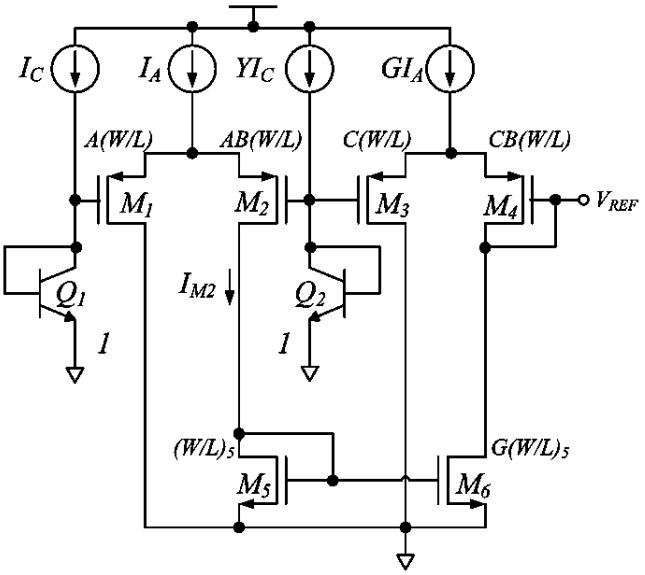

Fig. 13. Voltage Source based Voltage Reference

Simply connecting gate of the M_3 to V_{BE_2}, what we have is a voltage reference circuit, shown in Figure 13. Its governing equation is in Equation 28.

$$V_{REF} = V_{BE_2} + \sqrt{\frac{AG}{C}}\left(\Delta V_{BE_{2,1}}\right) = V_{BE_2} + MV_T \quad (28)$$

For the current source using NIC, by operating M_5 in linear region, shown in 12, we have a resistor-like relation as seen from Equation 29 [1].

$$I_{OUT} = \frac{V_{DS_5}}{R_{ON_5}} \quad (29)$$

IV. STATE OF THE ART CIRCUITS

A. Ultra Low Power

Cao'18 [8]: Cao et al. [8] present a 0.8V supply, ultra-low-power voltage reference for IoT applications. A standard 0.18μm CMOS process is used. 621mV reference voltage is provided by the reference, and it has a temperature coefficient of 13ppm/°C between -45°C and 120°C. It only consumes 4nW power. Circuit is shown in Figure 15 with a reference voltage given in Equation 30. The summary of the design parameters are given in Table II.

$$V_{REF} = \frac{V_{eb}}{2} + 3\eta V_T \ln\left(\frac{K_{D1}K_{M2}}{K_{D2}K_{M1}}\right) \quad (30)$$

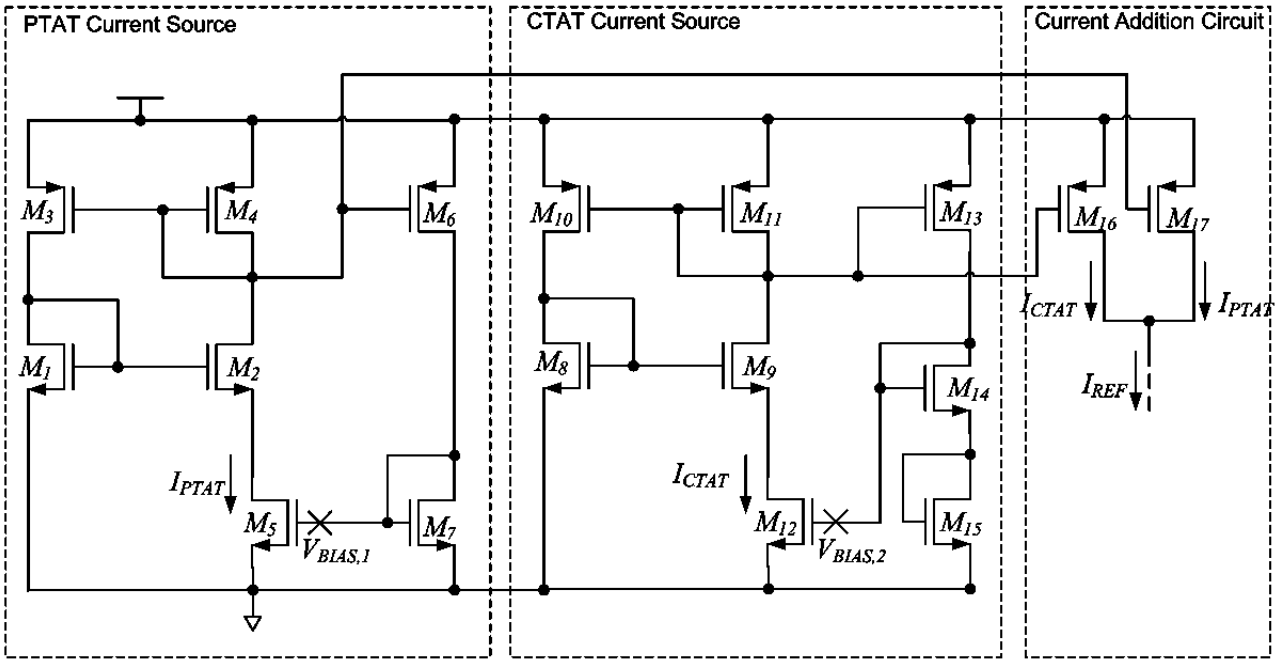

Fig. 14. Current Source based Voltage Reference

The architecture of the design includes an auxiliary bandgap voltage reference, an low-dropout regulator and a bandgap core. Auxiliary bandgap voltage reference creates a voltage of 198mV with low accuracy, then LDO receives this voltage and generates a fixed 1V for bandgap core. In this way, a high precision reference voltage can be obtained. BGR core consists of three blocks, namely current bias circuit, CTAT voltage generator, and 3-stage PTAT voltage generator as seen in Figure 15. Its prominent feature is to have 4nW power consumption, which can be used in applications such as biomedical and IoT [8].

TABLE II
SUMMARY OF DESIGN PARAMETERS

Parameters	**Cao'18 [8]**
Technology	0.18μm
Supply Voltage (V)	0.8
Reference Voltage (V)	0.621
Temperature Range (°C)	-45 a 120
TC (ppm/°C)	13
LNR (%/V)	0.107
PSRR@100Hz (dB)	-49
Power (nW)	4
Chip Area (mm^2)	0.0308

Chatterjee'17 [9]: Chatterjee et al. [9] present a 120nW ultra-low-power voltage reference with a high tolerance for PVT-variations. 180nm mixed-mode CMOS technology is used. 350.8mV reference voltage is provided by the reference, and it has a temperature coefficient of 76ppm/°C between 0°C and 70°C. It only consumes 120nW power. Circuit is shown in Figure 16 with a reference voltage given in Equation 31. The summary of the design parameters are given in Table III.

$$V_{REF} = \left(\frac{C_1 \cdot V_{PTAT}}{C_1 + C_2} + \frac{C_2 \cdot V_{CTAT}}{C_1 + C_2} \right) \tag{31}$$

The proposed circuit uses a PTAT and CTAT voltage and their sum to obtain a temperature-invariant reference voltage. It contains CTAT and PTAT voltage generators, supply independent current generator, and switched capacitor based averager circuit. High tolerance for PVT-variation is obtained by a switching circuit which changes the bias current of a key component. CTAT and PTAT voltages obtained from the generators are averaged by switched capacitor circuit as shown in Equation 31. Also, their proposed architecture is scalable and they analyze the performance of scaled technologies such as 65nm bulk CMOS and 28nm FD-SOI in their paper. What is deeply analyzed is noise attenuation performance of the circuit, which is high as compared the others presented here, 60dB PSNA is obtained [9].

TABLE III
SUMMARY OF DESIGN PARAMETERS

Parameters	**Chatterjee'17 [9]**
Technology	0.18μm
Supply Voltage (V)	0.8-1.8
Reference Voltage (mV)	350.8
Temperature Range (°C)	0 a 75
TC (ppm/°C)	76
LNR@27°C (%/V)	0.3
PSNA@100Hz (dB)	-65
Power@0.8V (nW)	120
Chip Area (mm^2)	0.023

De Oliveira'17 [11]: De Oliveira et al. [11] present the design and implementation of a pico-power, 0.45–0.6V

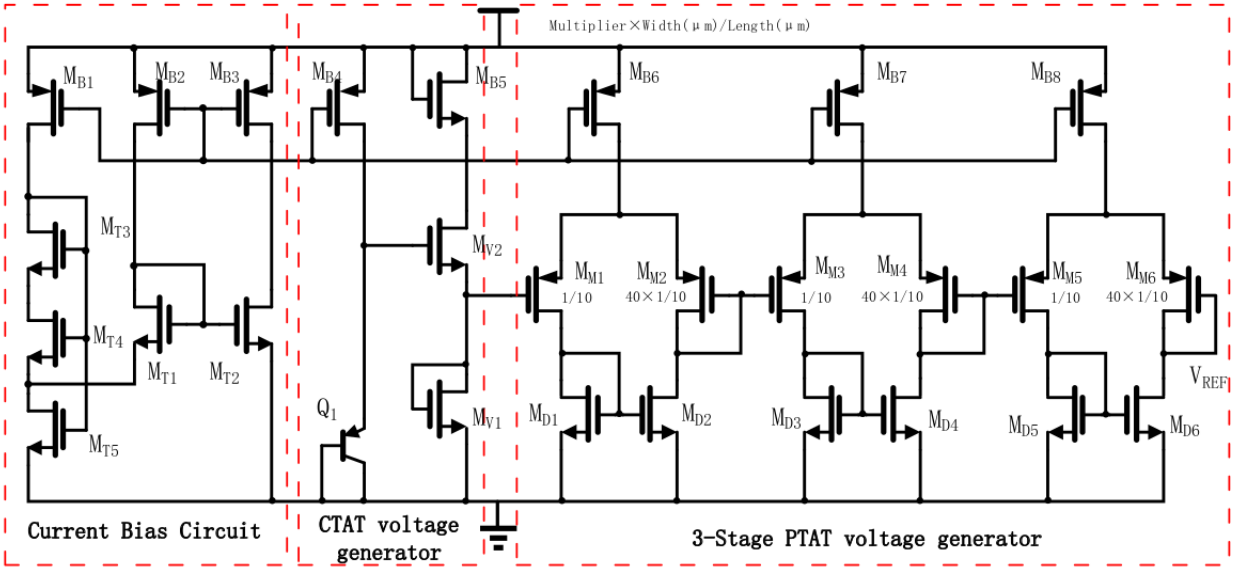

Fig. 15. Cao'18 [8]

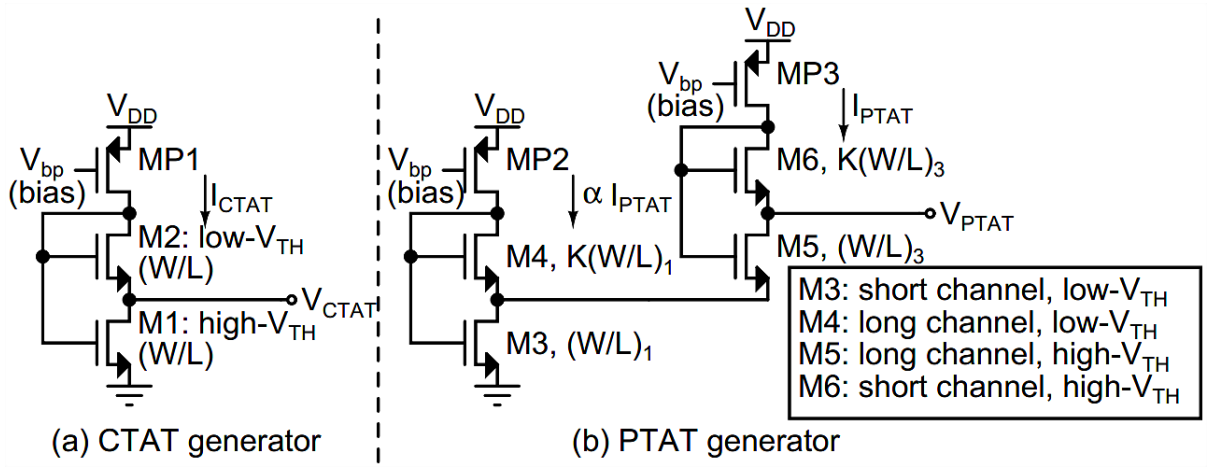

Fig. 16. Chatterjee'17 [9]

self-biased subthreshold CMOS voltage reference. Standard 0.18μm CMOS technology is used. 225.3mV reference voltage is provided by the reference, and it has a temperature coefficient of 104ppm/°C between 0°C and 120°C. It only dissipates 54.8pW. Circuit is shown in Figure 17 with a reference voltage given in Equation 32. The summary of the design parameters are given in Table IV.

$$V_{\mathrm{REF}} = \frac{V_{T2}(T_0) - V_{T3}(T_0)}{n_{3\varepsilon}} + \left(\frac{n_3 - n_2}{n_1 n_3 \varepsilon}\right) V_{T1}(T_0) + T_0 \left(\frac{n_1(\alpha_{T2} - \alpha_{T3}) - (n_2 - n_3)\alpha_{T1}}{n_1 n_3 \varepsilon}\right) \quad (32)$$

The authors gives two different variation for the core, which are self-biased self-cascode voltage reference, SBSCM, and self-biased NMOS load voltage reference, SBNMOS. Given parameters in Table IV and voltage reference in Equation 32 belong to SBSCM. A pico-watt circuit is proposed to for a demand of voltage references in IoT. The target for this voltage reference is low-voltage, low-power applications. It is achieved by using subthreshold operation in both cases. Trimming analysis of both circuits are done from 24 samples. Furthermore, they calculate a figure of merit and state that both circuits are among best circuits in the literature [11].

TABLE IV
SUMMARY OF DESIGN PARAMETERS

Parameters	De Oliveira'17 [11]
Technology	0.18μm
Supply Voltage (V)	0.45
Reference Voltage (mV)	225.3
Temperature Range (°C)	0 a 120
TC (ppm/°C)	104
Line Sensitivity (%/V)	0.15
PSRR@100Hz (dB)	-43.9
Power (pW)	54.8
Chip Area (mm^2)	0.002

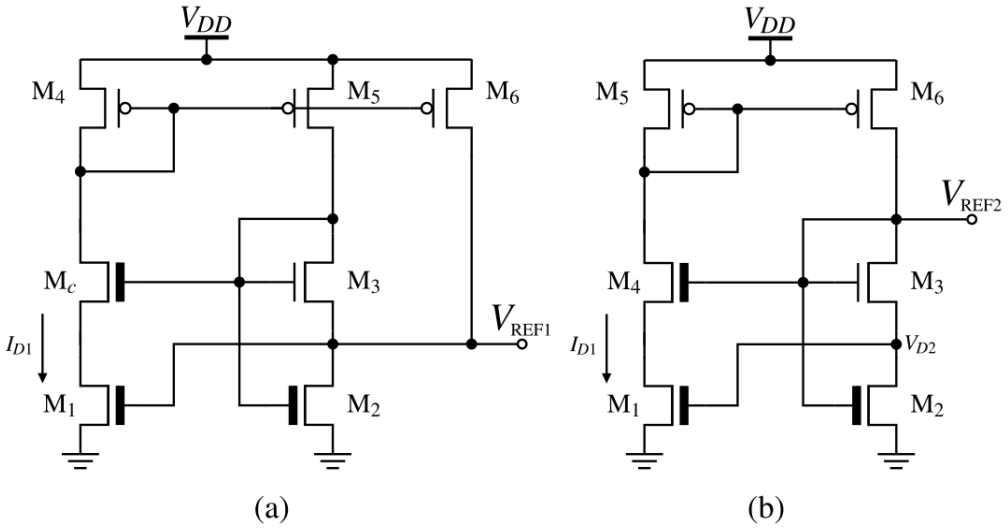

Fig. 17. De Oliveira'17 [11]

Duan'17 [12]: Duan et al. [12] present the design and implementation of a pico-power 0.8V all-CMOS voltage reference with -55dB PSRR. Standard 0.18μm CMOS technology is used. 328mV reference voltage is provided by the reference, and it has a temperature coefficient of 33.8ppm/°C between 10°C and 100°C. It only dissipates 79pW. Circuit is shown in Figure 18 with a reference voltage given in Equation 33. The summary of the design parameters are given in Table V.

$$\begin{aligned} V_{REF} &= V_{GS,R2} - V_{GS,R1} \\ &= \Delta V_{TH} + \eta V_T \ln\left(\frac{K_{R1} \cdot t_{OX,R2}}{K_{R2} \cdot t_{OX,R1}}\right) \end{aligned} \tag{33}$$

There are two current sources to obtain two PTAT currents, and a reference voltage that is independent of temperature is attained by substracting those PTAT currents and changing the current to a voltage value, i.e. reference voltage. So, it can be seperated as follows: PTAT-A current source, PTAT-B current source, reference voltage generator and a start-up circuit. Cascode structure is used to increase PSRR. To get rid of the resistors, transistors with deep-triode region are used so that TC of resistors can be ignored. The prominent of this circuit is that it has a pico-watt operation with a high PSRR, and quiescent current is in nano-ampere level [12].

TABLE V
SUMMARY OF DESIGN PARAMETERS

Parameters	**Duan'17 [12]**
Technology	0.18μm
Supply Voltage (V)	0.8-3.3
Reference Voltage (mV)	328
Temperature Range (°C)	10 a 100
TC (ppm/°C)	33.8
LNR@27°C (%/V)	0.21
PSRR@100Hz (dB)	-55
Power (nW)	79
Chip Area (mm^2)	0.014

Liu'17 [15]: Liu et al. [15] present the design and implementation of a ultra-low-power voltage reference with only 4.6nW power dissipation. Standard 0.18μm CMOS technology is used. 755mV reference voltage is provided by the reference, and it has a temperature coefficient of 34ppm/°C between -15°C and 140°C with an active area of 0.0598 mm^2. Circuit is shown in Figure 19 with a reference voltage given in Equation 34. The summary of the design parameters are given in Table VI.

$$V_{\text{ref}} = V_{\text{gap}} - \frac{V_{\text{th0}} + \alpha T_0}{m} \tag{34}$$

PTAT voltage is generated from a transistor having a zero gate-source voltage and its subthreshold leakage current and another diode-like connected transistor. CTAT voltage is generated from the body diodes of another transistor. With the assistance of an OTA, reference voltage is obtained from these PTAT and CTAT generators. It is a pure CMOS implementation, meaning that chip area is exclusively small. It is an appealing voltage reference for ultra-low-power applications [15].

TABLE VI
SUMMARY OF DESIGN PARAMETERS

Parameters	**Liu'17 [15]**
Technology	0.18μm
Supply Voltage (V)	1.1
Reference Voltage (mV)	755
Temperature Range (°C)	-15 a 140
TC (ppm/°C)	34
LNR@27°C (%/V)	0.28
PSRR@10Hz (dB)	-9
PSRR@1MHz (dB)	-47
Power (nW)	4.6
Chip Area (mm^2)	0.0598

Seok'12 [21]: Seok et al. [21] present a portable 2-transistor, picowatt power voltage reference with an operating

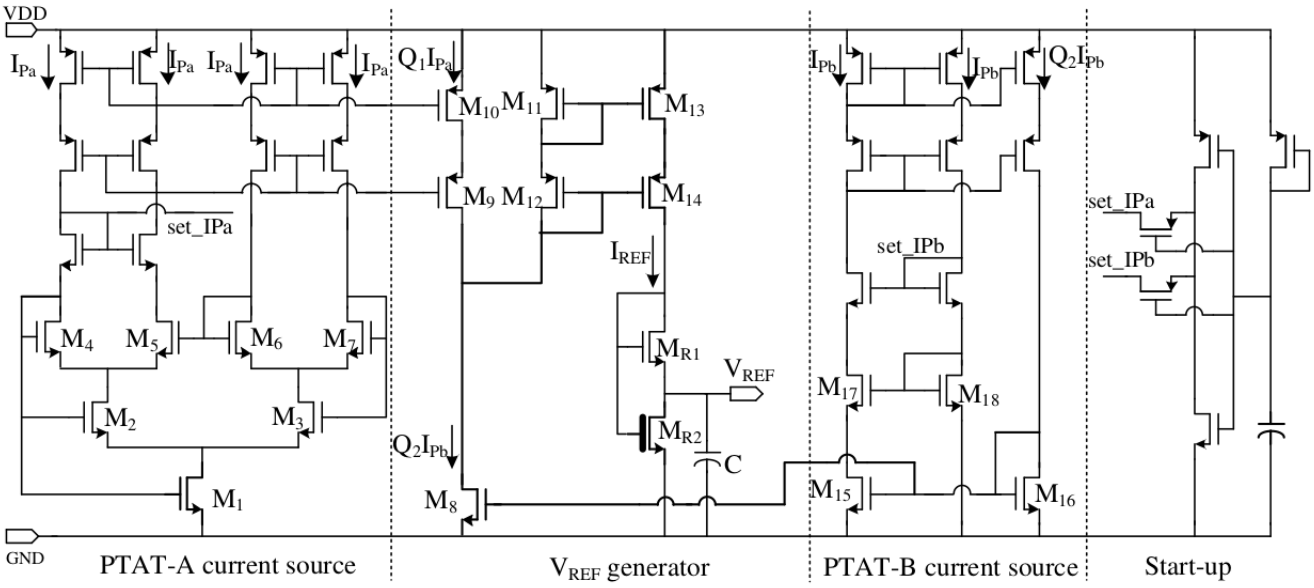

Fig. 18. Duan'17 [12]

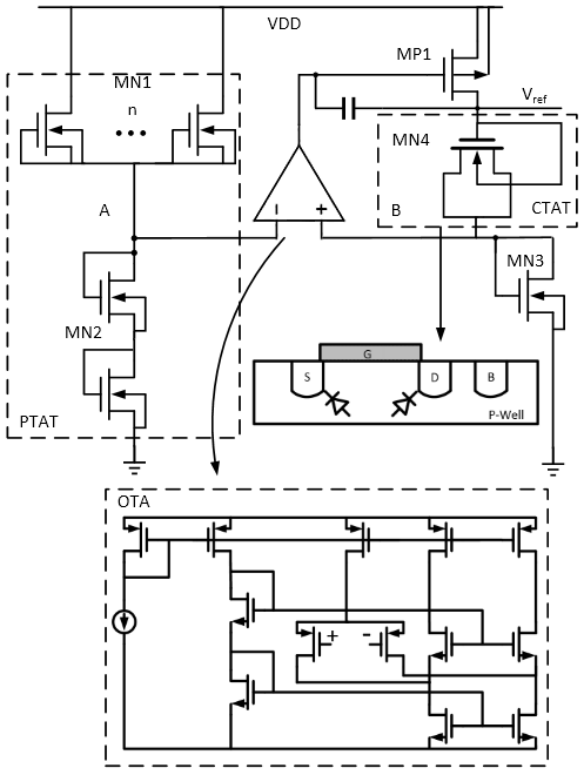

Fig. 19. Liu'17 [15]

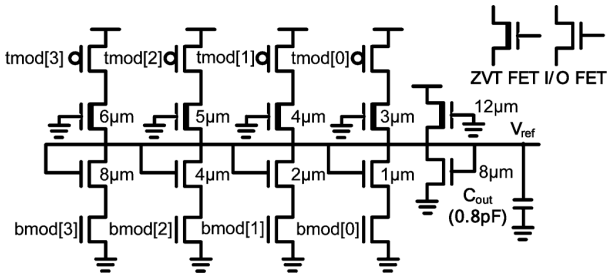

Fig. 20. Seok'12 [21]

voltage 0.5V. Simulations and experiments over a wide range of technologies are represented. 175mV reference voltage is provided by the reference, and it has a temperature coefficient of 5.3ppm/°C between -20°C and 80°C after post-trimming. Voltage reference is shown in Figure 20 with a reference voltage given in Equation 35. The summary of the design parameters are given in Table VII for 0.13μm CMOS technology.

$$V_{\text{ref}} = \frac{m_1 m_2}{m_1 + m_2}\left[(V_{\text{th2}} - V_{\text{th1}}) + V_T \ln\left(\frac{\mu_1 C_{\text{ox1}} W_1 L_2}{\mu_2 C_{\text{ox2}} W_2 L_1}\right)\right] \tag{35}$$

Main goal of this design is to implement a voltage reference for areas with limited energy sources like biomedical sensor applications, which also requires minimized areas, especially in implantable applications. Proposed method does not include any amplifier, start-up circuit or resistors, it has only two transistors. One of them is a native NFET and the other is thick oxide input/output (I/O) NFET. Equation 35 is obtained, where threshold voltage is complementary and the other term is proportional to temperature. It is a challenge to maintain a good temperature coefficient, line sensitivity, and power supply rejection ratio at the same and this voltage reference achieves that with only 2-transistor structure [21].

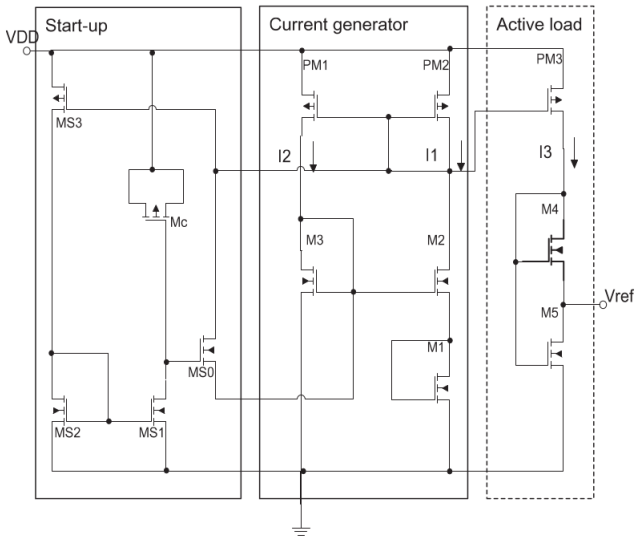

Fig. 21. Zeng'13 [27]

TABLE VII
SUMMARY OF DESIGN PARAMETERS

Parameters	Seok'12 [21]
Technology	0.13μm
Supply Voltage (V)	0.5
Reference Voltage (mV)	175
Temperature Range (°C)	-20 a 80
TC (ppm/°C)	16.9
LNR@27°C (%/V)	0.036
PSRR@100Hz (dB)	-51
PSRR@10MHz (dB)	-64
Power (pW)	29.5
Chip Area (mm^2)	0.0093

Zeng'13 [27]: Zeng et al. [27] present an ultra-low power, resistorless subthreshold CMOS voltage reference. Standard 0.18μm CMOS process is adopted for fabrication. 202.7mV reference voltage is provided by the voltage reference, and it has a temperature coefficient of as low as 2.1ppm/°C between -20°C and 80°C. The power supply rejection ratio is not that bad. It is around -49dB at 100Hz without any filtering. Circuit is shown in Figure 21 with a reference voltage given in Equation 36. The summary of the design parameters are given in Table VIII.

$$V_{ref} = \Delta V_{TH} + \eta V_T \ln\left(\frac{K_4}{K_5}\right) \tag{36}$$

The circuit is composed of a start-up circuit, a current generator and an active load with the operation of all MOSFETs at subthreshold region. Core of the circuit is current generator and generated current is sent to active load part of the circuit to become a reference voltage. V_{TH} and V_T contribute to the reference voltage as a negative TC and positive TC respectively. It is suitable for ultra-low power and low temperature coefficient applications [27].

TABLE VIII
SUMMARY OF DESIGN PARAMETERS

Parameters	Zeng'13 [27]
Technology	0.18μm
Supply Voltage (V)	0.65-5
Reference Voltage (mV)	202.7
Temperature Range (°C)	-20 a 80
TC (ppm/°C)	2.1
Line Sensitivity (ppm/V)	5.4
PSRR@100Hz (dB)	-49
PSRR@10MHz (dB)	-39
Power (nW)	1.2
Chip Area (mm^2)	0.011

B. Ultra Low Voltage

Wang'15 [23]: Wang et al. [23] propose a low-voltage, low-power (0.45V, 14.6nW) CMOS subthreshold voltage reference with no resistors and no BJTs. Standard 0.18μm-1.8V CMOS process is used for fabrication. 118.46mV reference voltage is provided by the reference, and it has an average temperature coefficient of 63.6ppm/°C between -40°C and 125°C. The voltage reference has a good line regulation that is 1.2mV/V. Voltage reference is shown in Figure 22 with a reference voltage given in Equation 37. The summary of the design parameters are given in Table IX.

$$\begin{aligned} V_{REF} &= V_{GS,M12} - V_{GS,M11} \\ &= \gamma(\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{REF} - V_{GS,M14}}) + \eta V_T \ln\frac{K_{11}}{K_{12}} \end{aligned} \tag{37}$$

Main blocks of the VR can be summarized as 1)bulk-driven current generator 2)output stage 3)body bias circuit 4)start-up circuit. Different body bias voltages to control the threshold voltages of MOSFETs dynamically. In this way, inaccuracy will not be posed even in worst process corners, reference voltage variation will be insignificant. Generated current from bulk-driven circuit is mirrored into the output stage, which are two stacked NMOS transistors operating in subthreshold region. Its prominent feature is high precision with ultra low-voltage and ultra low-power [23].

TABLE IX
SUMMARY OF DESIGN PARAMETERS

Parameters	Wang'15 [23]
Technology	0.18μm
Supply Voltage (V)	0.45
Reference Voltage (mV)	118.46
Temperature Range (°C)	-40 a 125
TC (ppm/°C)	63.6
LNR@27°C (mV/V)	1.2
PSRR@100Hz (dB)	-44.2
Power (nW)	14.6
Chip Area (mm^2)	0.012

Zhu'16 [31]: Zhu et al. [31] propose a design for a 0.45V, nano-watt, 0.033% line sensitivity, MOSFET-only subthreshold voltage reference with no amplifiers. Standard 0.18μm-1.8V CMOS process is used. 118.45mV reference voltage is

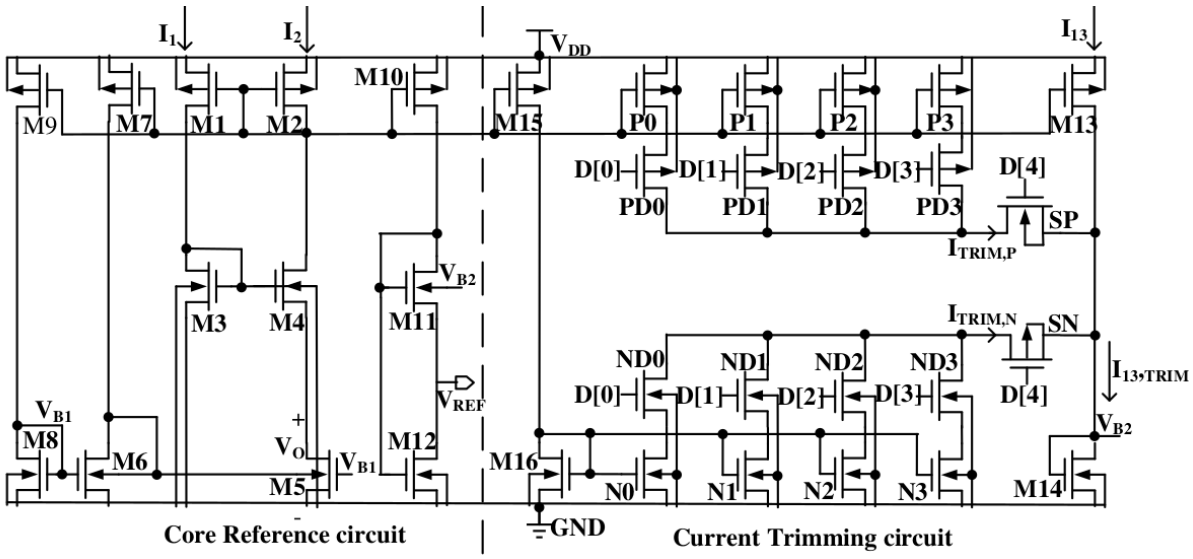

Fig. 22. Wang'15 [23]

provided by the voltage reference, and it has a temperature coefficient of 59.4ppm/°C between -40°C and 85°C. Circuit is shown in Figure 23 with a reference voltage given in Equation 38. The summary of the design parameters are given in Table X.

$$\begin{aligned} V_{\mathrm{REF}} =& V_{GS,\mathrm{M2}} - V_{GS,\mathrm{M1}} \\ =& \gamma(\sqrt{2\Phi_F} - \sqrt{2\Phi_F + V_{\mathrm{REF}} - V_{GS,\mathrm{M3}}}) \\ &+ \eta V_T \ln \frac{K_1}{K_2} \end{aligned} \tag{38}$$

The main blocks of the circuit is a single bulk-driven current generator, which is a low line sensitive current generator, an output stage, which subtracts two complementary currents, a body bias and a start-up circuit. For further temperature compensation, second-order compensation is used as in Section III-C. Supply and power are reduced by adopting bulk-driven technique and subthreshold operation. Process variation is compensated with trimming, and line sensitivity is not affected by this procedure. Ultra-low power, low power and high precision is what makes this circuit is appealing [31].

TABLE X
SUMMARY OF DESIGN PARAMETERS

Parameters	Zhu'16 [31]
Technology	0.18μm
Supply Voltage (V)	0.45-1.8
Reference Voltage (mV)	118.45
Temperature Range (°C)	-40 a 85
TC (ppm/°C)	59.4
Line Sensitivity (%/V)	0.033
PSRR@100Hz (dB)	-50.3
Power (nW)	15.61
Chip Area (mm^2)	0.0132

C. High PSRR

Alhassan'16 [2]: Alhassan et al. [2] present a sub-1V ultra-low-power and high PSRR voltage reference with a -51dB PSRR up to 60MHz. Standard 0.18μm-1.8V CMOS process is used. 489mV reference voltage is provided by the reference, and it has a temperature coefficient of 6.5ppm/°C between -30°C and 110°C, and a PSRR of 75dB at low frequencies. Circuit is shown in Figure 24 with a reference voltage given in Equation 39. The summary of the design parameters are given in Table XI.

$$V_{\mathrm{REF}} = V_{\mathrm{GSMN3}} = V_{\mathrm{THMN3}} + \sqrt{\frac{2\mathrm{MI}_{\mathrm{BIAS}}}{k_n S_{\mathrm{MN3}}}} \tag{39}$$

Since power supply noise is a huge issue for SoC application, high PSRR voltage references are needed for a wide spectrum for high precision. For instance, power supply and temperature sensitivity is radical for high resolution data acquisition systems, and this circuit is a proposal which can be used for those applications. Besides, to present a low-power voltage reference is even harder. That's why, Alhassan chooses not to use BJTs and go all-MOSFET. This proposal is a resistorless low-power nonbandgap voltage reference as in described Section III-D.

Subblocks can be summarized as a PTAT voltage generator, self-biased current source, start-up circuit, reference generator and leakage compensation, PSRR improvement with feedback, and a MOSFET low pass filter. To create a PTAT voltage, two dynamic threshold MOS transistors adopted and the difference between source-body voltages are taken as a PTAT voltage. Self-biased current source is the core of the voltage reference and a high PSRR is achieved by a feedback mechanism governed by this current source. Moreover, for high frequencies, as parasitic capacitances is in utmost effect, a MOSFET low pass filter is adopted in the voltage reference without adding any power consumption element [2].

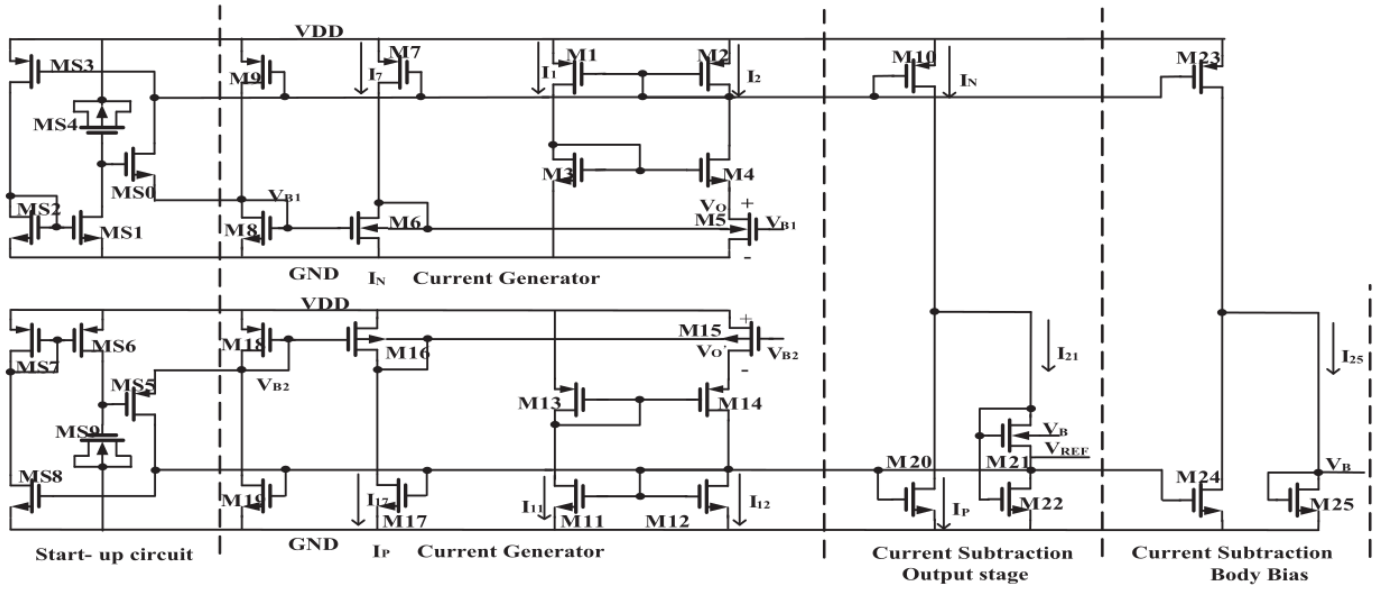

Fig. 23. Zhu'16 [31]

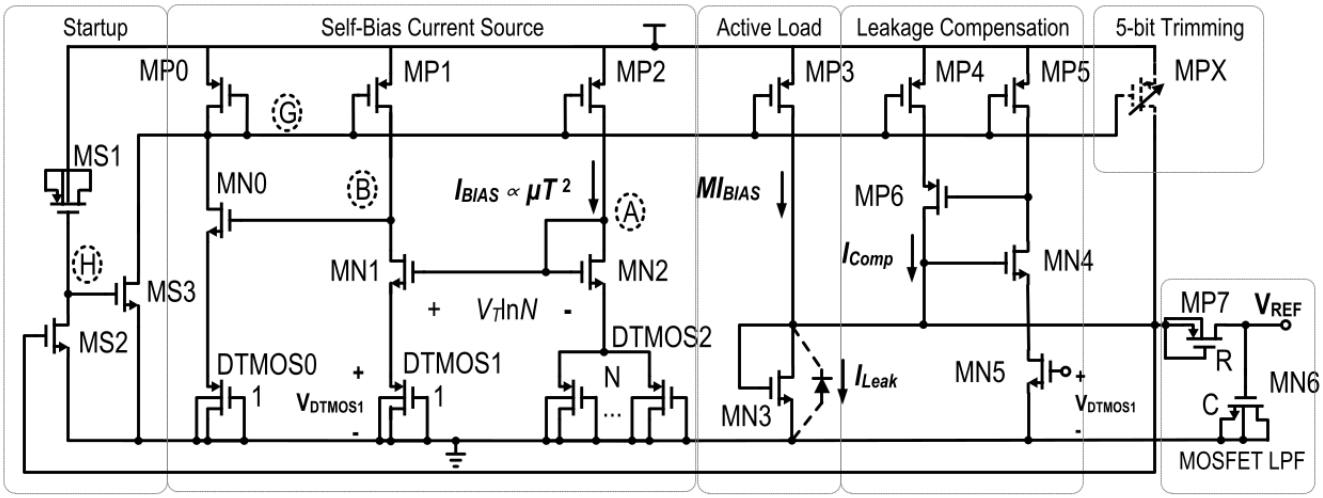

Fig. 24. Alhassan'16 [2]

TABLE XI
SUMMARY OF DESIGN PARAMETERS

Parameters	Alhassan'16 [2]
Technology	0.18μm
Supply Voltage (V)	0.8
Reference Voltage (mV)	489
Temperature Range (°C)	-30 a 110
TC (ppm/°C)	6.5
LNR (%/V)	0.076
PSRR@100Hz (dB)	-75
PSRR@100kHz (dB)	-61
PSRR@10MHz (dB)	-59
PSRR@60MHz (dB)	-51
Power (nW)	360
Chip Area (mm^2)	0.0143

Alhassan'16 [3]: Alhassan et al. [3] present a sub-1V ultra-low-power and high PSRR voltage reference with a -50dB PSRR up to 80MHz. Standard 0.18μm-1.8V CMOS process is used. 893mV reference voltage is provided by the reference, and it has a temperature coefficient of 19ppm/°C between -30°C and 80°C, and a PSRR of 75dB at low frequencies. Circuit is shown in Figure 25 with a reference voltage given in Equation 40. The summary of the design parameters are given in Table XII.

$$V_{REF} = V_{SGMP6} = |V_{THMP6}| + \sqrt{\frac{2MI_{BIAS}}{k_p S_{MP6}}} \qquad (40)$$

As in Alhassan'16 [2], the author suggest another ultra-low-power and high PSRR voltage reference for the demand

in SoC applications and lack of solutions to this problem. Its main objective is to suppress the effect of high frequency supply ripple. PTAT voltage is again extracted from MOSFETs and a composite transistor PTAT generator is used. A voltage to current converter with feedback is embodied, which helps to increase loop gain and thus improves PSRR. This bias current converted from a PTAT voltage is then transmitted to a reference voltage generator. For same reasons as in Alhassan'16 [2], a start-up circuit and a MOSFET low pass filter is added to the circuit [3].

TABLE XII
SUMMARY OF DESIGN PARAMETERS

Parameters	Alhassan'16 [3]
Technology	0.18μm
Supply Voltage (V)	1.1
Reference Voltage (mV)	893
Temperature Range (°C)	-30 a 80
TC (ppm/°C)	19
LNR (%/V)	0.093
PSRR@100Hz (dB)	-75
PSRR@100kHz (dB)	-58
PSRR@10MHz (dB)	-60
PSRR@80MHz (dB)	-50
Power (nW)	550
Chip Area (mm^2)	0.0180

Basyurt'14 [5]: Basyurt et al. [5] present a bulk-isolated curvature-corrected bandgap voltage reference. A 0.35μm-3.3V triple-well CMOS process is used. 201mV reference voltage is provided by the bandgap reference, and it has a temperature coefficient of 6.2ppm/°C between -40°C and 125°C. Circuit is shown in Figure 26 with a reference voltage given in Equation 41. The summary of the design parameters are given in Table XIII.

$$V_{OUT} = (I_{CTAT} + I_{PTAT})\, R_{OUT} \tag{41}$$

where

$$I_{CTAT} = \frac{V_{g0}}{R_1} - \frac{V_{g0} - \eta V_{BE1_1Tr} + (\eta - 1)V_{BE2\_Tr}}{R_1}\frac{T}{Tr}$$

$$I_{PTAT} = \frac{kT}{q}\frac{\ln(N)}{R_0}$$

BGR consists of a core with two amplifiers, a main and an auxiliary amplifier, and a curvature-compensation part along with a start-up circuit. It is a current mode BGR, which means it creates PTAT and CTAT currents and adds them. CTAT current is obtained from the base-emitter junction of a BJT and PTAT current is obtained from BJTs by driving them with different current densities. In the paper, the authors make minimum voltage, power, stability, noise, and PSRR analysis of the BGR. By employing bulk isolation strategy, the substrate noise sensitivity at the output of the voltage reference is improved more than 100dB up to 100MHz, which is what make this circuit distinct [5].

TABLE XIII
SUMMARY OF DESIGN PARAMETERS

Parameters	Basyurt'14 [5]
Technology	0.35μm
Supply Voltage (V)	2
Reference Voltage (V)	0.201
Temperature Range (°C)	-40 a 125
TC (ppm/°C)	6.2
Line Regulation (ppm/V)	690
PSRR@100Hz (dB)	-76.5
Power (μW)	103.95
Chip Area (mm^2)	0.165

Jing'12 [13]: Jing et al. [13] present a 0.5V nano-watt 4-transistor CMOS voltage reference with two high PSRR outputs. It is implemented with 0.13μm CMOS technology. 85.5/182mV reference voltages are provided by the reference, and it has a temperature coefficient of 52.5/32 ppm/°C between 0°C and 100°C. It only has a nanoampere quiescent current. Circuit is shown in Figure 27 with a reference voltages given in Equations 42 and 43. The summary of the design parameters are given in Table XIV.

$$V_{ref1} = \frac{2}{3} \times (V_{TH10} - V_{TH00}) \tag{42}$$

$$V_{ref2} = \frac{1}{3} \times (V_{TH10} - V_{TH00}) \tag{43}$$

It is fascinating that simple 4-transistor voltage reference can have two high PSRR outputs. Out of 4 transistors, one of them has a low threshold voltage, while the others have normal threshold voltages. Zero temperature coeeficient is obtained by substracting these different threshold voltages with the help of the thermal voltage [13].

TABLE XIV
SUMMARY OF DESIGN PARAMETERS

Parameters	Jing'12 [13]
Technology	0.13μm
Supply Voltage (V)	0.5-1.2
Reference Voltage (mV)	85.5/182
Temperature Range (°C)	0 a 100
TC (ppm/°C)	52.5/32
LNR@27°C (%/V)	0.104/0.095
PSRR@100Hz (dB)	-70.4/-63.8
PSRR@100kHz (dB)	-98/-77
PSRR@10MHz (dB)	-112/-110
Quiescent Current (nA)	3
Chip Area (mm^2)	small (4T VR)

Yusoff'12 [28]: Yusoff et al. [28] present a low-temperature coefficient, and high PSRR bandgap voltage reference. Standard 0.18μm-1.8V CMOS process is used. 1.204V reference voltage is provided by the BGR, and it has a temperature coefficient of below 6.5ppm/°C between -20°C and 90°C, and a PSRR of more than 80dB at low frequencies. Circuit is shown in Figure 28 with a reference voltage given in Equation 44. The summary of the design parameters are given in Table XV.

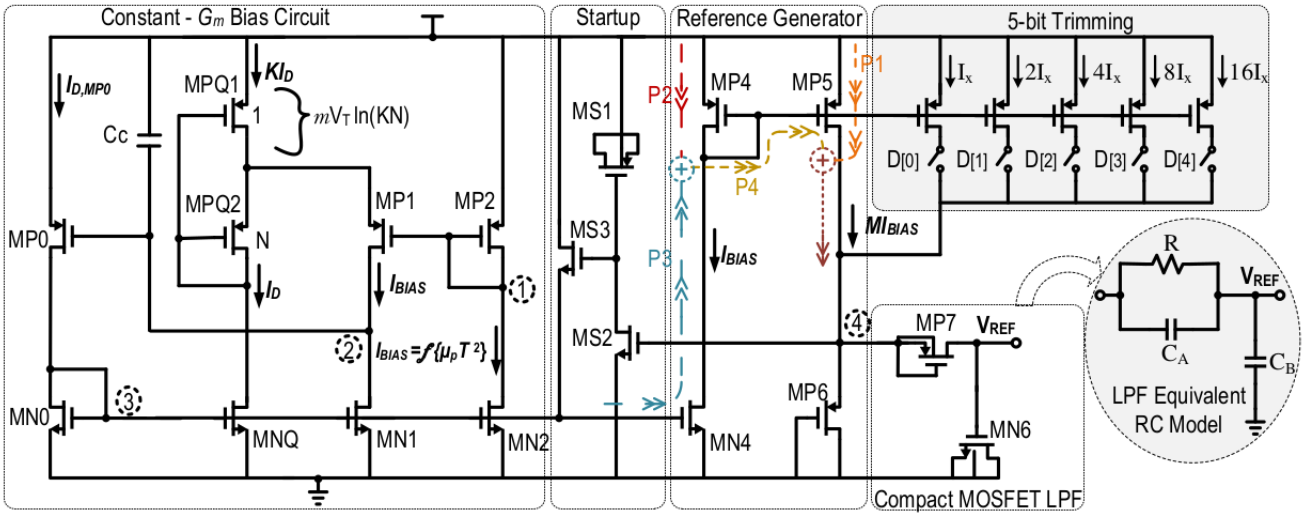

Fig. 25. Alhassan'16 [3]

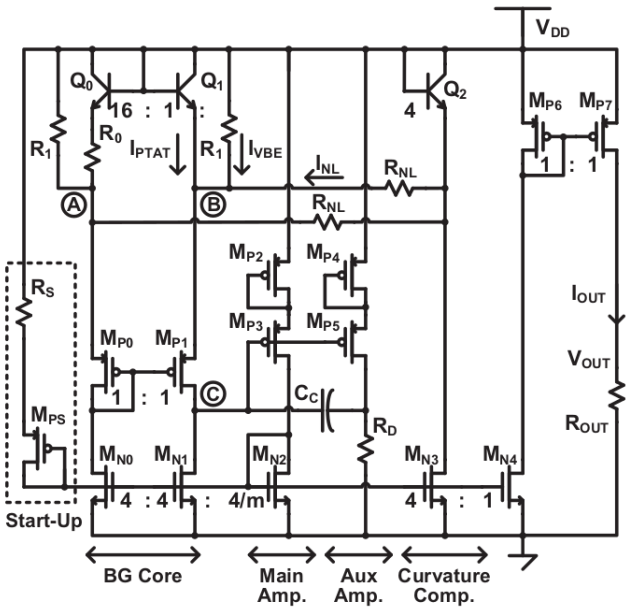

Fig. 26. Basyurt'14 [5]

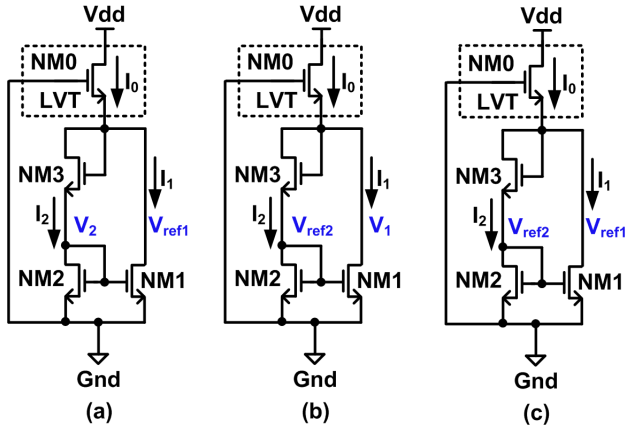

Fig. 27. Jing'12 [13]

$$V_{REF} = V_{BE2} + \left(1 + \frac{R_2}{R_3}\right)(V_T \ln n - V_{OS}) \qquad (44)$$

In this circuit, main blocks are a bandgap core, a start-up circuit and a power down circuit. Bandgap core has a two-stage amplifier so that it can have a high gain, which enables a high PSRR, and reduces errors in reference voltage. Two-stage amplifier used in the core is a standard differential amplifier with Miller compensation. Start-up circuit appears for a proper operation, and power down circuit is placed to reduce the power consumption.

While arranging the layout, parasitic resistances are taken into account so that mismatches for opamp do not create a problem. Common centroid technique is used for best matching. Resistor dummies are placed with same material and widths to improve further resistor matching. Simulations are done by SPECTRE and compared with experimental results. High PSRR is the prominent feature of this circuit [28].

TABLE XV
SUMMARY OF DESIGN PARAMETERS

Parameters	Yusoff'12 [28]
Technology	0.18μm
Supply Voltage (V)	1.8
Reference Voltage (V)	1.204
Temperature Range (°C)	-20 a 90
TC (ppm/°C)	6.1
LNR@27°C (mV/V)	4
PSRR@1kHz (dB)	-84
Power (μW)	150
Chip Area (mm^2)	0.111

Zhu'14 [30]: Zhu et al. [30] present a -115dB PSRR CMOS bandgap reference. Standard 0.18μm-1.8V CMOS process is

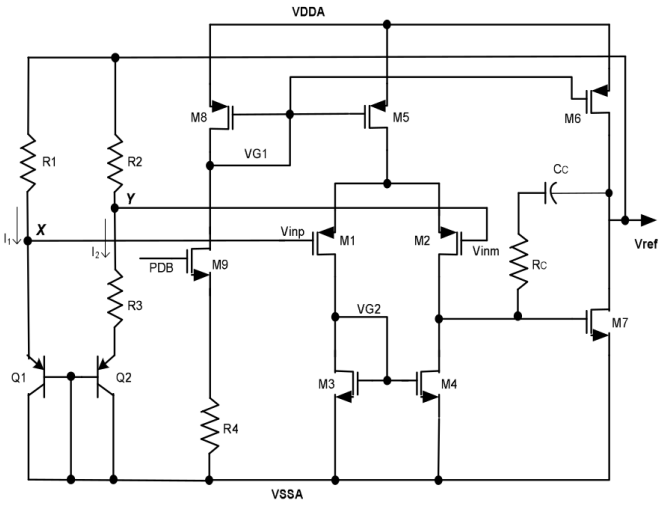

Fig. 28. Yusoff'12 [28]

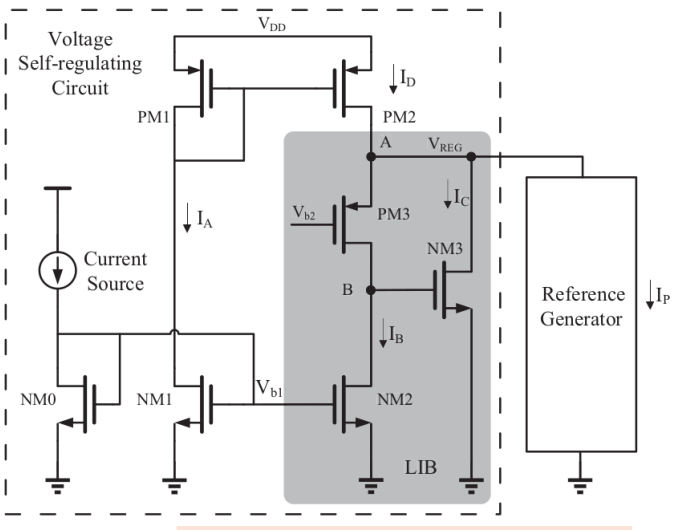

Fig. 29. Zhu'14 [30]

used. 1.176V reference voltage is provided by the BGR, and it has a temperature coefficient of 11.6ppm/°C between -40°C and 125°C, and a PSRR of 115dB at low frequencies. Circuit is shown in Figure 29 with a reference voltage given in Equation 45. The summary of the design parameters are given in Table XVI.

$$V_{BG} = V_{BE3} + M\frac{R_4}{R_3}V_T \ln(N) \tag{45}$$

By using modern SoC, analog circuits are placed in a noisy environment, and noise from power lines are unavoidable, which results in a need for high PSRR reference circuits for a steady reference voltage. This voltage reference circuit suggested by Zhu [30] achieves a high PSRR even in high frequencies by adopting a voltage self-regulating technique. It does not use any operational amplifiers or filtering capacitances, rather uses a voltage self-regulating circuit along with an improved start-up circuit to improve PSRR. PSRR calculated in the paper is as in Equation 46 and a high PSRR can be achieved by choosing long-channel devices for PM2 and PM3 as in Figure 29 [30].

$$PSRR \approx -20\lg\left(\frac{g_{m\_PM3} \times g_{m\_NM3}}{g_{ds\_PM3} \times g_{ds\_PM2}} + 1\right) \tag{46}$$

TABLE XVI
SUMMARY OF DESIGN PARAMETERS

Parameters	Zhu'14 [30]
Technology	0.18μm
Supply Voltage (V)	3.3
Reference Voltage (V)	1.176
Temperature Range (°C)	-40 a 125
TC (ppm/°C)	11.6
PSRR@DC (dB)	-115
PSRR@1MHz (dB)	-90
Power (μW)	277.2
Chip Area (mm^2)	0.0014

D. High Precision

Li'18 [14]: Li et al. [14] present the design and implementation of a low line regulation voltage reference with no amplifier. Standard 0.18μm CMOS technology is used. 902mV reference voltage is provided by the reference, and it has a temperature coefficient of 3.6ppm/°C between -50°C and 120°C. Circuit is shown in Figure 30 with a reference voltage given in Equation 47. The summary of the design parameters are given in Table XVII.

$$V_{\text{ref}} = V_{\text{EB1}} + (I_{\text{PTAT}} - I_5) \cdot R_2 \tag{47}$$

To design a low line regulation voltage reference, high-order curvature compensation techniques should be in use as described in Section III-C. By using extra operational amplifiers and exponential or piecewise compensation techniques, several approaches are tested by the others. Here, the authors propose a circuit without any operational amplifiers. Proposed VR includes a start-up circuit, first-order compensation block, high-order compensation block and CTAT current generator block. To decrease the area only one BJT in first-order compensation block is used for the procedure and MOSFETs working in subthreshold region are employed. It is a high precision voltage reference for extreme environments [14].

TABLE XVII
SUMMARY OF DESIGN PARAMETERS

Parameters	Li'18 [14]
Technology	0.18μm
Supply Voltage (V)	1.7-3.5
Reference Voltage (V)	0.902
Temperature Range (°C)	-50 a 120
TC (ppm/°C)	3.6-7.4
LNR@27°C (mV/V)	0.005
PSRR@1kHz (dB)	-80
Power (μW)	115
Chip Area (mm^2)	0.003

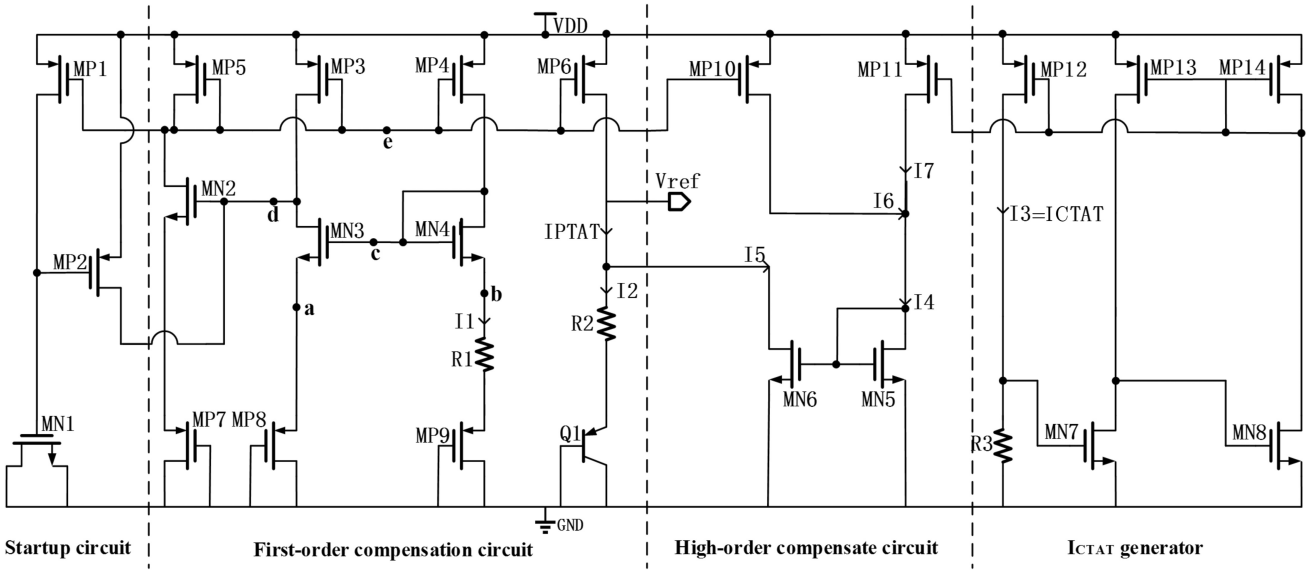

Fig. 30. Li'18 [14]

Xie'14 [24]: Xie et al. [24] propose a low power CMOS voltage reference generator with temperature and process compensation. Standard 0.18μm-1.8V CMOS process is used for fabrication. 193.95mV reference voltage is provided by the reference, and its best temperature coefficient is 9.77ppm/°C between -40°C and 85°C. The voltage reference has a good line regulation that is 0.036mV/V, high precision is tried to be obtained by process compensation. Voltage reference is shown in Figure 31 with a reference voltage given in Equation 48. The summary of the design parameters are given in Table XVIII.

$$V_{REF} = \Delta V_{th} + mV_T \ln\left(\frac{t_{OX1}K_2}{t_{OX2}K_1}\right) - V_{com} \qquad (48)$$

where compensation voltage is found as

$$V_{com} = \frac{R_2}{R_1} V_{th6}$$

Architecture of the voltage reference proposed by the authors includes a current source and a reference generator along with a start-up circuit. While current source generates a current proportional to threshold voltage, reference generator creates a reference voltage by this current and process compensation. Process compensation is well put, it achieves a maximum deviation of 0.35% for different process corners. Its main area of usage is low-cost, high-precision applications [24].

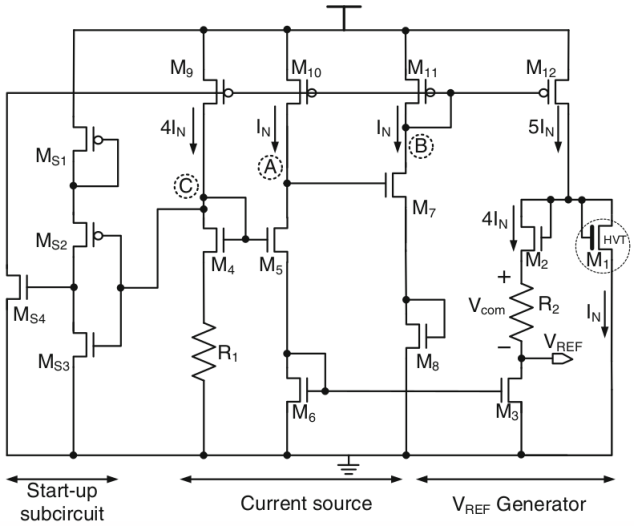

Fig. 31. Xie'14 [24]

TABLE XVIII
SUMMARY OF DESIGN PARAMETERS

Parameters	Xie'14 [24]
Technology	0.18μm
Supply Voltage (V)	1.2-2.5
Reference Voltage (mV)	193.95
Temperature Range (°C)	-40 a 85
TC (ppm/°C)	9.77-36.66
LNR@27°C (mV/V)	0.036
PSRR@100Hz (dB)	-49.6
Power (μW)	0.975
Chip Area (mm^2)	0.0219

Zhang'12 [29]: Zhang et al. [29] present a low-voltage, and high order curvature compensated bandgap voltage reference. 0.5μm BiCMOS process is used. Low voltages down to

1.285V reference voltage is provided by the BGR, and it has a temperature coefficient of below 7ppm/°C between -40°C and 110°C. Circuit is shown in Figure 32 with a reference voltage given in Equation 49. Sub-blocks of the circuit are start-up, auxiliary BGR, ECC, piecewise LCC, and I-V converter. The summary of the design parameters are given in Table XIX.

$$V_{\mathrm{REF}} = \left\{ \begin{array}{ll} DC, & T < T_1 \\ EV_T \ln(AT/C) + FC, & T \geq T_1 \end{array} \right\} \quad (49)$$

where $D = \alpha R_6/R_4 + \delta\left(R_5 + R_6\right)/R_4, E = R_6/R_1, F = \delta\left(R_5 + R_6\right)/R_4.\delta, D, E$, and F are temperature-independent constants and T_1 is the cross temperature. Normally, in BGRs like in Widlar and Brokaw proposed, first order compensation is used as mentioned in Section III-C. However, it is not enough to get low temperature coefficients with first order compensation. One can choose to use piecewise compensation as in this proposed bandgap reference. Firstly, to reduce temperature drift, exponential curvature compensation (ECC) is used. Then, logarithmic curvature compensation (LCC) is used to reduce further. Thus, reduction in temperature drift is obtained for a wide temperature range. Prominent feature of the proposed reference is high precision [29].

TABLE XIX
SUMMARY OF DESIGN PARAMETERS

Parameters	Zhang'12 [29]
Technology	0.5μm BiCMOS
Supply Voltage (V)	3.6
Reference Voltage (V)	1.285
Temperature Range (°C)	-40 a 110
TC (ppm/°C)	5
LNR@27°C (mV/V)	0.059
PSRR@1kHz (dB)	-70
Power (μW)	125
Chip Area (mm^2)	0.04

E. LVLP

Andreou'13 [4]: Andreou et al. [3] present all-subthreshold CMOS voltage reference with a compensation of third order curvature. Standard 0.35μm-3.3V CMOS process is used. 259mV reference voltage is provided by the reference, and it has a temperature coefficient of 2ppm/°C between -45°C and 145°C, which is a very wide temperature range. Moreover, its power consumption is 2μW. Circuit is shown in Figure 33 with a reference voltage given in Equation 50. The summary of the design parameters are given in Table XX.

$$\begin{aligned} V_{REF} &= \left(I_{CTAT} + I_{PTAT}\right)\left(R_7 + R_8\right) \\ &= \left(\frac{V_{GS\_MV4} + V_{R4} + V_{RS}}{R_2 + R_3} + \frac{V_{GS\_MN6} + V_{R6}}{r_{o7} + 1/G_{m7}}\right)\left(R_7 + R_8\right) \end{aligned} \quad (50)$$

Voltage reference circuit consists of a core reference, a PTAT generator and a start-up circuit, and summing circuit that sums PTAT and CTAT currents. High-resistivity polysilicon resistors (rpolyh), the low-temperature coefficient polysilicon resistors (rpolyz) and CMOS subthreshold devices have a non-linear temperature responses, which is used to create PTAT and CTAT currents. With the proper summation of these currents at the last block of the circuit a reference voltage is obtained. The prominent feature of this reference is that even though all of the transistors operate in subthreshold region, it performs with a nice temperature coefficient in a wide temperature range and little power [4].

TABLE XX
SUMMARY OF DESIGN PARAMETERS

Parameters	Andreou'13 [4]
Technology	0.35μm
Supply Voltage (V)	0.75
Reference Voltage (mV)	259
Temperature Range (°C)	-45 a 145
TC (ppm/°C)	2
Power (μW)	2

Campana'15 [7]: Campana et al. [7] present a 0.5V supply resistorless voltage reference using a Schottky diode for low-voltage applications. A standard 130nm CMOS process is used. 216mV reference voltage is provided by the reference, and it has a temperature coefficient of 192ppm/°C between -40°C and 120°C. Circuit is shown in Figure 34 with a reference voltage given in Equation 51. The summary of the design parameters are given in Table XXI.

$$V_{REF} = \phi_t \ln\left[\left(1 + 2\frac{S_7}{S_6}\right)\left(1 + 3\frac{S_5}{S_4}\right)\left(1 + 4\frac{S_3}{S_2}\right)\right] + V_D/2 \quad (51)$$

where the first term represents the PTAT behavior and the second term represents the CTAT behavior.

Supply voltages go down day by day, and now it is below 1V, particularly 0.5V for this circuit, with the advance of LVLP (low-voltage and low-power) applications. The authors choose to decrease high supply voltage need for BJTs by using a CMOS compatible Schottky diode instead of a BJT, since its forward bias voltage is around 150–450mV. CTAT part is obtained from the Schottky and added to PTAT part of the circuit which is found by a self-cascode structure. However, the authors state that it does not exhibit a good PSRR and line sensitivity, and needs to be improved. Also, they indicate that with trimming and diode curvature compensation its performance can be boosted [7].

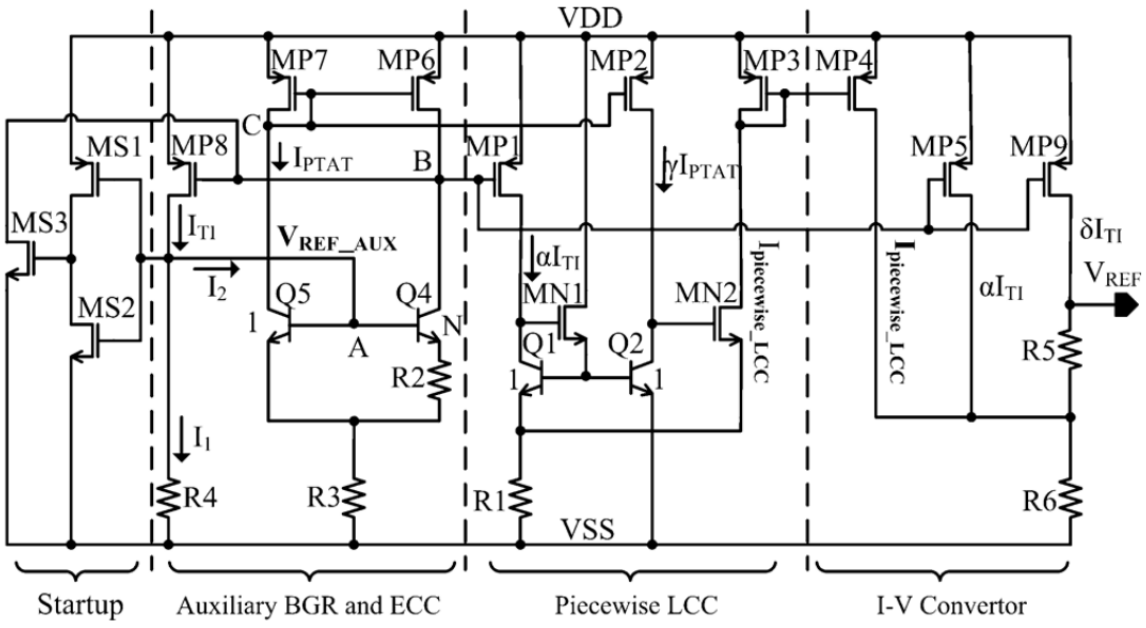

Fig. 32. Zhang'12 [29]

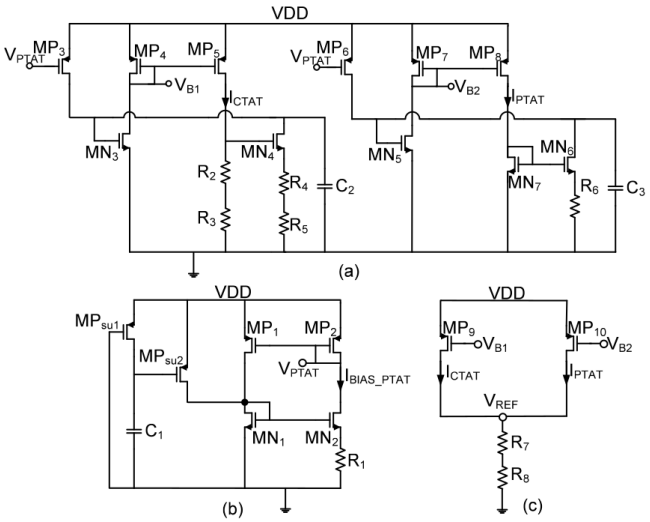

Fig. 33. Andreou'13 [4]

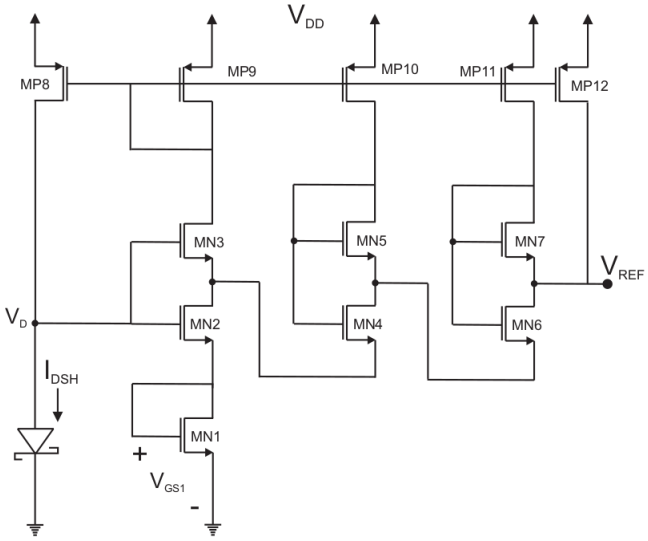

Fig. 34. Campana'15 [7]

TABLE XXI
SUMMARY OF DESIGN PARAMETERS

Parameters	**Campana'15 [7]**
Technology	130nm
Reference Type	Schottky
Supply Voltage (V)	0.5 (or 1.2)
Reference Voltage (mV)	216 (or 239)
Temperature Range (°C)	-40 a 120
TC (ppm/°C)	192 (or 43)
LNR@27°C (mV/V)	3.28
PSRR@1kHz (dB)	27 (or 32)
Power (nW)	113 (or 330)
Chip Area (mm^2)	0.0016

Tan'15 [22]: Tan et al. [22] present a sub1V, low-power MOS threshold monitoring based voltage reference. 65nm CMOS technology is used. 474mV reference voltage is provided by the reference, and it has a mean temperature coefficient of 40ppm/°C between -40°C and 90°C. Power dissipated by the voltage reference is 290nW. Voltage reference is shown in Figure 35 with a reference voltage given in Equation 52. The summary of the design parameters are given in Table XXII.

$$\begin{aligned} V_{\mathrm{REF}} =& V_R + V_{\mathrm{GS1}}(T) = 2I_1R_2(T) + I_2R_2(T) + V_{\mathrm{GS1}}(T) \\ =& 2\eta\frac{k_BT}{q}\frac{R_2(T)}{R_1(T)}\ln\left(\frac{S_2}{S_1}\right) + N\eta\frac{k_BT}{q}\frac{R_2(T)}{R_5(T)}\ln\left(\frac{S_4}{S_3}\right) \\ &+ V_{\mathrm{GS1}}(T) \end{aligned} \tag{52}$$

The authors state that this voltage reference is designed for the need of low-voltage, low-power and small temperature coefficient. It senses threshold voltage in the core of the voltage reference, which is in a Brokaw circuit. There are also a second-order temperature compensation current generator, and an operational amplifier, as well as a start-up circuit. After sensing this threshold voltage, its nonlinear temperature effects shows a CTAT behaviour. A PTAT current is generated on a high resistive poly resistor. Those currents are transmitted to two-stage operational amplifier with current mirrors and summed to create a zero TC at the output [22].

TABLE XXII
SUMMARY OF DESIGN PARAMETERS

Parameters	Tan'15 [22]
Technology	65nm
Supply Voltage (V)	0.75-1.2
Reference Voltage (mV)	474
Temperature Range (°C)	-40 a 90
TC (ppm/°C)	24-50.4
Line Sensitivity (ppm/V)	2423
PSRR@100Hz (dB)	-40
Power (nW)	290
Chip Area (mm^2)	0.0198

Yang'11 [25]: Yang et al. [25] present a low-voltage subthreshold bandgap voltage reference. 0.5μm CMOS process is used. 337mV reference voltage is provided by the reference by a supply of 1V, and power consumption of the reference is 32.8μW by occupying 0.3234mm^2. Operating temperature range is between 10°C and 100°C. Circuit is shown in Figure 36 with a reference voltage given in Equation 53. The summary of the design parameters are given in Table XXIII.

$$V_{out} = R_4I_3 = \frac{R_4}{R_3}\left(nV_T\ln(N) + \frac{R_3}{R_2}V_{GS}\right) \tag{53}$$

Opamp based β-multiplier circuit is used for its core. Weak inversion MOS transistors are used instead of BJTs, and a bulk-driven amplifier is added to reduce the power consumption. To decrease the mismatches of the transistors in bulk-driven amplifier, large gate areas are chosen, which leads to large parasitic capacitances. However, this does not bring a problem as it does not need a high GBWP. Furthermore, pin-selectable trimmed resistive network is implanted for resistor R_3 to cancel out the temperature coefficients of resistors. For this circuit, low-voltage operation and low power dissipation is key features, since it is a high demand for battery-operated devices [25].

TABLE XXIII
SUMMARY OF DESIGN PARAMETERS

Parameters	Yang'11 [25]
Technology	0.5μm
Supply Voltage (V)	1
Reference Voltage (mV)	337
Temperature Range (°C)	10 a 100
TC (ppm/°C)	9.9
Power (μW)	32.8
Chip Area (mm^2)	0.3234

Yang'14 [26]: Yang et al. [26] present a ultra low-voltage subthreshold bandgap voltage reference. 110nm CMOS process is used. 195.6mV reference voltage is provided by the reference by a supply of 250mV, and power consumption of the reference is 5.35μW by occupying 0.013mm^2. Operating temperature range is between 10°C and 90°C. Circuit is shown in Figure 37 with a reference voltage given in Equation 54. The summary of the design parameters are given in Table XXIV.

Since for subthreshold region, temperature coefficient of gate–source voltage of an NMOS is negative and it can be assumed that it is a function of temperature, we can obtain as follows:

$$V_{\mathrm{REF}} = \frac{R_4}{R_3}\left(nV_T\ln(N) + \frac{R_3}{R_1}V_{GS1}\right) \tag{54}$$

Note that obtaining such a low-voltage is impossible with the use of a BJT, since it is needed a voltage of 0.7V for forward biased junction of the BJT. Thus, it is obvious that voltage reference circuit is BJT-free. What is really interesting with this voltage reference is that it does not use an amplifier rather it uses a comparator with a charge-pump circuit and a digital control circuit. So, its sub-blocks can be listed as subthreshold CMOS voltage reference core, low-voltage comparator with auxiliary amplifier, charge-pump circuit, and control unit circuit. Its working principle can be summarized as 1) comparator detects voltage differences between its inputs, 2) charge-pump circuit changes gate voltage accordingly, i.e. increase or decrease, 3) currents are controlled along with this gate voltage, 4) control unit circuits controls comparator circuit and charge-pump circuit. It can also be said that its prominent feature is low power dissipation with low-voltage operation [26].

TABLE XXIV
SUMMARY OF DESIGN PARAMETERS

Parameters	Yang'14 [26]
Technology	110nm
Supply Voltage (mV)	250
Reference Voltage (mV)	195.6±14
Temperature Range (°C)	10 a 90
TC (ppm/°C)	134
Line Sensitivity (mV/100mV)	0.8
Power (μW)	5.35
Chip Area (mm^2)	0.013

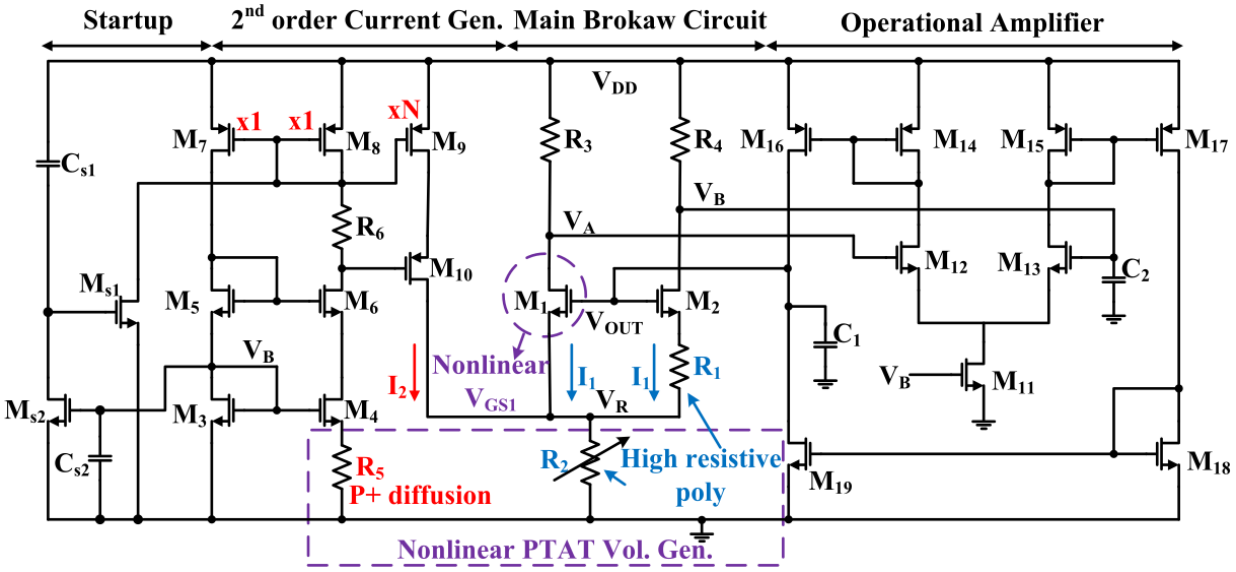

Fig. 35. Tan'15 [22]

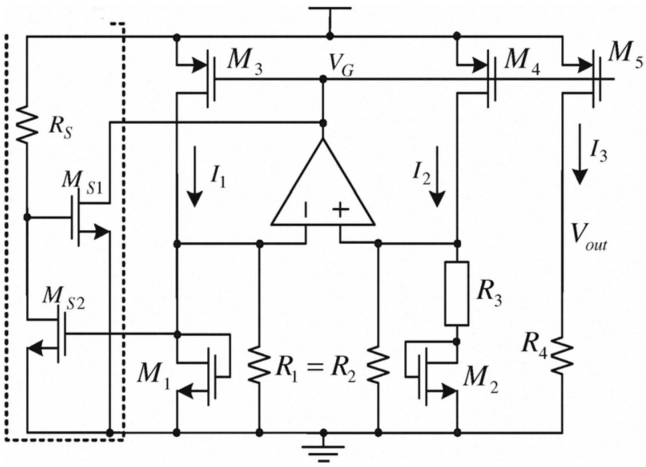

Fig. 36. Yang'11 [25]

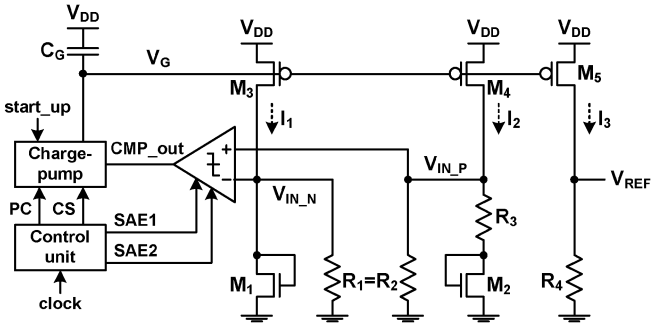

Fig. 37. Yang'14 [26]

F. Low Temperature Coefficient

Martinez-Nieto'13 [16]: Martinez-Nieto et al. [16] present a low-temperature coefficient CMOS BGR, which achieves a high-order curvature correction by biasing BJT with PTAT^2 current. Standard 0.18μm-1.8V CMOS process is used. 1.225V reference voltage is provided by the BGR, and it has a temperature coefficient of 1.6ppm/°C between -20°C and 140°C under process variations, and a line regulation of 3.3(mV/V) at 27°C, shown in Figure 38 with a reference voltage given in Equation 55. The summary of the design parameters are given in Table XXV [16].

It basically includes a bandgap core, a start-up circuit and a current generator for I_{PTAT^2}. Core is a opamp based β-multiplier bandgap voltage reference circuit described in Section III-A, here is where I_{PTAT} is generated. Current generator for I_{PTAT^2} is important, since it helps to get a high-order curvature correction. Reference voltage is obtained as in Equation 55.

$$V_{REF} = V_{BE4} + \frac{R_3}{R_1} V_T \ln r = V_{BE4} + \frac{R_3}{R_1}\left(\frac{kT}{q}\ln r\right) \quad (55)$$

TABLE XXV
SUMMARY OF DESIGN PARAMETERS

Parameters	Martinez-Nieto'13 [16]
Technology	0.18μm
Supply Voltage (V)	1.8
Reference Voltage (V)	1.225
Temperature Range (°C)	-20 a 140
TC (ppm/°C)	1.6
LNR@27°C (mV/V)	3.3
PSRR@1kHz (dB)	-60
Power (μW)	620
Chip Area (mm^2)	0.0308

Mattia'14 [17]: Mattia et al. [17] present a 40nW MOSFET-only voltage reference. 0.13μm CMOS process is used. 625mV reference voltage is provided by the voltage reference, and it has a temperature coefficient of 2.3ppm/°C between -40°C and 125°C, shown in Figure 39 with a refer-

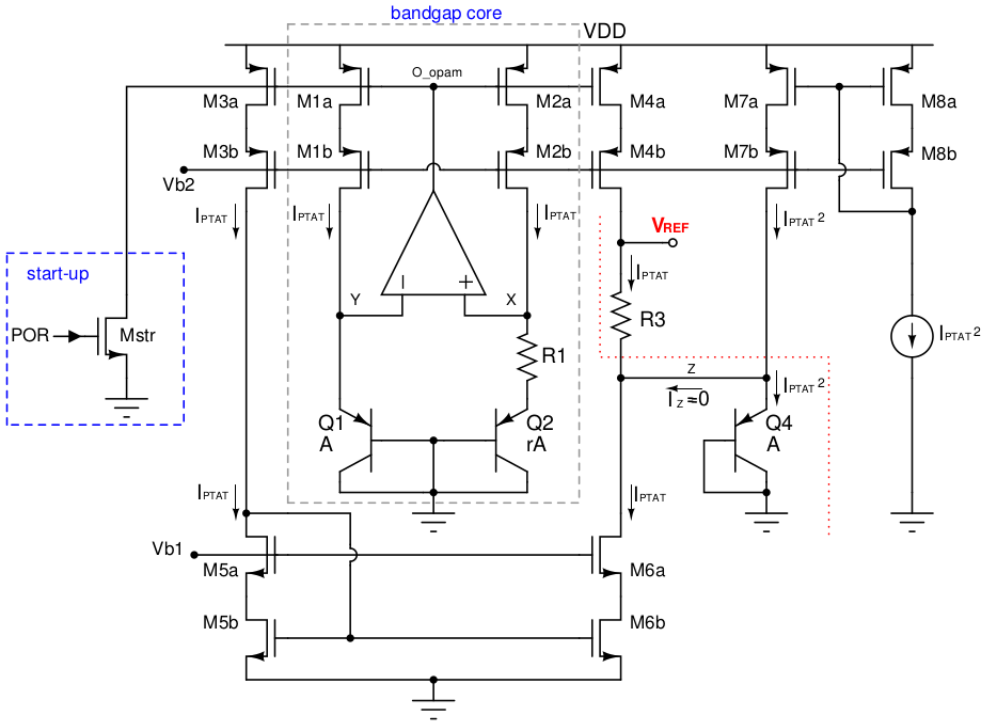

Fig. 38. Martinez-Nieto'13 [16]

ence voltage given in Equation 56. The summary of the design parameters are given in Table XXVI.

$$V_{REF} = V_{G1} + 2V_{DIFF} = V_{T0} + 2n\phi_t \left[F\left(i_{f9}\right) - F\left(i_{if8}\right)\right] \tag{56}$$

For a low-voltage, low-power application, MOSFET-only voltage references are almost indispensable. MOSFET threshold voltage can be a proposal to a CTAT voltage. Thus, in this paper a MOSFET threshold voltage extractor circuit is used for providing CTAT voltage. On the other hand, PTAT voltage is extracted from an unbalanced PMOS differential pair with weak inversion so that power dissipation stays low. Adding CTAT and PTAT terms accordingly, a zero TC is obtained over a wide range of temperature [17].

TABLE XXVI
SUMMARY OF DESIGN PARAMETERS

Parameters	Mattia'14 [17]
Technology	0.13μm
Supply Voltage (V)	0.9-1.2
Reference Voltage (mV)	625
Temperature Range (°C)	-40 a 125
TC (ppm/°C)	2.3
Line Sensitivity (ppm/V)	35200
PSRR@100Hz (dB)	-30
Power (nW)	39.6
Chip Area (mm^2)	0.0099

G. Harsh Environments

Boufouss'13 [6]: Boufouss et al. [6] present a high temperature and high radiation CMOS subthreshold voltage reference. A 0.13μm CMOS SOI process is used as usually for harsh environment applications. 1.5V reference voltage is provided by the reference, and it has a temperature coefficient of 133ppm/°C between -40°C and 90°C and of 470ppm/°C between -40°C and 200°C. Circuit is shown in Figure 40 with a reference voltage given in Equation 57. The summary of the design parameters are given in Table XXVII.

$$V_{REF} = n.V_T \cdot \left[\ln\left(\frac{\beta_{Mp}}{\beta_{Mn}}\right) + m_r.\ln\left(\frac{n.m.\ln(k)}{R_B \cdot \beta_{Mn} \cdot V_T}\right)\right] + (1+m_r)\,V_{thn} - |V_{thp}| \tag{57}$$

The author's aim is to implement a voltage reference working under high temperatures and radiation exposures. Besides, it is chosen an operation of subthreshold for CMOS devices so that low-power dissipation is obtained even in very high temperatures. This voltage reference is suitable for space and nuclear applications. For higher stability, they employed a cascode structure, a start-up circuit is introduced so that even in extreme temperatures and process corners it would not be a problem. Process corner analysis is done so that it can operate at extreme temperatures like 200°C properly. Radiation measurements are done by γ-rays with a Cobalt source (^{60}Co). Voltage reference is observed for one week with a steady dose of radiation, which resulted in at most a 75mV change in the 1.5V reference [6].

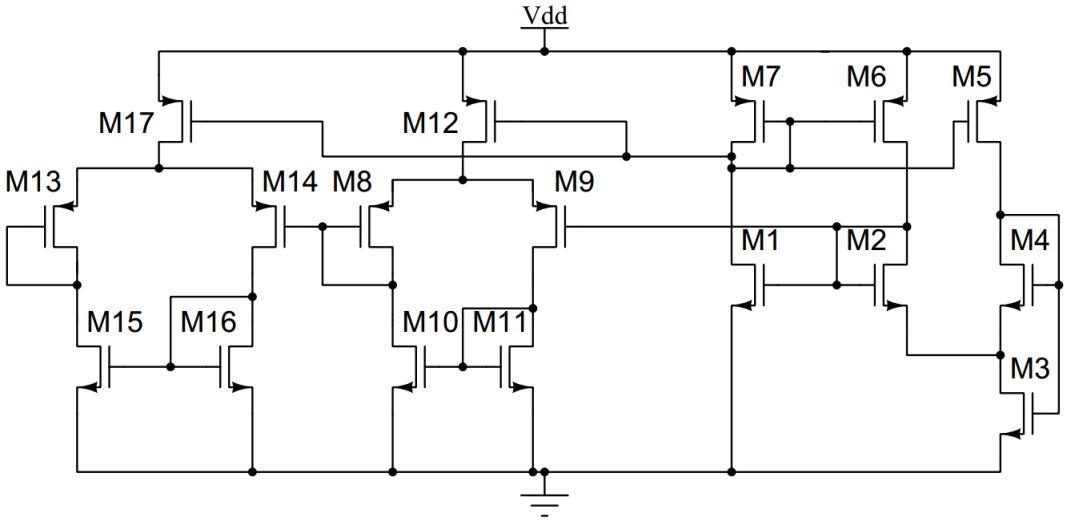

Fig. 39. Mattia'14 [17]

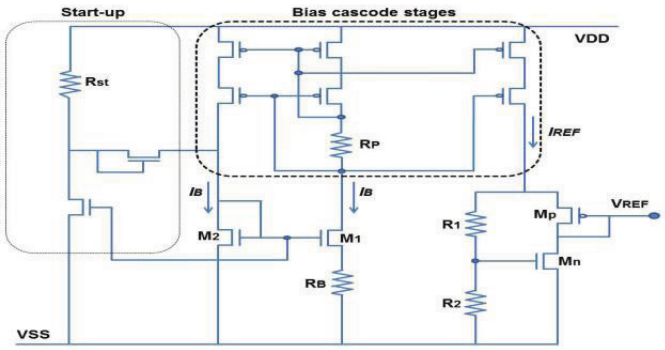

Fig. 40. Boufouss'13 [6]

TABLE XXVII
SUMMARY OF DESIGN PARAMETERS

Parameters	Boufouss'13 [6]
Technology	0.13μm CMOS SOI
Supply Voltage (V)	2.5
Reference Voltage (V)	1.5
Temperature Range (°C)	-40 a 200
TC (ppm/°C)	133
Power (μW)	75
Irradiation Particles	γ
Reference Shift@1.5Mrad (ppm/krad)	25
Chip Area (mm^2)	0.09

Piccin'14 [20]: Piccin et al. [20] present a radiation-hardening technique for a CMOS voltage reference. A standard 130nm CMOS technology is used. 781mV reference voltage is provided by the reference, and it has a temperature coefficient of 471ppm/°C. Circuit is shown in Figure 41 with a reference voltage given in Equation 58. The summary of the design parameters are given in Table XXVIII.

$$\begin{aligned} V_{REF} &= R_2 \left(I_{CTAT} + G I_{PTAT}\right) \\ V_{REF} &= \frac{R_2}{R_1}\left(V_{T1} - V_{T2}\right) + G\frac{R_2}{R_3}\ln(8) n V_t \end{aligned} \tag{58}$$

Current mode voltage reference is used as it can be understood from Equation 58, as its combinations are easier to create. There are 5 sub-circuits for this voltage reference. It can be listed as 1) threshold voltage difference-referenced current generator 2) OTA 3) PTAT current generator 4)CTAT and PTAT current to voltage converter 5) two start-up circuits. The authors irradiated the circuit with two doses 310rad/h and 650rad/h with γ-rays using Cobalt (^{6}0Co), and its effects are observed. Same voltage reference with different layouts are tested, and the importance of layout in TID-hardening is emphasized [20].

TABLE XXVIII
SUMMARY OF DESIGN PARAMETERS

Parameters	Piccin'14 [20]
Technology	130nm
Supply Voltage (V)	2.5-3.6
Reference Voltage (mV)	781
TC (ppm/°C)	471
PSRR@DC (dB)	78
Irradiation Particles	γ
Reference Shift@310rad/h (%)	0.5
Chip Area (mm^2)	0.0370

H. Small Die Area

Chouhan'15 [10]: Chouhan et al. [10] present the design and implementation of a micro-power voltage reference. Standard 0.18μm CMOS technology is used. 536.01mV reference voltage is provided by the reference, and it has a temperature coefficient of 19.3ppm/°C between -40°C and 85°C. It only dissipates 0.48μW. Circuit is shown in Figure 42 with a reference voltage given in Equation 59. The summary of the design parameters are given in Table XXIX.

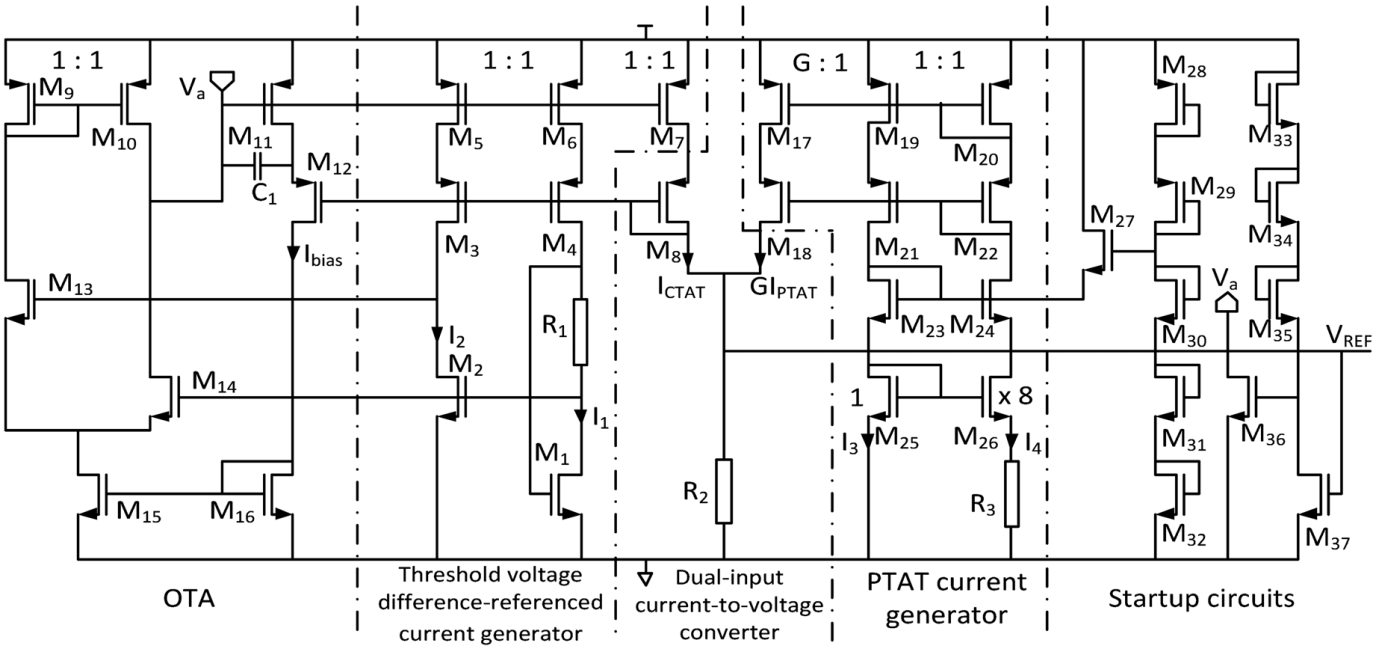

Fig. 41. Piccin'14 [20]

$$V_{ref} = \left[V_{thn}\left(T_0\right) - \kappa_n \cdot \left(T - T_0\right)\right]_a + \left[\chi_s \cdot \frac{S_5}{\sqrt{S_6}} \cdot \eta \cdot V_T \cdot \ln\left[\frac{S_4}{S_3}\right]\right]_b \quad (59)$$

A start-up circuit is adopted since it has two operation points, which is based on RC time constant, i.e. Ms1 is used a resistor. A resistorless CMOS β-multiplier with a cascode stage is used as described in III-D so that it eliminates the effect of channel length modulation and increase power supply rejection ratio. The temperature compensation is done at the last stage of the proposed voltage reference with composite NMOS transistors. It has a moderate TC and provides low-power with less area [10].

TABLE XXIX
SUMMARY OF DESIGN PARAMETERS

Parameters	Chouhan'15 [10]
Technology	0.18μm
Supply Voltage (V)	1.25-2
Reference Voltage (V)	536.01
Temperature Range (°C)	-40 a 85
TC (ppm/°C)	19.302
LNR@27°C (mV/V)	2.217
PSRR@10Hz (dB)	-55
Power (μW)	0.48
Chip Area (mm^2)	0.0077

Mattia'15 [18]: Mattia et al. [18] present a sub-1V 5nW resistorless sub-bandgap voltage reference. 0.13μm CMOS process is used. 570mV reference voltage is provided by sub-BGR, and it has a temperature coefficient of 11ppm/°C between 0°C and 125°C, shown in Figure 43 with a reference

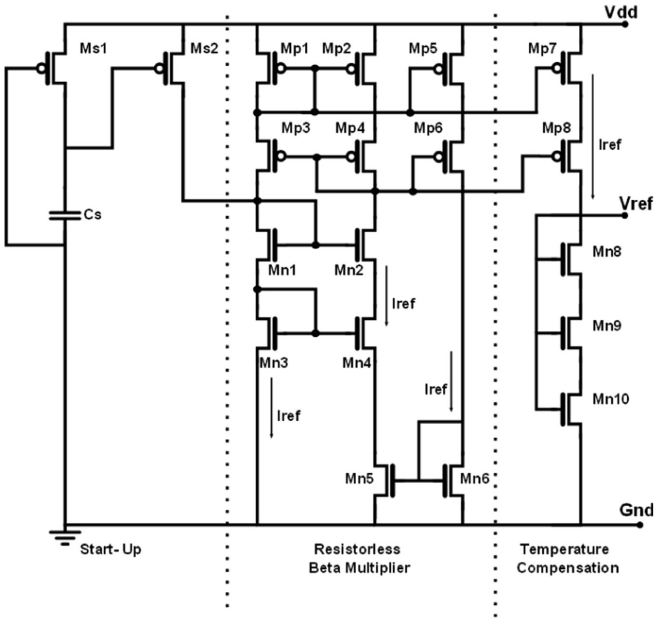

Fig. 42. Chouhan'15 [10]

voltage given in Equation 60. The summary of the design parameters are given in Table XXX.

$$V_{REF} \approx \frac{V_{BE}}{n+1} + V_{PTAT} \quad (60)$$

BJT emitter current is achieved by counterbalancing BJT junction voltage and MOSFETs gate-source voltage with a self-cascode. PTAT voltage is created by this self-cascode structure. While reference voltage is addition of gate voltage of M1 and PTAT voltage, and by noting that gate voltage

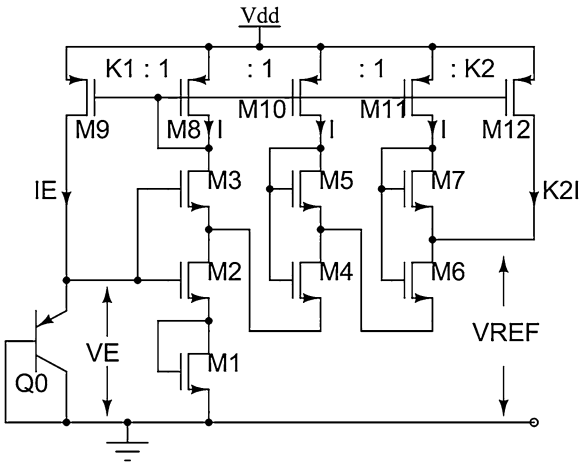

Fig. 43. Mattia'15 [18]

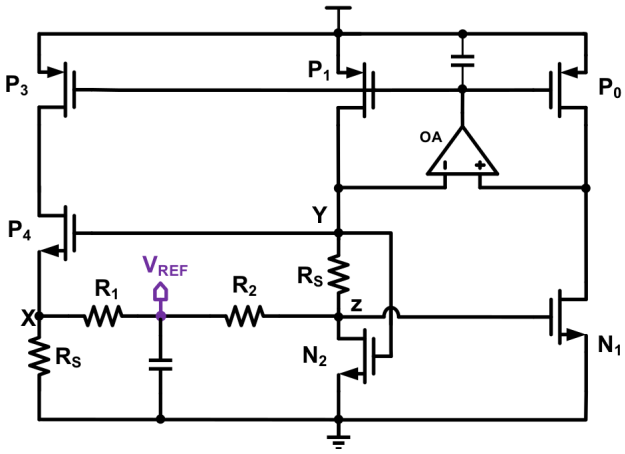

Fig. 44. Nagulapalli'17 [19]

of M1 is a sum portion is a base-emitter junction of BJT, Equation 60 can be obtained. Its main features are its low temperature coefficient and its small silicon area with only 5nW consumption [18].

TABLE XXX
SUMMARY OF DESIGN PARAMETERS

Parameters	Mattia'15 [18]
Technology	0.13μm
Supply Voltage (V)	0.9
Reference Voltage (mV)	570
Temperature Range (°C)	0 a 125
TC (ppm/°C)	11
LNR@27°C (mV/V)	0.9
PSRR@100Hz (dB)	-41
Power (nW)	5
Chip Area (mm^2)	0.0022

Nagulapalli'17 [19]: Nagulapalli et al. [19] present a low-voltage, microwatt power bandgap voltage reference for biomedical applications. 45nm CMOS process is used. 475mV reference voltage is provided by the BGR, and it has a temperature coefficient of 31ppm/°C between -40°C and 125°C, which is a relatively high temperature coeefficient. However, it consumes 16μW power with 0.8V supply voltage, and it only occupies an area of 0.004875mm^2. Circuit is shown in Figure 44 with a reference voltage given in Equation 61. The summary of the design parameters are given in Table XXXI.

$$\begin{aligned} V_{\text{ref}} &= \frac{V_x R_2 + V_y R_1}{R_1 + R_2} \\ &= \frac{1}{1+\beta}\left(V_{th} + \frac{\alpha}{u_n C_{ox}\frac{W}{L}}\right) \end{aligned} \tag{61}$$

where

$$\alpha = \frac{1}{R_S}\left(1 - \frac{1}{\sqrt{K}}\right)\left(\frac{1}{2} + \beta\left(1 - \frac{1}{\sqrt{K}}\right)\right)$$

In the paper, the presented circuit is a BJT-free circuit. It creates CTAT and PTAT currents using MOS transistors. A BJT-free CMOS β-multiplier is used as in described Section III-B. Opamp used in BGR is a two-stage differential amplifier. The prominent feature of this reference is low-power and less-area for biomedical application [19].

TABLE XXXI
SUMMARY OF DESIGN PARAMETERS

Parameters	Nagulapalli'17 [19]
Technology	45nm
Supply Voltage (V)	0.8
Reference Voltage (mV)	475
Temperature Range (°C)	-40 a 125
TC (ppm/°C)	31
Line Sensitivity (ppm/V)	26.5
PSRR@1MHz (dB)	-70
Power (μW)	16
Chip Area (mm^2)	0.004875

V. PERFORMANCE COMPARISON OF VOLTAGE REFERENCES

Voltage references discussed in Section IV are seperated categories as in IV-A, IV-B, IV-C, IV-D, IV-E, IV-F, IV-G, and IV-H, namely ultra-low power (ULP), ultra-low voltage (ULV), high PSRR (PSRR), high precision (LNR), low-voltage and low-power (LVLP), low temperature coefficient (LTC), harsh environments (HE), and small die area (DA) respectively and compared in their category in Tables XXXII, XXXIII, XXXIV, XXXV, XXXVI, XXXVII, XXXVIII, and XXXIX.

VI. CONCLUSION

This paper presents a comprehensive survey and comparative analysis of 30 state-of-the-art voltage reference circuits [2]–[31] published during the 2010s. The surveyed designs are systematically categorized into eight distinct groups based on their primary design objectives: ultra-low power (7 circuits), ultra-low voltage (2 circuits), high PSRR (6 circuits), high precision (3 circuits), low-voltage low-power (5 circuits), low temperature coefficient (2 circuits), harsh environment operation (2 circuits), and small die area (3 circuits).

The analysis reveals several key trends and insights in voltage reference design. Ultra-low power implementations have achieved remarkable power reductions down to picowatt levels, with some designs operating at less than 0.1 nW. Sub-1V operation has become increasingly important for modern scaled CMOS technologies, though it often comes at the cost of reduced precision and increased sensitivity to process variations. High PSRR designs demonstrate the critical importance of supply noise rejection in mixed-signal environments, with some circuits achieving better than -100 dB rejection.

The comparative analysis highlights the fundamental trade-offs inherent in voltage reference design. Achieving multiple performance objectives simultaneously remains challenging, as improvements in one metric often degrade others. For instance, ultra-low power operation typically increases temperature sensitivity, while high precision designs tend to consume more power and area.

This comprehensive review serves multiple purposes: it provides researchers with insights into current design trends and identifies promising directions for future work, offers practicing engineers a detailed comparison framework for selecting appropriate voltage reference architectures, and establishes a baseline for evaluating new designs against the current state-of-the-art. The systematic categorization and detailed performance comparisons presented here constitute one of the most extensive surveys of voltage reference circuits available in the literature, making it a valuable resource for the analog IC design community.

TABLE XXXII
SUMMARY OF DESIGN PARAMETERS FOR ULP

Parameters	**Cao'18 [8]**	**Chatterjee'17 [9]**	**De Oliveira'17 [11]**	**Duan'17 [12]**	**Liu'17 [15]**	**Seok'12 [21]**	**Zeng'13 [27]**
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm
Supply Voltage (V)	0.8	0.8	0.45	0.8	1.1	0.5	0.65
Reference Voltage (mV)	621	350.8	225.3	328	755	175	202.7
Temperature Range (°C)	-45 a 120	0 a 75	0 a 120	10 a 100	-15 a 140	-20 a 80	-20 a 80
TC (ppm/°C)	13	76	104	33.8	34	16.9	2.1
LNR (%/V)	0.107	0.3	0.15	0.21	0.28	0.036	0.00054
PSRR (dB)	-49@100Hz	-65@100Hz	-43.9@100Hz	-55@100Hz	-47@1MHz	-51@100Hz	-49@100Hz
Power (nW)	4	120	0.0543	79	4.6	0.0295	1.2
Chip Area (mm^2)	0.0308	0.023	0.002	0.014	0.0598	0.0093	0.011

TABLE XXXIII
SUMMARY OF DESIGN PARAMETERS FOR ULV

Parameters	**Wang'15 [23]**	**Zhu'16 [31]**
Technology	0.18μm	0.18μm
Supply Voltage (V)	0.45	0.45
Reference Voltage (mV)	118.46	118.45
Temperature Range (°C)	-40 a 125	-40 a 85
TC (ppm/°C)	63.6	59.4
LNR (%/V)	0.12	0.033
PSRR (dB)	-44.2@100Hz	-50.3@100Hz
Power (nW)	14.6	15.61
Chip Area (mm^2)	0.012	0.0132

TABLE XXXIV
SUMMARY OF DESIGN PARAMETERS FOR PSRR

Parameters	**Alhassan'16 [2]**	**Alhassan'16 [3]**	**Basyurt'14 [5]**	**Jing'12 [13]**	**Yusoff'12 [28]**	**Zhu'14 [30]**
Technology	0.18μm	0.18μm	0.35μm	0.13μm	0.18μm	0.18μm
Supply Voltage (V)	0.8	1.1	2	0.5	1.8	3.3
Reference Voltage (mV)	489	893	201	85.5	1204	1176
Temperature Range (°C)	-30 a 110	-30 a 80	-40 a 125	0 a 100	-20 a 90	-40 a 125
TC (ppm/°C)	6.5	19	6.2	52.5	6.1	11.6
LNR (%/V)	0.076	0.093	0.069	0.104	0.4	NA
PSRR@100Hz (dB)	-75	-75	-76.5	-70.4	NA	-115
PSRR@1kHz (dB)	NA	NA	NA	NA	-84	NA
PSRR@100kHz (dB)	-61	-58	NA	-98	NA	NA
PSRR@1MHz (dB)	NA	NA	NA	NA	NA	-90
PSRR@10MHz (dB)	-59	-60	NA	-112	NA	NA
PSRR@60MHz (dB)	-51	-50	NA	NA	NA	NA
Power (μW)	0.36	0.55	103.95	0.0015	150	277.2
Chip Area (mm^2)	0.0143	0.0180	0.165	NA	0.111	0.0014

TABLE XXXV
SUMMARY OF DESIGN PARAMETERS FOR LNR

Parameters	**Li'18 [14]**	**Xie'14 [24]**	**Zhang'12 [29]**
Technology	0.18μm	0.18μm	0.5μm BiCMOS
Supply Voltage (V)	1.7-3.5	1.2-2.5	3.6
Reference Voltage (mV)	902	193.95	1285
Temperature Range (°C)	-50 a 120	-40 a 85	-40 a 110
TC (ppm/°C)	3.6-7.4	9.77-36.66	5
LNR@27°C (mV/V)	0.005	0.036	0.059
PSRR (dB)	-80@1kHz	-49.6@100Hz	-70@1kHz
Power (μW)	115	0.975	125
Chip Area (mm^2)	0.003	0.0219	0.04

TABLE XXXVI
SUMMARY OF DESIGN PARAMETERS FOR LVLP

Parameters	**Andreou'13 [4]**	**Campana'15 [7]**	**Tan'15 [22]**	**Yang'11 [25]**	**Yang'14 [26]**
Technology	350nm	130nm	65nm	500nm	110nm
Supply Voltage (V)	0.75	0.5	0.75	1	0.25
Reference Voltage (mV)	259	216	474	337	195.6
Temperature Range (°C)	-45 a 145	-40 a 120	-40 a 90	10 a 100	10 a 90
TC (ppm/°C)	2	192	24	9.9	134
LNR@27°C (mV/V)	NA	3.28	2.42	NA	0.08
PSRR (dB)	NA	27@1kHz	-40@100Hz	NA	NA
Power (μW)	2	0.113	0.29	32.8	5.35
Chip Area (mm^2)	NA	0.0016	0.0198	0.3234	0.013

TABLE XXXVII
SUMMARY OF DESIGN PARAMETERS FOR LTC

Parameters	**Martinez-Nieto'13 [16]**	**Mattia'14 [17]**
Technology	0.18μm	0.13μm
Supply Voltage (V)	1.8	0.9
Reference Voltage (V)	1.225	0.625
Temperature Range (°C)	-20 a 140	-40 a 125
TC (ppm/°C)	1.6	2.3
LNR@27°C (mV/V)	3.3	35.2
PSRR (dB)	-60@1kHz	-30@100Hz
Power (μW)	620	0.0396
Chip Area (mm^2)	0.0308	0.0099

TABLE XXXVIII
SUMMARY OF DESIGN PARAMETERS FOR HE

Parameters	**Boufouss'13 [6]**	**Piccin'14 [20]**
Technology	0.13μm CMOS SOI	0.13μm
Supply Voltage (V)	2.5	2.5
Reference Voltage (V)	1.5	0.781
Temperature Range (°C)	-40 a 200	NA
TC (ppm/°C)	133	471
Power (μW)	75	NA
Irradiation Particles	γ	γ
Reference Shift	25ppm/krad@1.5Mrad	0.5%@310rad/h
Chip Area (mm^2)	0.09	0.0370

TABLE XXXIX
SUMMARY OF DESIGN PARAMETERS FOR DA

Parameters	**Chouhan'15 [10]**	**Mattia'15 [18]**	**Nagulapalli'17 [19]**
Technology	0.18μm	0.13μm	45nm
Supply Voltage (V)	1.25	0.9	0.8
Reference Voltage (V)	536.01	570	475
Temperature Range (°C)	-40 a 85	0 a 125	-40 a 125
TC (ppm/°C)	19.302	11	31
LNR@27°C (mV/V)	2.217	0.9	0.0265
PSRR (dB)	-55@10Hz	-41@100Hz	-70@1MHz
Power (μW)	0.48	0.005	16
Chip Area (mm^2)	0.0077	0.0022	0.004875

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