Semiconductor Switching Interpretability Theory: Establishing Interpretability for Semiconductor Switching Behaviors by Bridging Circuit Theory, Conservation Laws and Semiconductor Physics

Abstract

Global electricity demand is expected to more than double by 2050[1-8], driven by emerging loads including AI data centers,[3,4] electrified transport[5,6], heat pumps[7], electrolytic hydrogen production[8] and robotics[2]. The global sustainability urgently demands green electrical and electronic engineering (EEE), where semiconductors are core components. However, semiconductor switching behaviors have been treated as a "black box" lacking interpretability since 1947[9], placing fundamental limits on semiconductor sciences, engineering and downstream applications. Here we present the Semiconductor Switching Interpretability Theory (SSIT), which provides interpretability for semiconductor switching behaviors and interactions between semiconductors and other circuit elements, by bridging circuit theory[10], conservation laws and semiconductor physics. SSIT carries profound implications, including establishing a new fundamental groundwork and a wealth of foundations and directions for future investigation. As examples, SSIT yields a switching-energy-loss prediction model (errors: 0.88–11.60%), achieving a 17-fold average error reduction compared to the existing model (errors: 34.41–80.05%); it enables unprecedented causal-mechanism interpretations for switching waveforms and interactions between the semiconductor and other circuit elements across scenarios. It informs semiconductor engineering and downstream applications individually, and further enables future-generation co-design between them—currently treated separately—for optimal system performance such as maximized energy and emission savings and reliability. It also opens directions across disciplines including semiconductor materials,[11,12] device structure engineering,[13,14] packaging,[15,16] reliability,[17,18] thermal management;[19,20] and downstream applications such as power electronics (an EEE's sub-field handling electric power using semiconductors), and potentially across EEE sub-fields, including higher-frequency communication and computation devices and integrated circuits.[21,22]

Keyword: interpretability, semiconductor switching behaviors, transistor switching phenomena, semiconductor switching interpretability theory, SSIT, semiconductor-circuit interaction, switching loss prediction, semiconductor-application co-design

Nomenclature

Table 1. NOMENCLATURE

Symbol	Unit	Definition
S_x	N/A	Switch number, e.g., S_1 denotes the upper switch and S_2 denotes the lower switch.
R_{Sx}	Ω	Equivalent resistance of S_x.
$R_{drift,Sx}$	Ω	Drift-region resistance of S_x.
$R_{ch,Sx}$	Ω	Channel resistance of S_x.
$v_{ds,Sx}$	V	Drain-source voltage of S_x.
v_{GG}	V	Output voltage of the gate driver of S_1.
$v_{gs,Sx}$	V	Gate-source voltage of S_x.
$V_{th,Sx}$	V	Threshold voltage of S_x.
$C_{oss,Sx}$	pF	Output capacitance of S_x.
C_{Sx}	pF	Overall equivalent capacitance of S_x.
$C_{gs,Sx}$	pF	Gate-source capacitance of S_x.
$C_{gd,Sx}$	pF	Gate-drain capacitance (also known as Miller capacitance) of S_x.
$C_{ds,Sx}$	pF	Drain-source capacitance of S_x.
$i_{d,Sx}$	A	The drain current of S_x.
$i_{d,Sx}$	A	The channel current of S_x.
$i_{g,Sx}$	A	Gate driving current of S_x.
i_L	A	Load current.
i_{RSx}	A	Instantaneous current through R_{Sx}.
i_{DC}	A	DC-source current.
$i_{Cgs,Sx}$	A	Displacement current of $C_{gs,Sx}$.
$i_{Cgd,Sx}$	A	Displacement current of $C_{gd,Sx}$.
$i_{Cds,Sx}$	A	Displacement current of $C_{ds,Sx}$.
$i_{C,Sx}$	A	Displacement current of C_{Sx}.
$i_{rr,Sx}$	A	Current through the equivalent capacitance $C_{rr,Sx}$.
V_{DC}	V	DC-link voltage.
E_{on}	μJ	The turn-on energy dissipation.
$E_{gd,Sx}(v)$	μJ	The energy stored in $C_{gd,Sx}$ at drain-gate voltage of v.
$E_{ds,Sx}(v)$	μJ	The energy stored in $C_{ds,Sx}$ at drain-source voltage of v.
$E_{oss,Sx}(v)$	μJ	The energy stored in the output capacitance of S_x at drain-source voltage of v.
$Q_{oss,Sx}(v)$	nC	The charge stored in the output capacitance of S_x at drain-source voltage of v.
e_{pro}	N/A	Error of the proposed model's prediction results w.r.t. the measured results.
e_{con}	N/A	Error of the conventional model's prediction results w.r.t. the measured results.

Introduction

According to International Energy Agency and World Bank, global electrification[5-7], digitalization[3,4], and intelligentization,[2,4] including AI data centers,[3,4] electrification

including electrified transport[5,6], heat pumps[7] and electricity-enabled hydrogen production[8] and robotics[2], have placed unprecedented electricity demands. Consequently, global electricity demands are projected to more than double by 2050.[1-8] Global sustainability urgently demands green solutions in EEE, where semiconductors are core components. For example, over 80% of USA electricity is projected to be processed by power electronics (an EEE's sub-field handling electric power using semiconductors) by 2030,[23] where the switching-energy loss normally dominates overall system loss, and is further exacerbated by the constant push towards higher switching frequency, e.g., MHz-level and above for compactness.[19,24,25]

However, the interpretability of semiconductor switching behaviors has remained lacking,[26-29] despite their central role in EEE. In terms of the lumped-element-based equivalent-circuit modelling,[26,27,30] many works[26-29] model the device as a single two-terminal switch or three-terminal block; others[31-34] model the conductive path with added junction capacitances, distinguishing capacitive and conductive current components in the device; some works[35-38] further model the conductive path as either a current source or a voltage source by emulating its observed waveforms. Nonetheless, across all existing models, the interpretability is fundamentally obstructed as understanding is limited to descriptions for observed outputs, including measured or simulated switching waveforms or linearized approximations led by textbooks[26,27] and standards[39,40], as well as switching energy dissipation[39-42]. Consequently, causal-mechanism interpretations are hindered. For example, the energy dissipation associated with resistive components along the conductive current path remains obscured; the equivalent-circuit representations differ across switching scenarios and subintervals, lacking a unified model; the driving role of variable resistors has remained unrecognized, leaving the inputs decoupled from the output response.[26-29,34,38-40] This also obscures the criterion for the onset of switching, causing ambiguity for identifying the number and onset of turn-on events, potentially leading to mis-interpretation in situations including crosstalk-induced gate spikes[35,37], multiple threshold crossings and multi-level gate-driving[43] etc.

Moreover, some inputs that significantly influence output responses are unrecognized. For example, in modelling turn-on energy (E_{on}) under incomplete zero voltage switching (iZVS), Kasper et al.[42] accounts for the DC source and output capacitances of the upper (S_1) and lower (S_2) devices in a half bridge. The conventional E_{on} prediction model for a typical iZVS is thus derived from energy conservation.[42] However, the influence of load current, and associated energy dissipation during the current commutation (CC) subinterval remain unrecognized, leading to missing terms in modelling and thus systematic prediction inaccuracy. In addition, the two existing analytical frameworks—those based on energy conservation and charge conservation—remain fundamentally disconnected. Similarly, the unrecognized influence of S_2's non-linear junction capacitances obscures the causal-mechanism interpretations. For example, the Miller plateau (the subinterval of nearly constant v_{gs} in the switching transient) and its abrupt voltage drop at the end are well reported, but their causal mechanisms remain unclear,[26-29,34,38-40] despite their energy loss often constituting a significant portion of overall system energy losses.

In this work, we introduce SSIT, which addresses the abovementioned limitations and provide interpretability of semiconductor switching behaviors by bridging circuit theory[10], conservation laws of energy and charge and semiconductor physics (Fig. 1). As examples, based on SSIT, we derived a new E_{on} prediction model that delivers a 17-fold accuracy improvement over the conventional model (Fig. 2) and present causal-mechanism interpretations of switching waveforms across switching scenarios. Achieving such interpretability establishes a new fundamental groundwork for the foundational theoretical system, as well as for the design, optimization and standardization in semiconductor engineering and downstream applications. Furthermore, it enables future-generation co-design of semiconductors and applications, which are currently treated separately, for optimal system performance, including maximized system-level energy and emission savings and reliability.

In the following sections, we present SSIT concept, comparison of the calculated values using the new E_{on} prediction model derived from SSIT and conventional prediction model versus the measured results, present causal-mechanism interpretations

of typical switching waveforms across switching scenarios (Zero-Voltage-Switching (ZVS) and another iZVS scenarios are interpreted in *Methods: Causal-Mechanism Interpretation for switching waveforms within a Typical ZVS* and *Methods: Causal-Mechanism Interpretation for switching waveforms within another iZVS scenario*), and provide discussions with outlooks, followed by *Methods*.

SSIT concept

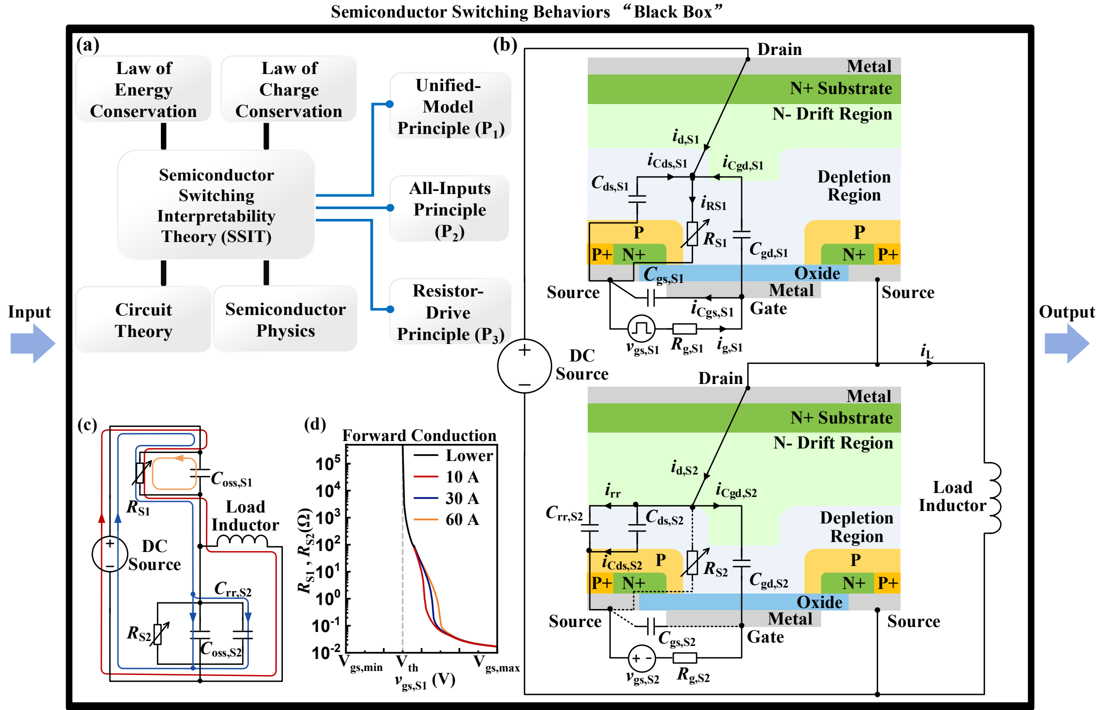


Fig. 1| Interpretability for semiconductor switching behaviors "black box". (a) Conceptual Illustration of the role of SSIT to bridge conservation laws of energy and charge, circuit theory and semiconductor physics, together with the three underlying principles of SSIT. (b) Illustration of the unified-model principle using an equivalent-circuit model of a MOSFET half-bridge with a load inductor, showing individual current components at a representative instant during VF under hard switching. (c) Simplified equivalent-circuit representation of (b), where the red current component denotes the load current; the blue current components denote the charging current component of S_2, supplied by the DC source and the orange current component denotes the discharging current of $C_{oss,S1}$ via S_1's channel. (d) R_{S1}–$v_{gs,S1}$ curve in forward conduction over the $v_{gs,S1}$ swing, where $V_{gs,max}$ and $V_{gs,min}$ denote the maximum and minimum $v_{gs,S1}$ during the switching transition, respectively. The red, blue and purple curves correspond to conducting current of 10 A, 30 A and 60 A, respectively; the black curve denotes the R_{S1}–$v_{gs,S1}$ relationship for $v_{gs,S1}$<4 V at lower current levels.

SSIT is grounded in the following three principles, namely Unified-Model Principle, All-Inputs Principle and Resistor-Drive Principle.

Principle 1 (P_1)—Unified-Model Principle: As detailed in *Methods: The unified equivalent-circuit model with variable resistors and variable capacitors*, the

semiconductor device is represented by a unified equivalent-circuit model[10,29,30] comprising a lumped variable resistor (e.g., with the resistance R_{S1} and R_{S2}) and lumped variable capacitors (e.g., with the capacitance $C_{oss,S1}$ and $C_{oss,S2}$) and reverse-recovery equivalents (e.g., with the capacitance $C_{rr,S1}$ and/or $C_{rr,S2}$). As a capacitive counterpart to the unified equivalent-circuit model of transformers[27] built from lumped inductors and resistors only, this model uses lumped capacitors and resistor(s) only, provides concise yet effective representations, enabling interpretations using circuit theory[10], and universal applicability across circuit topologies, device types, and all switching scenarios and subintervals.

Principle 2 (P_2)—All-Inputs Principle: All inputs that exert a non-negligible influence on switching behaviors must be incorporated into the analysis. For example, in a half-bridge with a load inductor, these inputs include the nonlinearity of output capacitances of both devices, and the charge and energy exchange associated with the load inductor and the DC source etc.

Principle 3 (P_3)—Resistor-Drive Principle: Resistance variation of the externally driven variable resistor R_{S1} is the driving force of the time evolution of the switching waveforms and interaction between the semiconductor device and other circuit elements, initiating and sustaining the entire switching causal chain. Accordingly, the onset of the turn-on process is defined by the initial rapid drop in R_{S1} that occurs when $v_{gs,S1}$ exceeds $V_{th,S1}$, as detailed in *Methods: Criterion for turn-on onset*.

Results comparison of E_{on} prediction models and measurement

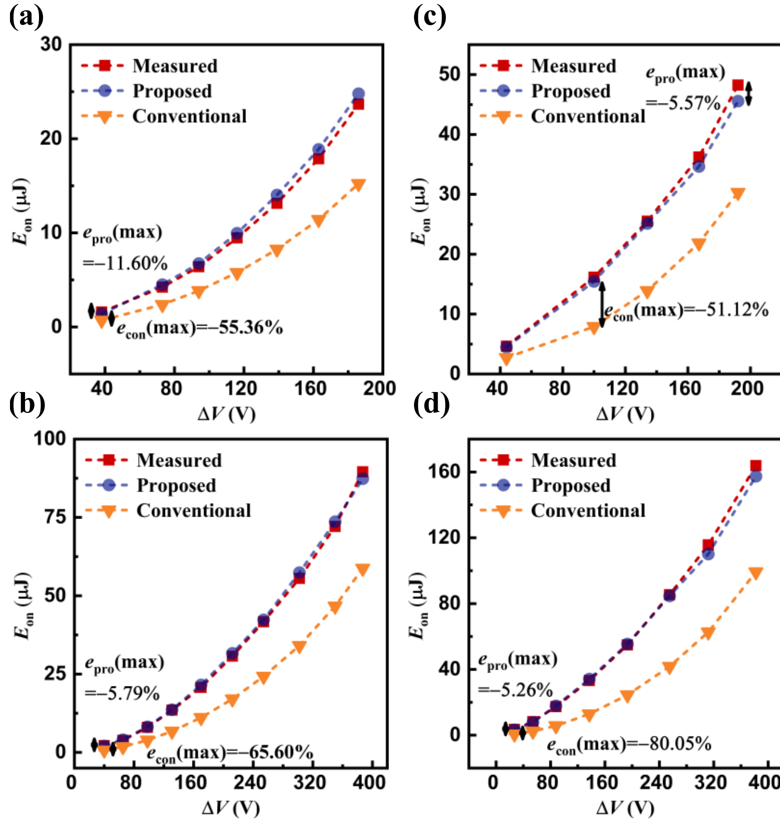


Fig. 2| Comparison of measured results (red) with calculated results from the proposed E_{on} prediction model (blue) and the conventional E_{on} model (orange). Measurements were performed using commercially available MOSFETs from Wolfspeed, specifically devices C2M0080120D and C2M0025120D. Results are shown for (a) V_{DC}=200 V with C2M0080120D; (b) V_{DC}=400 V with C2M0080120D; (c) V_{DC}=200 V with C2M0025120D and (d) V_{DC}=400 V with C2M0025120D.

Based on SSIT, we derived a new E_{on} prediction model for a typical iZVS scenario from charge and energy conservation, respectively, as detailed in *Methods: derivation for E_{on} prediction model in a typical iZVS*. Predicted values using the proposed model and conventional model are compared with experimental measurement results. It demonstrates that the proposed model achieves a 17-fold average error reduction compared to the conventional model.

Causal-Mechanism Interpretation for Switching Waveforms within a Typical Hard-Switching (HS)

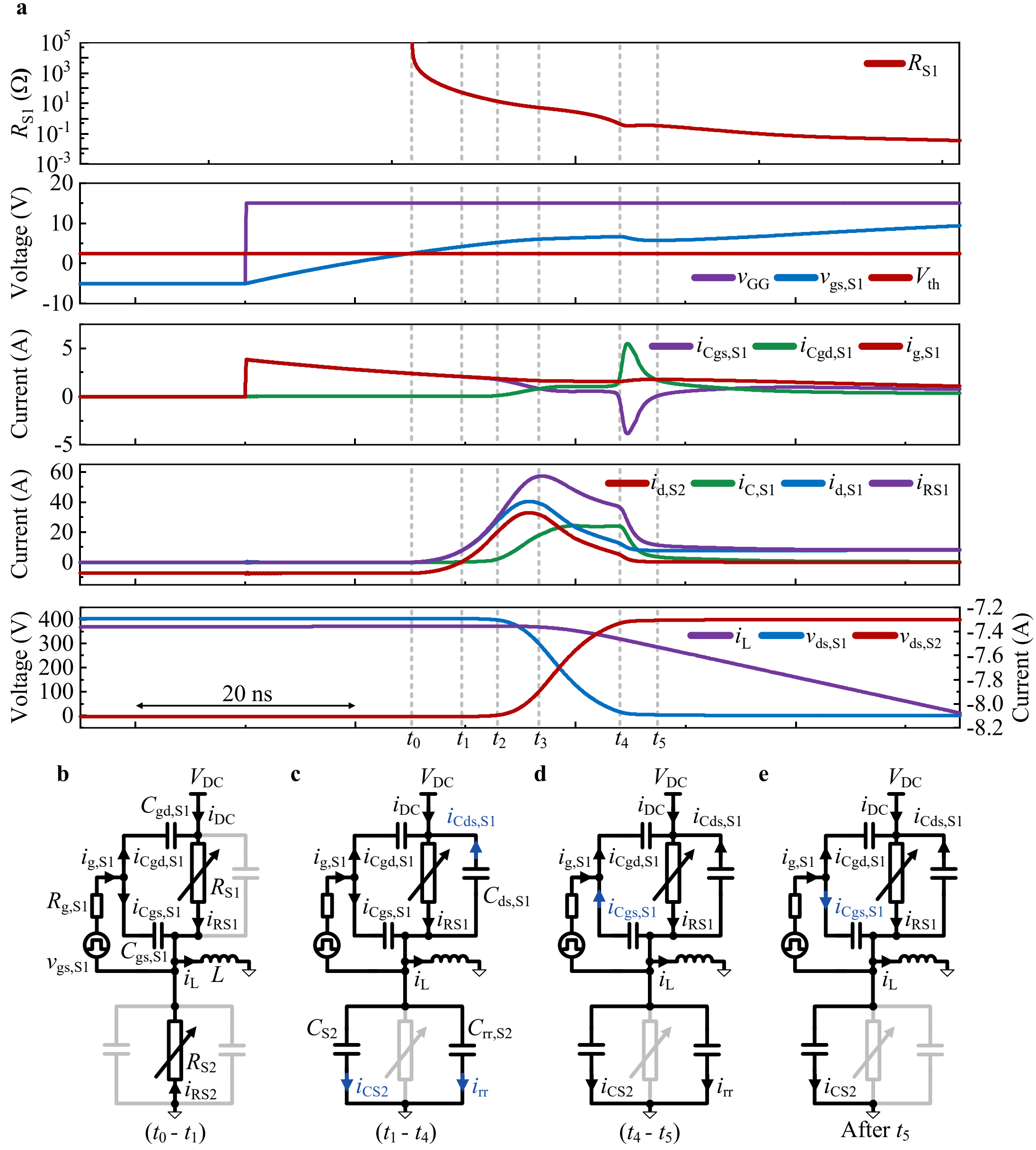


Fig. 3 | Causal-mechanism interpretation for switching waveforms within a typical HS. a, switching waveforms within a typical HS. **b**, Operation mode during subinterval (t_0-t_1). **c**, Operation mode during subinterval (t_1-t_4). **d**, Operation mode during subinterval (t_4-t_5). **e**, Operation mode after t_5. The equivalent-circuit model in **b, c, d** and **e** is obtained based on **P**$_1$**;** the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

At t_0 (i.e., the onset of HS), i_L is reverse-conducted by R_{S2}. During (t_0 - t_1), whilst $v_{ds,S1}$ remains nearly constant, with increasing $v_{gs,S1}$, R_{S1} decreases rapidly (by **P**$_3$), increasing i_{RS1}. As a result, a lossy CC occurs where i_L commutates from R_{S2} to R_{S1} (by **P**$_2$; accounting for influence of i_L).

At t_1, i_L is entirely conducted by R_{S1}, indicating the CC's completion; a RR and a VF commence simultaneously, where the excessive carriers in S_2 are removed by the

combined effects of recombination and $i_{d,S2}$, which is also known as reverse-recovery current. After t_1, $i_{d,S2}$ charges C_{S2} via R_{S1}, increasing $v_{ds,S2}$. As $V_{DC}=v_{ds,S1}+v_{ds,S2}$, whilst V_{DC} remains constant, $v_{ds,S1}$ drops, resulting in a discharging current through C_{S1} via R_{S1} (by **P2**; considering influence of DC source). Notably, during (t_1-t_5), $|dv_{ds,S2}/dt|=|i_{d,S2}|/(C_{S2}+C_{rr,S2})$.

During (t_1-t_3), a quicker relative drop in R_{S1} compared to $v_{ds,S1}$ (i.e., $|dR_{S1}/R_{S1}|>|dv_{ds,S1}/v_{ds,S1}|$) causes a continued increase in i_{RS1}, increasing $i_{d,S2}$ (by **P3**); meanwhile, as $v_{gs,S1}$ increases, $|dR_{S1}/R_{S1}|$ decreases, leading to a reduced *di/dt* of i_{RS1} (by **P3**).

During (t_1-t_2), although $C_{oss,S2}$ decreases (by **P2**; considering $C_{oss,S2}$'s nonlinearity) and $i_{d,S2}$ increases, causing an increase in S_2's *dv/dt*, S_2's *dv/dt* remains low due to high $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity). Therefore, only a small portion of $i_{g,S1}$ is required by $C_{gd,S1}$ to follow S_2's *dv/dt*, allowing most of $i_{g,S1}$ to charge $C_{gs,S1}$.

During (t_2-t_3), $C_{oss,S2}$ transitions from its high- to low-capacitance region, leading to an increase in S_2's *dv/dt* (by **P2**; considering $C_{oss,S2}$'s nonlinearity). As negative feedback, more $i_{g,S1}$ is diverted to $C_{gd,S1}$, leading to: (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, which slows the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction (by **P3**) and consequently slowing i_{RS1} increase. The slower increase in i_{RS1}, combined with a significant increase in $i_{C,S1}$, reduces *di/dt* of $i_{d,S2}$ – initially positive then turning negative before t_3 – thus limiting the increase in S_2's *dv/dt* despite decreasing $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity). As a result of the negative feedback, $C_{gd,S1}$'s *dv/dt* follows S_2's *dv/dt*.

During (t_3-t_4), the quicker relative reduction in $v_{ds,S1}$ than the relative reduction in R_{S1} (by **P3**), causes a decrease in i_{RS1}. Initially, as $C_{ds,S1}$ and $C_{gd,S1}$ increase whilst *dv/dt* changes insignificantly, $i_{C,S1}$ has a brief increase; slightly more $i_{g,S1}$ is diverted to $C_{gd,S1}$. Both decreasing i_{RS1} and increasing $i_{C,S1}$ contribute to a decrease in $i_{d,S2}$. After that, i_{RS1} continues to drop, decreasing $i_{d,S2}$, which leads to a decreasing S_2's *dv/dt*. As S_2's *dv/dt* decreases whilst $C_{ds,S1}$ and $C_{gd,S1}$ increase (by **P2**; considering nonlinearity of $C_{ds,S1}$ and $C_{gd,S1}$), $i_{Cds,S1}$ and $i_{Cgd,S1}$ nearly stabilize.

During (t_4-t_5), as $v_{ds,S1}$ falls, $C_{gd,S1}$ enters its high-capacitance region and rises

sharply (by **P2**; considering $C_{gd,S1}$'s nonlinearity). In contrast, as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low (by **P2**; considering $C_{oss,S2}$'s nonlinearity), whilst $i_{d,S2}$ sustains a significant *dv/dt*, $i_{Cgd,S1}$ must remain sufficient to sustain a comparable *dv/dt* for $C_{gd,S1}$. Consequently, limited $i_{g,S1}$ causes further negative feedback – a drop in $v_{gs,S1}$, which boosts $i_{g,S1}$, strengthening $i_{Cgd,S1}$; simultaneously it causes R_{S1}'s rise (by **P3**), combined with $v_{ds,S1}$ reduction, lowering i_{RS1}, and suppressing $i_{d,S2}$ and thus S_2's *dv/dt*. Besides, a supplementary current pulse from $C_{gs,S1}$ results to help discharge $C_{gd,S1}$ via R_{S1}. These effects ensure that $C_{gd,S1}$'s *dv/dt* follows S_2's *dv/dt*. These also explain the causal mechanism associated with the drop in $v_{gs,S1}$ at the end of the Miller plateau.

After t_5, as $v_{gs,S1}$ further increases, R_{S1} decreases slowly (by **P3**), causing a slight drop in mid-point voltage and consequently a minor discharge and charge of C_{S1} and C_{S2} via R_{S1}, respectively.

Causal-Mechanism Interpretation for Switching Waveforms within a Typical iZVS

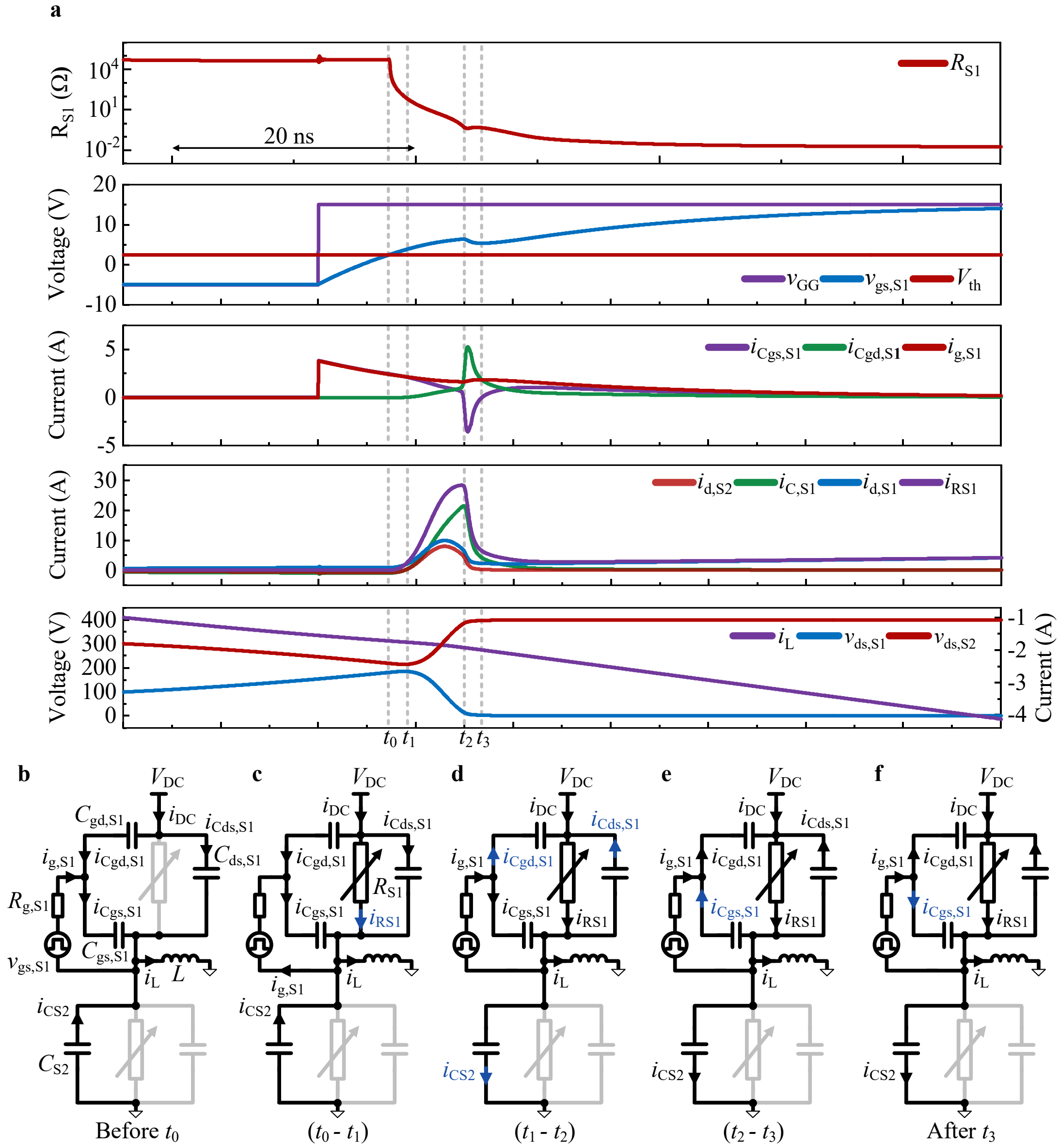


Fig. 4| **Causal-mechanism interpretation for switching waveforms within a typical iZVS. a**, Switching waveforms within a typical iZVS (i_L flows out from the half-bridge midpoint throughout the entire iZVS). **b**, Operation mode before t_0. **c**, Operation mode during subinterval (t_0-t_1). **d**, Operation mode during subinterval (t_1-t_2). (e) Operation mode (t_2-t_3). (f) Operation mode after t_3. The equivalent-circuit model in **b**, **c**, **d**, **e** and **f** is obtained based on **P₁;** the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

Before t_0 (i.e., the onset of the iZVS), i_{L} charges C_{S1} and discharges C_{S2} simultaneously. During (t_0-t_1), i_{L} continues to charge C_{S1} and discharge C_{S2} simultaneously; as $v_{\mathrm{gs,S1}}$ is larger than $V_{\mathrm{th,S1}}$ and continues to increase, R_{S1} decreases (by **P₃**), increasing i_{RS1}. Consequently, i_{L} gradually commutates to R_{S1}, till t_1, at which point the entire i_{L} is conducted by R_{S1} (by **P₂**; accounting for influence of i_{L}).

During (t_1-t_2), initially, as $v_{gs,S1}$ continues to increase, R_{S1} decreases (by **P3**), increasing i_{RS1}, which increases i_{CS2}. Combined with lower $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity), increasing i_{CS2} leads to a higher S_2's *dv/dt*. This triggers negative feedback: more $i_{g,S1}$ is diverted to $C_{gd,S1}$, causing (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, slowing the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction (by **P3**) and consequently slowing i_{RS1} increase. The slower increase in i_{RS1}, combined with a rapid increase in i_{CS1}, reduces the *di/dt* of $i_{d,S2}$ – initially positive, turning negative before t_3 - limiting S_2's *dv/dt* despite decreasing $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity). These combined effects enable $C_{gd,S1}$'s *dv/dt* to follow S_2's *dv/dt*. These interpretations also explain the causal mechanism underlying the observed phenomenon whereby i_{RS1} discharges C_{S1} and charges C_{S2} simultaneously, whilst supplying i_L during (t_1-t_2).

During (t_2-t_3), $C_{gd,S1}$ is in its high-capacitance region, increasing rapidly as $v_{ds,S1}$ decreases; as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low; as $i_{d,S2}$ remains significant, S_2's *dv/dt* remains significant (by **P2**; considering $C_{gd,S1}$'s and $C_{oss,S2}$'s nonlinearity). Consequently, $C_{gd,S1}$'s *dv/dt* has to remain significant. The insufficient $i_{g,S1}$ to maintain $C_{gd,S1}$'s *dv/dt* to track S_2's *dv/dt*, triggers further negative feedback – a drop in $v_{gs,S1}$. This boosts $i_{g,S1}$, enhancing $i_{Cgd,S1}$, but also increases R_{S1} (by **P3**), and with decreasing $v_{ds,S1}$, leading to a rapid reduction in i_{RS1}, and consequently a lower $i_{d,S2}$, thereby a lower S_2's *dv/dt*. Meanwhile, $C_{gs,S1}$ supplies a pulse current to help discharge $C_{gd,S1}$ via S_1's channel. Together, these effects enable $C_{gd,S1}$'s *dv/dt* to follow S_2's *dv/dt.* These interpretations also explain the causal mechanism associated with the drop in $v_{gs,S1}$ at the end of the Miller plateau.

After t_3, $C_{gs,S1}$ stops discharging and is instead charged by $i_{g,S1}$, which charges both $C_{gs,S1}$ and $C_{gd,S1}$ simultaneously. As $v_{gs,S1}$ further increases, R_{S1} decreases slowly (by **P3**), causing a slight rise in midpoint voltage and consequently a minor discharge of C_{S1} and charge of C_{S2} via R_{S1}.

Discussion and outlook

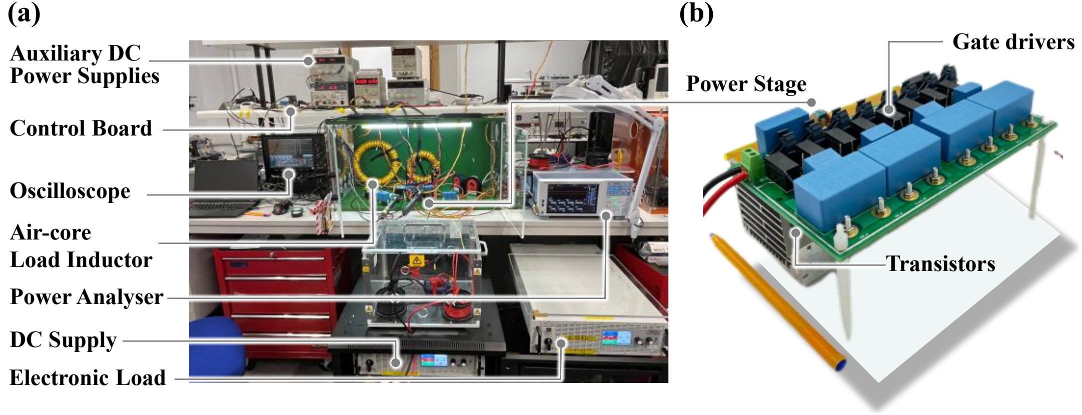
Here we present SSIT to provide interpretability that causally links inputs and output responses of the semiconductor switching behaviors “black box”, by bridging

circuit theory[10], conservation laws of energy and charge and semiconductor physics. As an example of SSIT's implications, we derived an E_{on} prediction model (errors: 0.88—11.60%) achieving 17-fold averaged error reduction compared to the conventional model (errors: 34.41—80.05%), and providing unprecedented casual-mechanism interpretations for switching waveforms across switching scenarios. As detailed in *Methods: derivation for E_{on} prediction model in a typical iZVS*, we validated the fundamental applicability and equivalence of the energy- and charge-conservation-based analytical frameworks for switching energy analyses, and revealed complementary perspectives: energy conservation emphasizes the initial and final energy states, whilst charge conservation describes the transient charge evolution.

Such interpretability establishes a new fundamental groundwork for the foundational theoretical system, as well as for the design, optimization and standardization in semiconductor engineering and downstream applications individually. It also opens directions across disciplines including semiconductor materials,[11,12] semiconductor physics,[44] semiconductor engineering,[13,14] packaging,[15,16] reliability,[17,18] thermal management;[19,20] and downstream applications including power electronics and potentially higher-frequency communications and computation devices and integrated circuits.[21,22]

SSIT further enables future-generation co-design of semiconductors and applications, which are currently treated separately, to optimize system performance. The interpretability provided by SSIT enables semiconductor materials, chip design, packaging and thermal management to be informed by application-level requirements, rather than heuristic optimization such as lower on-resistance and input capacitance in device structure design[45]. It further supports co-optimization across the design chain such as semiconductor engineering, topology selection, printed circuit board (PCB) and magnetic component design, and control strategies. One of the immediate implications is support for minimizing semiconductor energy losses, which within power electronics alone are estimated to exceed 10% of global electricity consumption and emissions. SSIT may further extend across EEE sub-fields, including communication and computation systems.

Extended Data - Experimental platform



Extended Data Fig. 1. Experimental platform for E_{on} measurement, using a power electronic converter as the demonstrative example. **(a)** Overview picture of the entire experimental platform. **(b)** Close-up picture of the power electronic converter.

Table 2. Detailed comparison of E_{on} measured results with calculated values using the proposed and conventional prediction models, respectively

CREE 1.2Kv 2nd -gen SiC MOSFET (mΩ)	V_{DC} (V)	ΔV (V)	Measured results (μJ)	Calculated values using conventional prediction (μJ) (*Error*(conventional))	Calculated values using proposed prediction (μJ) (*Error*(proposed))	Error reduction |*Error*(conventional)/ *Error*(proposed)|
25	200	44	4.65	2.74 (–41.11%)	4.49 (–3.57%)	11.50
25	200	100	16.17	7.91 (–51.12%)	15.45 (–4.50%)	11.35
25	200	134	25.53	13.91 (–45.52%)	25.14 (–1.53%)	29.67
25	200	167	36.25	21.88 (–39.64%)	34.65 (–4.41%)	8.98
25	200	192	48.25	30.31 (–37.19%)	45.57 (–5.57%)	6.68
25	400	27	3.52	0.70 (–80.05%)	3.33 (–5.26%)	15.21
25	400	54	8.25	2.39 (–71.02%)	7.87 (–4.58%)	15.49
25	400	88	17.36	5.75 (–66.91%)	17.88 (2.95%)	22.66
25	400	137	33.21	12.91 (–61.11%)	34.14 (2.82%)	21.67
25	400	193	54.94	24.46 (–55.48%)	55.46 (0.94%)	58.75
25	400	255	85.42	41.79 (–51.08%)	84.67 (–0.88%)	57.75
25	400	312	115.68	62.76 (–45.75%)	110.10 (–4.82%)	9.49
25	400	382	163.86	99.24 (–39.44%)	157.42 (–3.93%)	10.02
80	200	38	1.59	0.709 (–55.36%)	1.40 (-11.60%)	4.77
80	200	73	4.24	2.38 (–43.78%)	4.50 (6.10%)	7.17
80	200	94	6.40	3.85 (–39.77%)	6.74 (5.40%)	7.37
80	200	116	9.47	5.78 (–38.91%)	9.96 (5.18%)	7.51
80	200	139	13.14	8.26 (–37.13%)	14.02 (6.70%)	5.54
80	200	163	17.88	11.42 (–36.11%)	18.87 (5.56%)	6.49
80	200	186	23.68	15.23 (–35.69%)	24.79 (4.69%)	7.61
80	400	40	2.17	0.748 (–65.60%)	2.05 (–5.79%)	11.33
80	400	65	3.89	1.82 (–53.14%)	4.06 (4.50%)	11.81
80	400	98	8.03	3.92 (–51.21%)	8.20 (2.12%)	24.13
80	400	131	13.50	6.77 (–49.82%)	13.66 (1.25%)	39.99
80	400	170	20.77	11.13 (–46.40%)	21.54 (3.73%)	12.45
80	400	212	30.73	17.05 (–44.53%)	31.65 (2.98%)	14.93

80	400	254	41.71	24.28 (−41.79%)	42.34 (1.51%)	27.70
80	400	302	55.54	34.10 (−38.61%)	57.40 (3.34%)	11.54
80	400	350	72.14	46.67 (−35.31%)	73.67 (2.11%)	16.70
80	400	387	89.57	58.75 (−34.41%)	87.35 (−2.49%)	13.85

Methods

The unified equivalent-circuit model with variable resistors and variable capacitors

Taking a MOSFET-based half-bridge as an example, the equivalent-circuit model of S_1's conductive current path is represented by a lumped variable resistor,[10,29,30] with its resistance defined by Ohm's law, namely $R_{S1}=v_{ds,S1}/i_{RS1}$, where i_{RS1} includes all the conductive current components, as opposed to displacement current components across junction capacitances (i.e., capacitive current components). R_{S1} aggregates all resistive elements along the i_{RS1} path, including the channel resistance, accumulation region resistance, JFET region resistance, drift region resistance and contact resistance etc.[26] The R_{S1} model applies to all device types, for both forward and reverse conduction, at any gate voltage. Specifically, the I–V characteristic follows the output characteristic in forward conduction and the third-quadrant (body-diode) characteristic in reverse conduction. At any operating point, R_{S1} is given by the reciprocal slope of the line connecting the operating point and the origin of the I-V curve. With the same modelling, R_{S2} model applies to S_2; when a shoot-through event occurs across the half bridge, an additional current component flows through R_{S2}.

Regarding S_1's capacitive current paths, variable-capacitance equivalent-circuit models are used for representation.[10,29,30] Both the displacement current components of $C_{ds,S1}$ and $C_{gd,S1}$ traverse the channel, accumulation region, JFET region and drift region. As the aggregate resistance of these regions dominates R_{S1} both $C_{ds,S1}$ and $C_{gd,S1}$ could be approximated as being directly in parallel with R_{S1}. For simplicity, they are combined into a single lumped output capacitance $C_{oss,S1}$, directly in parallel with R_{S1}.

The reverse-recovery effects within S_1 and S_2 are represented by lumped variable capacitors, namely $C_{rr,S1}$ and $C_{rr,S2}$ in parallel with $C_{oss,S1}$ and $C_{oss,S2}$, respectively. As no RR occurs in S_1 during its turn-on, $C_{rr,S1}$ is zero, equivalent to an open circuit; in the

case that RR occurs in S_2, $C_{\mathrm{rr},S2}$ is a non-zero variable capacitor.

Criterion for turn-on onset

Consistent with SSIT, the onset is defined as the moment that the initial rapid drop in R_{S1} occurs, triggered by $v_{\mathrm{gs},S1}$ exceeding the threshold. Each threshold crossing increments the turn-on event count by one. As all switching phenomena evolve from this initial rapid drop in R_{S1}, this event is also identified as the starting point for time evolution and causal reasoning.

Derivation for E_{on} prediction model in a typical iZVS

Derivation from charge conservation

In all the turn-on scenarios, since the energy dissipated in the ESR of C_{S1} is negligible compared to that along the i_{RS1} paths[46,47] it is valid to assume that the entire $E_{\mathrm{on},S1}$ is incurred in R_{S1}. Hence, $E_{\mathrm{on},S1}$ is given by

$$E_{on,S1}=\int_{switching\text{-}ON} v_{ds,S1}(t)\,i_{RS1}(t)\,dt\,. \tag{1}$$

In case-2 iZVS process, as vast majority of the energy dissipation during S_1's turn-on is incurred during $(t_0 - t_3)$, it is valid to assume the dissipated energy incurred during $(t_0 - t_3)$ is $E_{\mathrm{on},S1}$.

Applying Kirchhoff's Current Law (KCL) at S_1's drain terminal, yielding

$$i_{RS1}(t)=i_{d,S1}(t)+i_{C_{gd},S1}(t)+i_{C_{ds},S1}(t)+i_{par,C_{gd},S1}(t)+i_{par,C_{ds},S1}(t)\,. \tag{2}$$

Substitute (2) into (1), yielding the expression of $E_{\mathrm{on},S1}$, given by

$$\begin{aligned}E_{on,S1}=&\int_{switching-ON} v_{ds,S1}(t)\,i_{d,S1}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{gd},S1}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{ds},S1}(t)\,dt\\&+\int_{switching-ON} v_{ds,S1}(t)\,i_{par,C_{gd},S1}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{par,C_{ds},S1}(t)\,dt\end{aligned}\,. \tag{3}$$

As $v_{\mathrm{gs},S1}$ during $(t_0 - t_3)$ is negligibly small compared to ΔV, it can be approximated as a constant V_{gp}; ΔV-V_{gp} can be approximated to ΔV and 0 V-V_{gp} can be approximated to 0 V. Therefore, the summation of 2$^{\mathrm{nd}}$, 3$^{\mathrm{rd}}$, 4$^{\mathrm{th}}$ and 5$^{\mathrm{th}}$ terms of the expression of $E_{\mathrm{on},S1}$ could be approximated as

$$\begin{aligned}&\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{gd},S1}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{ds},S1}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{par,gd,S1}}(t)\,dt+\int_{switching-ON} v_{ds,S1}(t)\,i_{C_{par,ds,S1}}(t)\,dt\\
=&\underbrace{E_{oss,S1}(\Delta V)}_{\text{Energy dissipated by output capacitance of } S1}+\underbrace{\int_{0-V_{gp}}^{\Delta V-V_{gp}} v_{ds,S1}C_{par,gd,S1}(v_{gd,S1})\,dv_{gd,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{gd,S1}}+\underbrace{\int_{0}^{\Delta V} v_{ds,S1}C_{par,ds,S1}\,dv_{ds,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{ds,S1}}\\
\approx&\underbrace{E_{oss,S1}(\Delta V)}_{\text{Energy dissipated by output capacitance of } S1}+\underbrace{\int_{0}^{\Delta V} v_{ds,S1}C_{par,gd,S1}(v_{gd,S1})\,dv_{gd,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{gd,S1}}+\underbrace{\int_{0}^{\Delta V} v_{ds,S1}C_{par,ds,S1}\,dv_{ds,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{ds,S1}}\\
=&\underbrace{E_{oss,S1}(\Delta V)}_{\text{Energy dissipated in RS1 due to discharge of S1's output capacitance}}+\underbrace{\frac{1}{2}C_{par,S1}\Delta V^2}_{\text{Energy dissipated in RS1 due to discharge of S1's paralleled capacitance}}\end{aligned}\,. \tag{4}$$

Besides, the charge obtained by $C_{gd,S2}$, $C_{ds,S2}$ and the charge obtained by their paralleled capacitances during ($t_0 - t_3$), are given by

$$\begin{aligned}\Delta Q_{S2} &= \int_{switching-ON} i_{Cgd,S2}(t)\,dt + \int_{switching-ON} i_{Cds,S2}(t)\,dt \\ &= \int_{V_{DC}-\Delta V-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{gd,S2}\,dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}\,dv_{ds,S2} \\ &\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2}\,dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}\,dv_{ds,S2} \\ &= Q_{oss,S2}(V_{DC}) - Q_{oss,S2}(V_{DC}-\Delta V)\end{aligned} ; \quad (5)$$

$$\begin{aligned}&\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{par,gd,S2}(v_{gd})\,dv_{gd} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds})\,dv_{ds} \\ &\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2}(v_{gd})\,dv_{gd} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds})\,dv_{ds} \\ &= \left[\int_0^{V_{DC}} C_{par,gd,S2}(v_{gd})\,dv_{gd} - \int_0^{V_{DC}-\Delta V} C_{par,gd,S2}(v_{gd})\,dv_{gd}\right] + \left[\int_0^{V_{DC}} C_{par,ds,S2}(v_{ds})\,dv_{ds} - \int_0^{V_{DC}-\Delta V} C_{par,ds,S2}(v_{ds})\,dv_{ds}\right] \\ &= C_{par,gd,S2}\Delta V + C_{par,ds,S2}\Delta V \\ &= C_{par,S2}\Delta V\end{aligned} . \quad (6)$$

Applying Kirchhoff's Voltage Law (KVL) across the loop incorporating the DC source, S_1 and S_2, yielding

$$V_{DC} = v_{ds,S1}(t) + v_{ds,S2}(t). \quad (7)$$

Applying KCL at the source terminal of S_2, yielding

$$i_{DC}(t) = i_{d,S2}(t) - i_L(t) = i_{RS2}(t) + i_{C,S2}(t) - i_L(t). \quad (8)$$

Hence, the 1st term of the expression of $E_{on,S1}$ could be derived as

$$\begin{aligned}&\int_{switching-ON} v_{ds,S1}(t)\,i_{d,S1}(t)\,dt \\ &= \int_{switching-ON} V_{DC}\,i_{DC}(t)\,dt - \int_{switching-ON} v_{ds,S2}(t)\left[i_{d,S2}(t) - i_L(t)\right]dt \\ &= V_{DC}\int_{switching-ON}\left[i_{RS2}(t) + i_{C,S2}(t) - i_L(t)\right]dt - \int_{switching-ON} v_{ds,S2}(t)\,i_{d,S2}(t)\,dt + \int_{switching-ON} v_{ds,S2}(t)\,i_L(t)\,dt\end{aligned} . \quad (9)$$

where

$$\begin{aligned}\int_{switching-ON} v_{ds,S2}(t)\,i_{d,S2}(t)\,dt = &\underbrace{\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2}C_{gd,S2}(v_{gd,S2})\,dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{ds,S2}(v_{ds,S2})\,dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}} \\ &+ \underbrace{\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2}C_{par,gd,S2}(v_{gd,S2})\,dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}'s\ paralleled\ capacitance} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{ds,S2}(v_{ds,S2})\,dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}'s\ paralleled\ capacitance} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\,i_{RS2}(t)\,dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through}\end{aligned} . \quad (10)$$

(10) could be approximated to

$$
\begin{aligned}
&\int_{switching-ON} v_{ds,S2}(t)\, i_{d,S2}(t)\, dt \\
&\approx \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S1} C_{gd,S2}(v_{gd,S2})\, dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2} C_{ds,S2}(v_{ds,S2})\, dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S1} C_{par,gd,S2}(v_{gd,S2})\, dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}'s\ paralleled\ capacitance} \\
&+ \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2} C_{par.ds,S2}(v_{ds,S2})\, dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}'s\ paralleled\ capacitance} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_{RS2}(t)\, dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through} \\
&= \underbrace{E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)}_{Energy\ stored\ by\ C_{oss,S2}} + \underbrace{\frac{1}{2}(C_{par,gd,S2}+C_{par,ds,S2})\left[V_{DC}^{\ 2}-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_{RS2}(t)\, dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through} \\
&= \underbrace{E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)}_{Energy\ stored\ by\ C_{oss,S2}} + \underbrace{\frac{1}{2}C_{par,S2}\left[V_{DC}^{\ 2}-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_{RS2}(t)\, dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through}
\end{aligned}
\quad .(11)
$$

It is important to note that

$$
\int_{switching-ON} i_{C,S2}(t)\, dt = \Delta Q_{S2} + C_{par,S2}\Delta V\ . \quad (12)
$$

Combining (3)(4)(5)(6)(7)(8)(9)(10)(11)(12), yielding the $E_{\mathrm{on,S1}}$ prediction model derived from the perspective of charge conservation, given by

$$
\begin{aligned}
E_{on,S1} &\approx \underbrace{V_{DC}\left[\int_{switching-ON} i_{RS2}(t)\, dt + \Delta Q_{S2} + C_{par,S2}\Delta V - \int_{switching-ON} i_L(t)\, dt\right]}_{Energy\ provided\ by\ DC\ source\ to\ the\ half-bridge} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_L(t)\, dt}_{Energy\ provided\ by\ the\ overall\ AC-link\ impedance\ to\ the\ half-bridge} \\
&- \underbrace{\left[E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)\right]}_{Energy\ stored\ by\ output\ capacitance\ of\ S2} - \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_{RS2}(t)\, dt}_{Energy\ dissipated\ in\ S2\ due\ to\ shoot-through} - \underbrace{\frac{1}{2}C_{par,S2}\left[V_{DC}^{\ 2}-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} \\
&+ \underbrace{E_{oss,S1}(\Delta V) + \frac{1}{2}C_{par,S1}\Delta V^2}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1's\ output\ capacitance\ and\ paralleled\ capacitance}
\end{aligned}
\quad .(13)
$$

Derivation from energy conservation

The half-bridge during the S_1's turn-on process is taken as the study object. For simplicity reasons, the analysis is limited to (t_0 – t_3) as vast majority of the energy dissipation during S_1's turn-on is incurred during this interval. According to the law of energy conservation, the overall energy initially stored in the study object, minus the various dissipated energies incurred during the turn-on process and the energy delivered to the external circuit, yields the remaining stored energy at the end of the interval. The general mathematical expression is given by

$$
E_{initial} - E_{dissipated} - E_{delivered} = E_{final}\ , \quad (14)
$$

where E_{initial} denotes the overall energy stored in the study object at the initial instant; $E_{\mathrm{dissipated}}$ denotes the total energy losses during S_1's turn-on process, including but not limited to turn-on loss and ESR losses; $E_{\mathrm{delivered}}$ denotes the energy delivered to the external circuit; E_{final} denotes the total energy stored in the study object at the end of

the process. Among them, E_{initial} and E_{final} are given by

$$\begin{aligned} E_{initial} &= \left[E_{gd,S1}\left(\Delta V - v_{gs,S1}(t_0)\right) + E_{ds,S1}(\Delta V) + \frac{1}{2}C_{par,gd,S1}\left(\Delta V - v_{gs,S1}(t_0)\right)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\ &+ \left[E_{gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}(t_0)\right) + E_{ds,S2}(V_{DC} - \Delta V) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}(t_0)\right)^2 + \frac{1}{2}C_{par,ds,S2}(V_{DC} - \Delta V)^2 \right] \\ &= \left[E_{gd,S1}\left(\Delta V - V_{th,S1}\right) + E_{ds,S1}(\Delta V) + \frac{1}{2}C_{par,gd,S1}\left(\Delta V - V_{th,S1}\right)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\ &+ \left[E_{gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}(t_0)\right) + E_{ds,S2}(V_{DC} - \Delta V) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}(t_0)\right)^2 + \frac{1}{2}C_{par,ds,S2}(V_{DC} - \Delta V)^2 \right] \end{aligned} ;$$

(15)

$$\begin{aligned} E_{final} &= \left[E_{gd,S1}\left(-V_{th,S1}\right) + E_{ds,S1}(0) + \frac{1}{2}C_{par,gd,S1}\left(0 - V_{th,S1}\right)^2 + \frac{1}{2}C_{par,ds,S1}0^2 \right] \\ &+ \left[E_{gd,S2}\left(V_{DC} - v_{gs,S2}(t_0)\right) + E_{ds,S2}(V_{DC}) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - v_{gs,S2}(t_0)\right)^2 + \frac{1}{2}C_{par,ds,S2}V_{DC}^2 \right] \end{aligned} . \quad (16)$$

where $v_{\text{gs,S1}}(t_0)=V_{\text{th,S1}}$. As both $v_{\text{gs,S1}}$ and $v_{\text{gs,S2}}$ during the process are negligibly small compared to ΔV and V_{DC}-ΔV, both $v_{\text{gs,S1}}$ and $v_{\text{gs,S2}}$ can be approximated to 0 V, yielding

$$\begin{aligned} E_{initial} &\approx \left[E_{gd,S1}(\Delta V) + E_{ds,S1}(\Delta V) + \frac{1}{2}C_{par,gd,S1}(\Delta V)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\ &+ \left[E_{gd,S2}(V_{DC} - \Delta V) + E_{ds,S2}(V_{DC} - \Delta V) + \frac{1}{2}C_{par,gd,S2}(V_{DC} - \Delta V)^2 + \frac{1}{2}C_{par,ds,S2}(V_{DC} - \Delta V)^2 \right] ; \\ &= \left[E_{oss,S1}(\Delta V) + \frac{1}{2}C_{par,S1}(\Delta V)^2 \right] + \left[E_{oss,S2}(V_{DC} - \Delta V) + \frac{1}{2}C_{par,S2}(V_{DC} - \Delta V)^2 \right] \end{aligned} \quad (17)$$

$$\begin{aligned} E_{final} &\approx E_{gd,S2}(V_{DC}) + E_{ds,S2}(V_{DC}) + \frac{1}{2}C_{par,gd,S2}V_{DC}^2 + \frac{1}{2}C_{par,ds,S2}V_{DC}^2 \\ &= E_{oss,S2}(V_{DC}) + \frac{1}{2}C_{par,S2}V_{DC}^2 \end{aligned} . \quad (18)$$

During S_1's iZVS process , the energy dissipation caused by ESR is negligible compared to $E_{\text{dissipated}}$. The dominant dissipated energy arises from $E_{\text{on,S1}}$ and the dissipated energy within S_2 due to the shoot-through effect. Hence, $E_{\text{dissipated}}$ can be approximated as consisting only of these two components, namely

$$E_{dissipated} \approx E_{on,S1} + E_{dissipated,S2} , \quad (19)$$

where $$E_{dissipated,S2} = \underbrace{\int_{switching-ON} v_{ds,S2}(t)\, i_{RS2}(t)\, dt}_{Energy\ dissipated\ \text{in}\ S2\ due\ to\ shoot-through} .$$

(20)

Regarding the energy delivered to the external circuit, $E_{\text{delivered}}$ could be obtained as

$$E_{delivered} = -(W_{DC} + W_L) \quad (21)$$

where W_{DC} and W_{L} denote the work done by the DC source and load inductor to the study object, respectively.

In order to obtain W_{DC}, it is important to obtain the total charge obtained by the DC source, denoted ΔQ_{DC} during the process. Applying KCL at S_2's source terminal,

yielding

$$i_{DC}\left(t\right)=i_{d,S2}\left(t\right)-i_{L}\left(t\right)=i_{C,S2}\left(t\right)+i_{RS2}\left(t\right)-i_{L}\left(t\right). \tag{22}$$

Integrating both sides of (22), yielding

$$\Delta Q_{DC}=\int\limits_{switching-ON} i_{DC}\left(t\right)dt=\int\limits_{switching-ON} i_{C,S2}\left(t\right)dt+\int\limits_{switching-ON} i_{R,S2}\left(t\right)dt-\int\limits_{switching-ON} i_{L}\left(t\right)dt, \tag{23}$$

where

$$\begin{aligned}
&\int\limits_{switching-ON} i_{C,S2}\left(t\right)dt\\
&=\int\limits_{switching-ON} i_{Cgd,S2}\left(t\right)dt+\int\limits_{switching-ON} i_{Cds,S2}\left(t\right)dt+\int\limits_{switching-ON} i_{Cpar,gd,S2}\left(t\right)dt+\int\limits_{switching-ON} i_{Cpar,ds,S2}\left(t\right)dt\\
&=\int\limits_{switching-ON} C_{gd,S2}\frac{dv_{gd,S2}}{dt}dt+\int\limits_{switching-ON} C_{ds,S2}\frac{dv_{ds,S2}}{dt}dt\\
&+\int\limits_{switching-ON} C_{par,gd,S2}\frac{dv_{gd,S2}}{dt}dt+\int\limits_{switching-ON} C_{par,ds,S2}\frac{dv_{ds,S2}}{dt}dt\\
&=\int_{V_{DC}-\Delta V-v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{gd,S2}dv_{gd,S2}+\int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}dv_{ds,S2}\\
&+\int_{V_{DC}-\Delta V-v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{par,gd,S2}dv_{gd,S2}+\int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}dv_{ds,S2}
\end{aligned}. \tag{24}$$

As $v_{gs,S2}$ is negligibly small compared to V_{DC}-ΔV during the process, (24) could be approximated to

$$\begin{aligned}
&\int\limits_{switching-ON} i_{C,S2}\left(t\right)dt\\
&\approx\int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2}dv_{gd,S2}+\int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}dv_{ds,S2}+\int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2}dv_{gd,S2}+\int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}dv_{ds,S2}\\
&=Q_{oss,S2}\left(V_{DC}\right)-Q_{oss,S2}\left(V_{DC}-\Delta V\right)+\left(C_{par,gd,S2}+C_{par,ds,S2}\right)\Delta V\\
&=\Delta Q_{S2}+C_{par,S2}\Delta V
\end{aligned}. \tag{25}$$

Therefore, ΔQ_{DC} is obtained as

$$\Delta Q_{DC}\approx\Delta Q_{S2}+C_{par,S2}\Delta V+\int\limits_{switching-ON} i_{RS2}(t)dt-\int\limits_{switching-ON} i_{L}(t)dt. \tag{26}$$

Hence, W_{DC} is obtained as

$$\begin{aligned}
W_{DC}&=\int\limits_{switching-ON} V_{DC}i_{DC}\left(t\right)dt=V_{DC}\Delta Q_{DC}\\
&=V_{DC}\left[\Delta Q_{S2}+C_{par,S2}\Delta V+\int\limits_{switching-ON} i_{RS2}\left(t\right)dt-\int\limits_{switching-ON} i_{L}\left(t\right)dt\right]
\end{aligned}. \tag{27}$$

In terms of the work done by the load inductor W_L, it could be obtained as

$$W_{L}=\int\limits_{switching-ON} v_{L}\left(t\right)i_{L}\left(t\right)dt=\int\limits_{switching-ON} v_{ds,S2}\left(t\right)i_{L}\left(t\right)dt. \tag{28}$$

Substituting (27) and (28) into (21), yielding

$$\begin{aligned}
&E_{delivered}=-\left(W_{DC}+W_{L}\right)=\\
&=-V_{DC}\left[\Delta Q_{S2}+C_{par,S2}\Delta V+\int\limits_{switching-ON} i_{RS2}\left(t\right)dt-\int\limits_{switching-ON} i_{L}\left(t\right)dt\right]-\int\limits_{switching-ON} v_{ds,S2}\left(t\right)i_{L}\left(t\right)dt
\end{aligned}. \tag{29}$$

Substituting (17),(18),(19),(20),(29) into (14), yielding the $E_{on,S1}$ prediction model, given by

$$E_{on,S1} \approx \underbrace{V_{DC}\left[\int\limits_{switching-ON} i_{RS2}(t)dt + \Delta Q_{S2} + C_{par,S2}\Delta V - \int\limits_{switching-ON} i_L(t)dt\right]}_{Energy\ provided\ by\ DC\ source\ to\ the\ half-bridge} + \underbrace{\int\limits_{switching-ON} v_{ds,S2}(t)i_L(t)dt}_{Energy\ provided\ by\ the\ load\ inductor\ to\ the\ half-bridge}$$

$$-\underbrace{\left[E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)\right]}_{Energy\ stored\ by\ output\ capacitance\ of\ S2} - \underbrace{\int\limits_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipated\ in\ S2\ due\ to\ shoot-through} - \underbrace{\frac{1}{2}C_{par,S2}\left[V_{DC}^2 - (V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2}.$$

$$+ \underbrace{E_{oss,S1}(\Delta V) + \frac{1}{2}C_{par,S1}\Delta V^2}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1's\ output\ capacitance\ and\ paralleled\ capacitance}$$

(30)

Notably, (30) is identical to (13), demonstrating that the prediction model derived from energy conservation is fundamentally equivalent to that derived from charge conservation, and establishing the fundamental applicability of both conservation laws in the domain of semiconductor switching behaviors. Complementary perspectives are revealed: energy-conservation-based analytical framework emphasizes the initial and final energy states, whilst charge-conservation-based analytical framework describes the transient charge evolution.

Summary of origin of Miller plateau in switching scenarios

Table 3. Summary of origins of Miller plateau in switching scenarios

Switching scenario	ZVS	HS	Case-1 iZVS	Case-2 iZVS
1st phase	CC	CC	CC	CC
2nd phase	N/A	VF and RR	VF	VF
Miller plateau existence	NO	YES	YES	YES
1st sub-phase of Miller plateau; associated physical origin	N/A	(t_1-t_2); high $C_{oss,S2}$ and low $i_{d,S2}$, causing low dv/dt, thus low $i_{Cgd,S1}$.	(t_1-t_2); high $C_{oss,S2}$ and low $i_{d,S2}$, causing low dv/dt; as $C_{gd,S1}$ is also low, $i_{Cgd,S1}$ is low.	(t_1-t_2); medium-to-low $C_{oss,S2}$ and high $i_{d,S2}$, causing high dv/dt; as $C_{gd,S1}$ is medium-to-high, $i_{Cgd,S1}$ is high.
2nd sub-phase of Miller plateau; associated physical origin	N/A	(t_2-t_3); medium $C_{oss,S2}$ and high $i_{d,S2}$, causing medium dv/dt; given low $C_{gd,S1}$, low-to-medium $i_{Cgd,S1}$ results.	(t_2-t_3); medium $C_{oss,S2}$ and high $i_{d,S2}$, causing medium dv/dt; given low-to-medium $C_{gd,S1}$, low-to-medium $i_{Cgd,S1}$ results.	(t_2-t_3); low $C_{oss,S2}$ and decreasing $i_{d,S2}$, causing high-to-low dv/dt; as $C_{gd,S1}$ is high, $i_{Cgd,S1}$ is high-to-low.
3rd sub-phase of Miller plateau; associated physical origin	N/A	(t_3-t_4); $\lvert dR_{S1}/R_{S1}\rvert > \lvert dv_{ds,S1}/v_{ds,S1}\rvert$ causes decreasing i_{RS1}, and thus a decreasing $i_{d,S2}$, leading to a decreasing dv/dt, whilst $C_{gd,S1}$ increases, causing	(t_3-t_4); medium-to-low $C_{oss,S2}$ and decreasing $i_{d,S2}$, causing decreasing dv/dt; given increasing $C_{gd,S1}$, nearly unchanged $i_{Cgd,S1}$ results.	

		nearly unchanged $i_{Cgd,S1}$ at medium level.	
4th sub-phase of Miller plateau; associated physical origin	N/A	(t_4-t_5); high $C_{gd,S1}$ and medium dv/dt, causing high $i_{Cgd,S1}$.	(t_4-t_6); high $C_{gd,S1}$ and medium dv/dt, causing high $i_{Cgd,S1}$.

Causal-Mechanism Interpretation for Switching Waveforms within a Typical ZVS

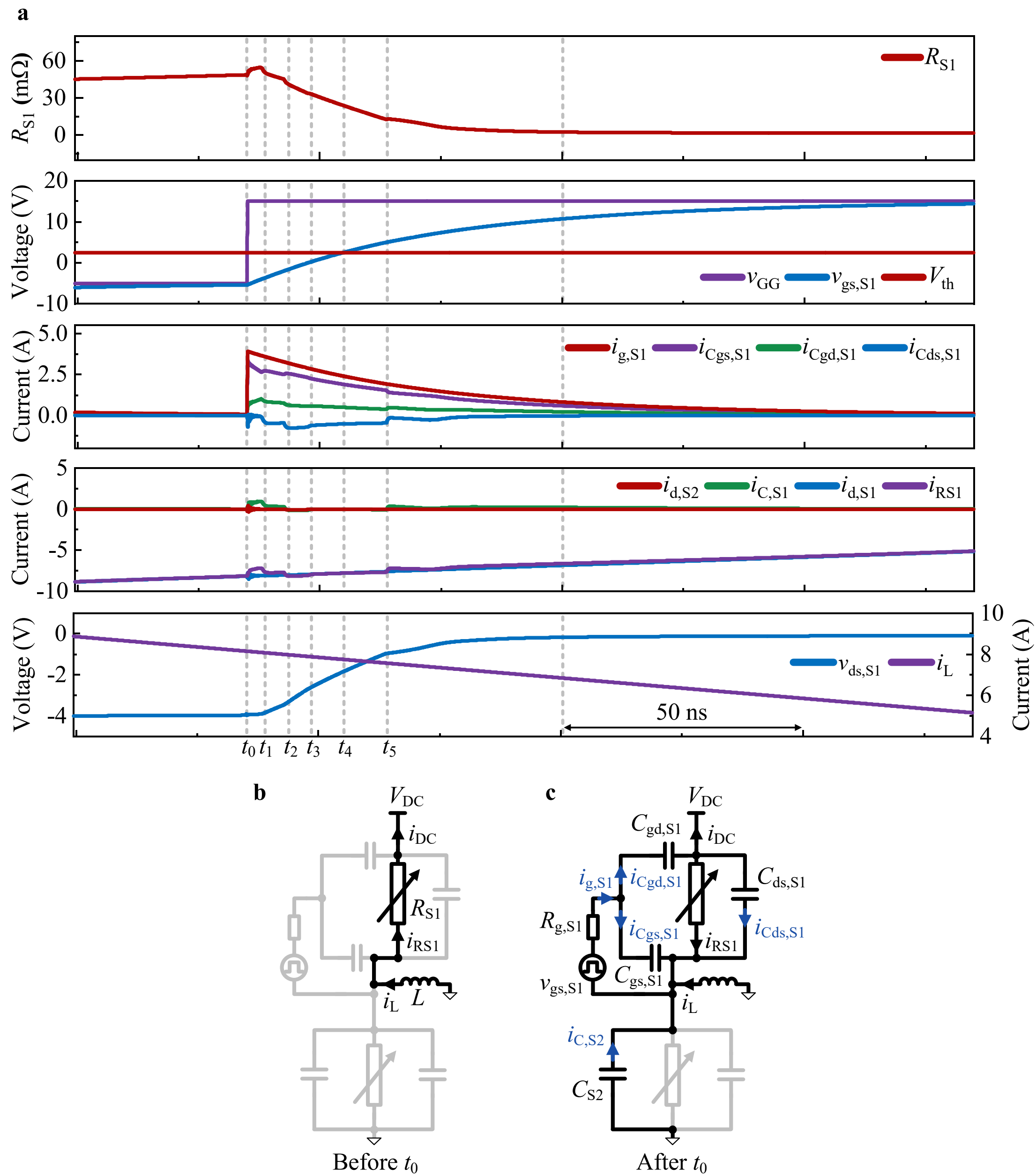


Fig. 5| **Causal-mechanism interpretation for switching waveforms within a typical ZVS. a**, Switching waveforms during a typical ZVS, obtained using LTspice. **b**, Operation mode before t_0. **c**, Operation mode after t_0. The equivalent-circuit model in **b** and **c** is obtained based on **P₁;** the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

Before t_0, i_L is reverse-conducted by R_{S1}. During (t_0-t_1), as $v_{gs,S1}$<–4 V, $v_{gs,S1}$

increase has insignificant influence on R_{S1} (by **P3**); $i_{g,S1}$ charges $C_{gs,S1}$ and discharges $C_{gd,S1}$ simultaneously. Applying KCL at the half-bridge midpoint, yielding $|i_{RS1}|+|i_{Cgd,S1}|=|i_L|+|i_{Cds,S1}|$ (by **P2**; considering influences of other elements including i_L). Since $|i_{Cgd,S1}|>|i_{Cds,S1}|$, $|i_{RS1}|<|i_L|$, explaining the observed drop in $|i_{RS1}|$, which causes a brief rise in R_{S1} (by **P3**). As $C_{ds,S1}$ is high (by **P2**; considering $C_{ds,S1}$'s nonlinearity) and $i_{Cds,S1}$ is low, S_1's *dv/dt* remains low. Consequently, $v_{ds,S1}$ remains nearly constant.

After t_1, as $v_{gs,S1}>-4$ V, the increase in $v_{gs,S1}$ causes R_{S1} to decrease (by **P3**), decreasing $v_{ds,S1}$, thereby promoting both $i_{Cds,S1}$ and $i_{C,S2}$ via R_{S1}. During (t_2-t_3), R_{S1} falls most rapidly per unit rise in $v_{gs,S1}$ (by **P3**), causing the quickest fall in $v_{ds,S1}$ and hence a peak in $i_{Cds,S1}$. During (t_1-t_2) and (t_3-t_5), R_{S1} falls less rapidly (by **P3**), leading to a slower fall in $v_{ds,S1}$ and secondary peaks in $i_{Cds,S1}$. After t_5, increasing $v_{gs,S1}$'s influence on reducing R_{S1} weakens further (by **P3**). As the reduction in R_{S1} flattens (by **P3**), the midpoint voltage drops slightly, with a minor discharge of $C_{oss,S1}$ and C_{S2} via R_{S1}.

Causal-Mechanism Interpretation for Switching Waveforms within Another iZVS Scenario

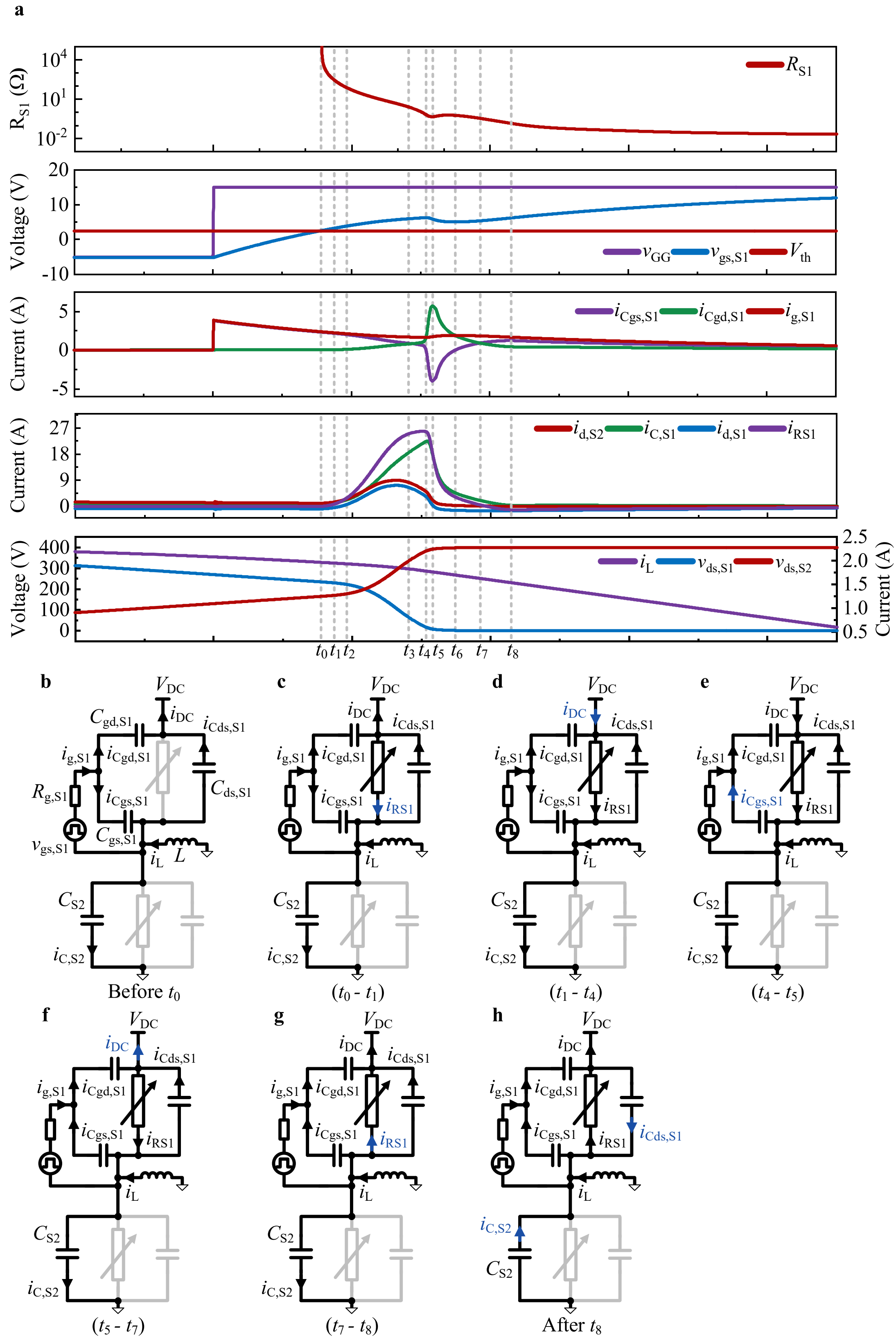


Fig. 6 | **Causal-mechanism interpretation for switching waveforms within another iZVS scenario.**

a, Switching waveforms within another iZVS scenario (i_L flows into the half-bridge midpoint throughout the entire iZVS process). **b**, Operation mode before t_0. **c**, Operation mode during subinterval (t_0-t_1). **d**, Operation mode during subinterval (t_1-t_4). **e**, Operation mode during subinterval (t_4-t_5). **f**, Operation mode during subinterval (t_5-t_7). **g**, Operation mode during subinterval (t_7-t_8). **h**, Operation mode after t_8. The equivalent-circuit model in **b, c**, **d**, **e**, **f**, **g**, and **h** is obtained based on **P_1;** the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

Before t_0 (i.e., the onset of iZVS), i_L discharges C_{S1} and charges C_{S2} simultaneously. During (t_0-t_1), the low $i_{d,S2}$ results in a low S_2's *dv/dt*, despite a relatively low $C_{oss,S2}$ (by **P_2**; considering $C_{oss,S2}$'s nonlinearity; due to the relatively high $v_{ds,S2}$ compared to that in HS). Consequently, only a small portion of $i_{g,S1}$ discharging $C_{gd,S1}$ is required to follow S_2's *dv/dt*, allowing most of $i_{g,S1}$ to charge $C_{gs,S1}$. This leads to a significant increase in $v_{gs,S1}$, sharply reducing R_{S1} (by **P_3**), consequently increasing i_{RS1} significantly. As a result, a lossy CC occurs, where the C_{S1}-conducted share of i_L commutates to C_{S2} (by **P_2**; accounting for influence of i_L). Unlike the near-zero S_2's *dv/dt* in the CC of HS, this CC features a non-zero *dv/dt* that increases with time, due to the increasing i_{CS2} and decreasing $C_{oss,S2}$ (by **P_2**; considering $C_{oss,S2}$'s nonlinearity). At t_1, i_{RS1} exceeds $i_{C,S1}$, indicating the completion of the CC and triggering a reversal of i_{DC}'s direction.

During (t_1-t_2), $i_{RS1}+i_L=i_{d,S2}+i_{C,S1}$ (by **P_2**; considering influences of other elements including i_L). Due to the initially high R_{S1} (by **P_3**), i_{RS1} and thus $i_{d,S2}$ are low. As $v_{gs,S1}$ increases, R_{S1} decreases (by **P_3**), increasing i_{RS1} and consequently increasing $i_{d,S2}$. Combined with the much lower $C_{oss,S2}$, increasing $i_{d,S2}$ leads to a higher S_2's *dv/dt* compared to that in HS. The higher S_2's *dv/dt*, combined with the higher $C_{oss,S1}$ (by **P_2**; considering $C_{oss,S1}$'s nonlinearity), results in a larger $i_{C,S1}$. This, in turn, limits $i_{d,S2}$'s increase, thereby slowing *dv/dt* rise. Consequently, only a small portion of $i_{g,S1}$ is diverted to discharge $C_{gd,S1}$ to follow S_2's *dv/dt*, whilst the majority of $i_{g,S1}$ charges $C_{gs,S1}$.

During (t_2-t_3), the continued increase in i_{RS1} leads to an increase in $i_{d,S2}$, consequently an increase in S_2's *dv/dt*. As negative feedback, more $i_{g,S1}$ is diverted to $C_{gd,S1}$, leading to two consequences: (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, which slows the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction (by **P_3**) and consequently slowing i_{RS1} increase. The slower increase in i_{RS1}, combined with a significant increase in $i_{C,S1}$, reduces the *di/dt* of $i_{d,S2}$ – initially positive in (t_2-t_3), eventually becoming negative before t_3 - limiting increase in S_2's *dv/dt* despite the

decreasing $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity). As a result of these combined effects, $C_{gd,S1}$'s *dv/dt* follows S_2's *dv/dt*.

During (t_3-t_4), the quicker relative reduction in $v_{ds,S1}$ than the relative reduction in R_{S1} (by **P3**), causes a slight decrease in i_{RS1}, contributing to a decreasing $i_{d,S2}$. A significant increase in $C_{gd,S1}$ and $C_{ds,S1}$ causes an increase in $i_{Cgd,S1}$ and $i_{Cds,S1,}$ respectively, and thus the increase in $i_{C,S1}$, also contributing to the decrease in $i_{d,S2}$. Despite a slower relative drop in $C_{oss,S2}$ (by **P2**; considering $C_{oss,S2}$'s nonlinearity), the significant decrease in $i_{d,S2}$ leads to a slight decrease in S_2's *dv/dt* and consequently a slight decrease in S_1's *dv/dt*. Hence, more $i_{g,S1}$ is diverted to discharge $C_{gd,S1}$, further slowing the increase of $v_{gs,S1}$ and thus slowing the reduction in R_{S1} (by **P3**).

During (t_4-t_6), $C_{gd,S1}$ is in its high-capacitance region (by **P2**; considering $C_{gd,S1}$'s nonlinearity), increasing rapidly as $v_{ds,S1}$ decreases; as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low (by **P2**; considering $C_{oss,S2}$'s nonlinearity); as $i_{d,S2}$ remains significant, S_2's *dv/dt* remains significant. Consequently, $C_{gd,S1}$'s *dv/dt* has to remain significant. The insufficient $i_{g,S1}$ to maintain $C_{gd,S1}$'s *dv/dt* to follow S_2's *dv/dt*, triggers further negative feedback – a drop in $v_{gs,S1}$. This boosts $i_{g,S1}$, enhancing $i_{Cgd,S1}$, but also increases R_{S1} (by **P3**), which combined with decreasing $v_{ds,S1}$, leads to a rapid reduction in i_{RS1}, and consequently a decreasing $i_{d,S2}$, thereby a lower *dv/dt*. Meanwhile, $C_{gs,S1}$ supplies a pulse current to help discharge $C_{gd,S1}$ via R_{S1}. Together, these effects enable $C_{gd,S1}$'s *dv/dt* to follow S_2's *dv/dt*. Notably, at t_5, i_{RS1} drops below i_{CS1}, causing a direction reversal of i_{DC}.

During (t_6-t_8), $C_{gs,S1}$ stops supplying charge and is instead charged by $i_{g,S1}$, which supplies charge to both $C_{gs,S1}$ and $C_{gd,S1}$. Notably, the mid-point voltage remains below V_{DC} (by **P2**; considering influence of DC source) before t_7 keeping i_{RS1} positive; after t_7, the mid-point voltage exceeds V_{DC} (by **P2**; considering influence of DC source), reversing I_{RS1}'s direction. Meantime, the C_{S2}-conducted share of i_L gradually commutates to S_1 (by **P2**; considering influence of i_L). At t_8, the current commutation is completed and C_{S2} is fully charged, raising the mid-point voltage to $V_{DC}+R_{S1}(t_8)i_L(t_8)$. After t_8, as $v_{gs,S1}$ further increases, R_{S1} decreases slowly (by **P3**), causing a slight drop in mid-point voltage and consequently a minor discharge of C_{S1} and C_{S2} via R_{S1}.

Data availability

The data presented in this study are available in this manuscript.

Code availability

No custom code was used in this study.

Reference

1 (IEA), I. E. A. Electricity Mid-YearUpdate 2025. (2025).

2 *Future Jobs: Robots, Artificial Intelligence, and Digital Platforms*. (World Bank, 2025).

3 (IEA), I. E. A. Energy and AI *World Energy Outlook Special Report* **International Energy Agency (IEA)**.

4 Measuring the Emissions & Energy Footprint of the ICT Sector:Implications for Climate Action. *World Bank* (2024).

5 Huang, Z., Yang, T., Giangrande, P., Galea, M. & Wheeler, P. Technical Review of Dual Inverter Topologies for More Electric Aircraft Applications. *IEEE Transactions on Transportation Electrification* **8**, 1966-1980, doi:10.1109/TTE.2021.3113606 (2022).

6 Global EV Outlook 2025. *International Energy Agency (IEA)* (2025).

7 The Future of Heat Pumps. *International Energy Agency (IEA)* (2022).

8 (IEA), I. E. A. Global Hydrogen Review 2024.

9 Bardeen, J. B., W. H. The Transistor, A Semi-Conductor Triode. *Physical Review* (1947).

10 Nilsson, J. W. R., Susan A. *Electric Circuits*. (Pearson).

11 Cheema, S. S. *et al.* Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors. *Nature* **604**, 65-71, doi:10.1038/s41586-022-04425-6 (2022).

12 Kang, H. & Udrea, F. True Material Limit of Power Devices—Applied to 2-D Superjunction MOSFET. *IEEE Transactions on Electron Devices* **65**, 1432-1439, doi:10.1109/TED.2018.2808181 (2018).

13 Si, M. *et al.* A ferroelectric semiconductor field-effect transistor. *Nature Electronics* **2**, 580-586, doi:10.1038/s41928-019-0338-7 (2019).

14 He, Q. *et al.* Numerical Simulation and Analytical Modeling of Multichannel AlGaN/GaN Devices. *IEEE Transactions on Electron Devices* **71**, 1710-1717, doi:10.1109/TED.2024.3359165 (2024).

15 Janabi, A. *et al.* Substrate Embedded Power Electronics Packaging for Silicon Carbide mosfets. *IEEE Transactions on Power Electronics* **39**, 9614-9628, doi:10.1109/TPEL.2024.3396779 (2024).

16 Mu, W., Janabi, A., Hu, B., Shillaber, L. & Long, T. Liquid Metal Fluidic Connection and Floating Die Structure for Ultralow Thermomechanical Stress of SiC Power Electronics Packaging. *IEEE Transactions on Power Electronics* **39**, 7808-7814, doi:10.1109/TPEL.2024.3379121 (2024).

17 Zhang, Y. *et al.* Power Cycling Testing for Power Semiconductor Switches: Methods, Standards, Limitations, and Outlooks. *IEEE Transactions on Power Electronics*, 1-21, doi:10.1109/TPEL.2025.3595180 (2025).

18 Xu, C. *et al.* Full-Time Junction Temperature Extraction of IGCT Based on Electrothermal Model and TSEP Method for High-Power Applications. *IEEE Transactions on Industrial Electronics* **68**, 47-58, doi:10.1109/TIE.2019.2962423 (2021).

19 van Erp, R., Soleimanzadeh, R., Nela, L., Kampitsis, G. & Matioli, E. Co-designing electronics with microfluidics for more sustainable cooling. *Nature* **585**, 211-216, doi:10.1038/s41586-

020-2666-1 (2020).

20 Wang, H., Zhu, R., Wang, H., Liserre, M. & Blaabjerg, F. A Thermal Modeling Method Considering Ambient Temperature Dynamics. *IEEE Transactions on Power Electronics* **35**, 6-9, doi:10.1109/TPEL.2019.2924723 (2020).

21 Cao, W. *et al.* The future transistors. *Nature* **620**, 501-515, doi:10.1038/s41586-023-06145-x (2023).

22 Rezaei, M., Esteghamat, A. & Matioli, E. Terahertz Electronic Metadevices: Principles Behind the Ultra-High Cutoff Frequency. *IEEE Electron Device Letters* **46**, 1986-1989, doi:10.1109/LED.2025.3606749 (2025).

23 Agile Delivery of Electrical Power Technology. *U.S. Department of Energy* (2010).

24 Ying, W. *et al.* Towards the True Zero-Voltage-Switching Boundary. *IEEE Transactions on Power Electronics*, 1-6, doi:10.1109/TPEL.2025.3592857 (2025).

25 Kolar, J. W. *et al.* in *2007 Power Conversion Conference - Nagoya.* P-9-P-29.

26 Baliga, B. J. *Fundamentals of Power Semiconductor Devices*. (Springer, 2008).

27 Robert W. Erickson, D. M. *Fundamentals of Power Electronics*. (Springer New York, NY).

28 Mohan, N., Undeland, T. M. & Robbins, W. P. *Power Electronics: Converters, Applications, and Design*. (John Wiley & Sons, 2003).

29 Horowitz, P. & Hill, W. *The Art of Electronics*. (Cambridge University Press, 2015).

30 Powell, E. I. R. G. in *Introduction to Electric Circuits* (ed Eur Ing R. G. Powell) 10-39 (Butterworth-Heinemann, 1995).

31 Brown, D. W. *et al.* Turn-Off Time as an Early Indicator of Insulated Gate Bipolar Transistor Latch-up. *IEEE Transactions on Power Electronics* **27**, 479-489, doi:10.1109/TPEL.2011.2159848 (2012).

32 Chen, K., Zhao, Z., Yuan, L., Lu, T. & He, F. The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET. *IEEE Transactions on Electron Devices* **62**, 333-338, doi:10.1109/TED.2014.2362657 (2015).

33 Wang, L. *et al.* A Brief Review of SiC MOSFET Transient Analytical Modeling Methods: Principles, Current Status, and Parameters Modeling. *IEEE Transactions on Power Electronics* **40**, 5177-5189, doi:10.1109/TPEL.2024.3439364 (2025).

34 Li, X. *et al.* A SiC Power MOSFET Loss Model Suitable for High-Frequency Applications. *IEEE Transactions on Industrial Electronics* **64**, 8268-8276, doi:10.1109/TIE.2017.2703910 (2017).

35 Zhang, Z. *et al.* Methodology for Wide Band-Gap Device Dynamic Characterization. *IEEE Transactions on Power Electronics* **32**, 9307-9318, doi:10.1109/TPEL.2017.2655491 (2017).

36 Zhang, Z., Guo, B. & Wang, F. Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices. *IEEE Transactions on Power Electronics* **34**, 9082-9094, doi:10.1109/TPEL.2018.2883454 (2019).

37 Ahmed, M. R., Todd, R. & Forsyth, A. J. Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions. *IEEE Transactions on Industrial Electronics* **64**, 9001-9011, doi:10.1109/TIE.2017.2721882 (2017).

38 Wu, Y., Wang, L., Wang, J., Shi, Z. & Zhang, J. Comparison and Optimization of Datasheet-Driven Extraction of Gate-Drain Overlap Oxide Capacitance in IGBT Modeling. *IEEE Transactions on Power Electronics* **37**, 14023-14027, doi:10.1109/TPEL.2022.3194023 (2022).

39 IEC 60747-9: Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors. *International Electrotechnical Commission (IEC)*.

40 IEC 60747-8: Semiconductor devices – Discrete devices – Part 8: Field-effect transistors. *International Electrotechnical Commission (IEC)*.

41 Perera, N. *et al.* Hard-Switching Losses in Power FETs: The Role of Output Capacitance. *IEEE Transactions on Power Electronics* **37**, 7604-7616, doi:10.1109/TPEL.2021.3130831 (2022).

42 Kasper, M., Burkart, R. M., Deboy, G. & Kolar, J. W. ZVS of Power MOSFETs Revisited. *IEEE Transactions on Power Electronics* **31**, 8063-8067, doi:10.1109/TPEL.2016.2574998 (2016).

43 Shelton, E., Rogers, D. & Palmer, P. in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe).* 1-10.

44 Burroughes, J. H., Jones, C. A. & Friend, R. H. New semiconductor device physics in polymer diodes and transistors. *Nature* **335**, 137-141, doi:10.1038/335137a0 (1988).

45 Baliga, B. J. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters* **10**, 455-457, doi:10.1109/55.43098 (1989).

46 Li, X. *et al.* Achieving Zero Switching Loss in Silicon Carbide MOSFET. *IEEE Transactions on Power Electronics* **34**, 12193-12199, doi:10.1109/TPEL.2019.2906352 (2019).

47 Jafari, A. *et al.* Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies. *IEEE Transactions on Power Electronics* **35**, 12595-12600, doi:10.1109/TPEL.2020.2990628 (2020).

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Competing Interests Statement

The authors declare no competing interests.

Supplementary Information

N/A