

Charge-Unified Semiconductor Switching Theory

Abstract

Semiconductors and downstream applications sustain the electronic, information, energy and industrial systems underpinning society. Their sustainability is an urgent global priority, particularly as global electricity generation is projected to rise more than 2.5-fold by 2050¹. However, since 1947², a unified, global view of circuit elements as media for charge redistribution and transfer, which reveals switching inertia and dynamical nature of switching, and connects microscopic and macroscopic domains across semiconductor value chain within a unified theoretical language has yet to be established^{3,4}; switching lacks a unified mechanistic account of its physical origins and spatiotemporal evolution⁵⁻¹², without fundamental unifications between charge- and energy-conservation frameworks, across carrier dynamics and across equivalent-circuit formalisms^{5-7,10-19}. These limitations fragment the domains and impede sustainability gains, particularly those requiring cross-domain causal information. Here we present Charge-Unified Semiconductor Switching Theory (CUSST), a general theory that unifies circuit elements through a charge-mediated view, reveals inertia and the dynamical nature of switching, achieves aforementioned long-missing unifications, and establishes a unified formulation across conceptual, mechanistic, formal and analytical levels, with unprecedented simplicity through unifications. CUSST establishes a unified micro–macro spatiotemporal view of switching, generalizes circuit theory, extends conservation laws and guides theoretical systems. For example, a CUSST-based switching-energy-loss model (errors: 0.88–11.60%) achieves a 17-fold average error reduction compared to the conventional model (errors: 34.41–80.05%); CUSST enables unprecedented causal–mechanistic interpretability to reveal the underlying switching dynamics across scenarios. More broadly, CUSST may support domains along the semiconductor value chain, such as semiconductor materials²⁰, chip design²¹, packaging²², reliability^{23,24}, thermal engineering^{25,26} and downstream applications such as power electronics and potentially extend to broader systems such as computing, communications and integrated circuits.^{27,28} By offering cross-domain causal

information, CUSST could advance these fragmented domains towards a unified discipline including through enabling full-chain causal feedback and cross-domain co-design and research, and unlock sustainability gains beyond individual-domain optimization.

Keyword: semiconductor switching, cross-domain integrated research, co-design, unified discipline, semiconductor value chain

Nomenclature

Table 1| NOMENCLATURE

Symbol	Unit	Definition
S_x	N/A	Switch index, e.g., S_1 denotes the upper switch and S_2 denotes the lower switch.
R_{Sx}	Ω	Equivalent resistance of S_x .
$v_{ds,Sx}$	V	Drain-source voltage of S_x .
v_{GG}	V	Output voltage of the gate driver of S_1 .
$v_{gs,Sx}$	V	Gate-source voltage of S_x .
$V_{th,Sx}$	V	Threshold voltage of S_x .
V_{gp}	V	Gate-source voltage at the Miller plateau (assumed constant)
$C_{oss,Sx}$	pF	Output capacitance of S_x .
C_{Sx}	pF	Overall equivalent capacitance of S_x .
$C_{gs,Sx}$	pF	Gate-source capacitance of S_x .
$C_{gd,Sx}$	pF	Gate-drain capacitance (also known as Miller capacitance) of S_x .
$C_{ds,Sx}$	pF	Drain-source capacitance of S_x .
C_x	pF	A generic linear or nonlinear capacitance.
$i_{d,Sx}$	A	The drain current of S_x .
$i_{d,Sx}$	A	The channel current of S_x .
$i_{g,Sx}$	A	Gate driving current of S_x .
i_L	A	Load current.
i_{RSx}	A	Instantaneous current through R_{Sx} .
i_{DC}	A	DC-source current.
$i_{Cgs,Sx}$	A	Displacement current of $C_{gs,Sx}$.
$i_{Cgd,Sx}$	A	Displacement current of $C_{gd,Sx}$.
$i_{Cds,Sx}$	A	Displacement current of $C_{ds,Sx}$.
$i_{C,Sx}$	A	Displacement current of C_{Sx} .
i_{RSx}	A	Conductive current through the equivalent capacitance R_{Sx} .
i_{inj}	A	Injection current.
i_{ext}	A	Extraction current.
i_{rec}	A	Equivalent recombination current.
V_{DC}	V	DC-link voltage.
E_{on}	μJ	The turn-on energy dissipation.
$E_{gd,Sx}(v)$	μJ	The energy stored in $C_{gd,Sx}$ at drain-gate voltage of v .
$E_{ds,Sx}(v)$	μJ	The energy stored in $C_{ds,Sx}$ at drain-source voltage of v .
$E_{oss,Sx}(v)$	μJ	The energy stored in the output capacitance of S_x at drain-source voltage of v .
$Q_{oss,Sx}(v)$	nC	The charge stored in the output capacitance of S_x at drain-source voltage of v .
$Q_x(v)$	nC	The charge stored in a generic capacitance at drain-source voltage of v .
ΔQ_x	nC	The change in stored charge.
$e_{CUSST-based}$	N/A	Error of the CUSST-based model's prediction results w.r.t. the measured results.
e_{con}	N/A	Error of the conventional model's prediction results w.r.t. the measured results.
HS	N/A	Hard switching; turn-on without prior v_{ds} discharge.
iZVS	N/A	Incomplete zero-voltage switching; turn-on with partial v_{ds} discharge and residual v_{ds} .
ZVS	N/A	Zero-voltage switching; turn-on after v_{ds} is discharged to approximately zero.
CC	N/A	Current-commutation process
VF	N/A	Voltage-fall process

Introduction

The International Energy Agency and World Bank project that AI and robotics-driven intelligentization^{29,30}, transport electrification³¹, heat pumps³², hydrogen production³³, digitalization³⁰ and advanced manufacturing²⁹ are driving unprecedented electricity demands, with global generation exceeding 2.5 times today’s level by 2050¹. Greener semiconductors downstream applications are therefore an increasingly urgent priority for global sustainability. By 2030, power electronics, a subfield of electrical engineering is projected to process over 80% of US electricity,³⁴ while global data centres could emit 399 million tonnes of CO₂ and consume 9.3 trillion litres of water annually—enough to meet the domestic water needs of 1.3 billion people in sub-Saharan Africa³⁵. Yet semiconductor losses remain a major source of energy inefficiency and water-cooling demand. For example, in AI data centres, power-electronics losses can reach about 12% of total facility power³⁶, with semiconductor loss forming a major contribution, while graphics processing units (GPUs) can account for a further 40% of total facility power³⁷. By 2030, the annual footprint of data centres could approach 945 TWh—about 16.3 times Switzerland’s current electricity use^{38,39}.

However, despite its key role in semiconductor losses, electromagnetic interference (EMI) and other nonidealities that govern the sustainability of electrical and electronic systems^{17,18,40}, semiconductor switching has for decades lacked a unified formulation across conceptual, mechanistic, formal and analytical levels. Conceptually, the charge-mediated nature of circuit elements, particularly semiconductor devices, has yet to be elucidated within a unified, global framework^{3,4}; conventional circuit theory lacks insights on carrier dynamics and conductive-path evolution in semiconductors and lacks a unified, physics-based definition of turn-on onset (detailed in *Methods*). Mechanistically, unification of macro- and microscopic insights through switching inertia and interactions is absent; a unified mechanistic account of the physical origins of the spatiotemporal evolution of semiconductor switching remains lacking, with the causal pathways linking input interactions to output responses unresolved, despite substantial efforts to reproduce observed switching waveforms or their linearized approximations.⁵⁻¹² For example, the conventional E_{on} model properly accounts for the

DC source and output capacitances of both half-bridge devices under iZVS,¹⁴ but not the load current or associated energy dissipation, which leads to prediction errors of 34.41–80.05%. For another example, although the so-called Miller plateau, its abrupt drop (here termed Inertia plateau and Inertia drop, respectively within CUSST) and their absence under ZVS have been widely reported^{5,6,10-12}, their common origin remains obscured by the unrecognized switching inertia and interactions between devices, despite their potentially substantial contributions to system losses, EMI and nonlinearity. In addition, intra-device carrier recovery under ZVS (here termed ZVS recovery) has yet to be revealed, leaving recoveries across switching scenarios unrecognized as different manifestations of the same underlying carrier dynamics and fundamentally ununified. Formally, existing representations remain fragmented. Many of them⁵⁻⁷ represent the semiconductor device as a two- or three-terminal block; more advanced representations^{12,15,16} add junction capacitances to capture dielectric phenomena; some further employ complex, non-unified representations, modelling the conductive path with waveform-fitted current or voltage sources that vary across scenarios and subintervals^{11,17-19}. Analytically, energy and charge conservation arise from distinct fundamental symmetries: time-translation symmetry through Noether’s theorem and electromagnetic gauge symmetry, respectively, with charge conservation expressed in circuit theory through Kirchhoff’s current law (KCL). The two frameworks remain separate, and their applicability to switching dynamics has not been established.

Substantial efforts have demonstrated that cross-domain research and co-design can achieve gains beyond individual-domain optimization, including a 50-fold increase in cooling coefficient of performance via electronics-thermal co-design²⁶, a 15.8-fold enhancement in thermal conductivity via materials–thermal–packaging–application co-design⁴¹, and a twofold increase in energy efficiency via device–circuit–architecture–algorithm research⁴². However, the absence of underpinning theoretical foundations impedes unlocking the full potential of such cross-domain research and co-design along the semiconductor value chain, by obscuring causal links and leaving no unified theoretical language. For example, conventional device-level figure-of-merit (FOM)

optimization^{43,44} does not reliably improve application-level performance. Although this limitation has been recognized^{45,46}, mechanistic understanding of switching dynamics remains unresolved, leaving device-to-application causal pathways obscured. As switching heat can be highly localized in space and time—within die regions and switching subintervals orders of magnitude smaller than the full die area and switching period, respectively—average junction-temperature estimates may mask much higher local temperature peaks (Fig. 1b).⁴⁷ More broadly, limited understanding of how switching dynamics translate into electrothermal stress and degradation drives reliance on average thermal metrics, empirical derating and conservative margins, leading to material-intensive overdesign while obscuring spatiotemporally localized temperature peaks that may define the true reliability limit.⁴⁸⁻⁵⁰

Here we introduce Charge-Unified Semiconductor Switching Theory (CUSST), which establishes a unified formulation across conceptual, mechanistic, formal and analytical levels (Fig. 1). Conceptually, CUSST reveals the physical nature of circuit elements, including semiconductor devices, as physical media for charge redistribution and transfer, unifying macro- and microscopic physical pictures. Mechanistically, CUSST reveals switching inertia, its physical origins, and the dynamical nature of switching. As demonstrated in the following representative switching examples, CUSST identifies the Inertia plateau and Inertia drop—and their absence under ZVS—as distinct manifestations of capacitive-charge inertia governed by the same underlying dynamics. It further reveals the physical unity of carrier dynamics across switching scenarios and identifies carrier inertia—namely, the finite-time response of the stored-carrier distribution—as the common origin of carrier-recovery phenomena across scenarios. Formally, CUSST-enabled insights are expressed in a representative equivalent-circuit formalism that unifies macro- and microscopic physical pictures. It may serve as a semiconductor counterpart to the standard transformer equivalent-circuit^{6,51}, in principle generalizable across circuits, devices, scenarios and subintervals. Analytically, CUSST generalizes circuit theory with a charge-unified view, encompassing charge-storage mechanisms and conductive-path resistance in semiconductors. It further unifies charge- and energy-conservation frameworks,

establishing their equivalent applicability to switching dynamics. As a result, CUSST enables four fundamental unifications: across charge-storage mechanisms (detailed in Table 3); across charge- and energy-conservation frameworks; across macro- and microscopic insights; and through a unified equivalent-circuit formalism in principle universally applicable across devices, circuits, scenarios and subintervals. These unifications offer unprecedented conceptual, formal and analytical simplicity, immediate practical utility and broader generality, while retaining compatibility with existing theories.

After establishing CUSST, we found that CUSST yielded a new CUSST-based E_{on} model, with a 17-fold prediction accuracy improvement over the conventional model¹⁴ (Fig. 2 and Table 2); CUSST also revealed underlying causal mechanisms and dynamical nature of switching across representative scenarios, including HS and ZVS cases (Fig. 3 and Fig. 4), together with a representative iZVS and an additional iZVS case presented in *Methods*. Beyond these demonstrated implications, as further discussed in the *Discussion and Outlook*, CUSST formulates the theoretical foundations of a unified system for modelling, design, optimization and standardization across semiconductor science, engineering and downstream applications; CUSST further paves the way for unifying these disparate domains into a unified discipline. For example, by revealing cross-domain causal information, CUSST could enable full-chain causal feedback, cross-domain integrated research and co-design across the semiconductor value chain, unlocking new levels of device- and system-level sustainable performance. A related ZVS study¹³ illustrates this potential: by revealing previously unresolved interactions such as opposite-device channel current during turn-off before ZVS—it achieved an approximately 60-fold improvement in average modelling accuracy over prior-art methods, now underpinning ongoing international standardization⁵² and advancing the domains across the semiconductor value chain by offering a key piece of causal information.

To our knowledge, CUSST establishes the first unified, global, micro–macro spatiotemporal view of switching throughout the multiscale system and across timescales, moving beyond local, fragmented and domain-isolated descriptions. By

offering a unified theoretical language across the semiconductor value chain and cross-domain causal information, CUSST paves the way towards a unified discipline spanning the semiconductor value chain.

CUSST concept

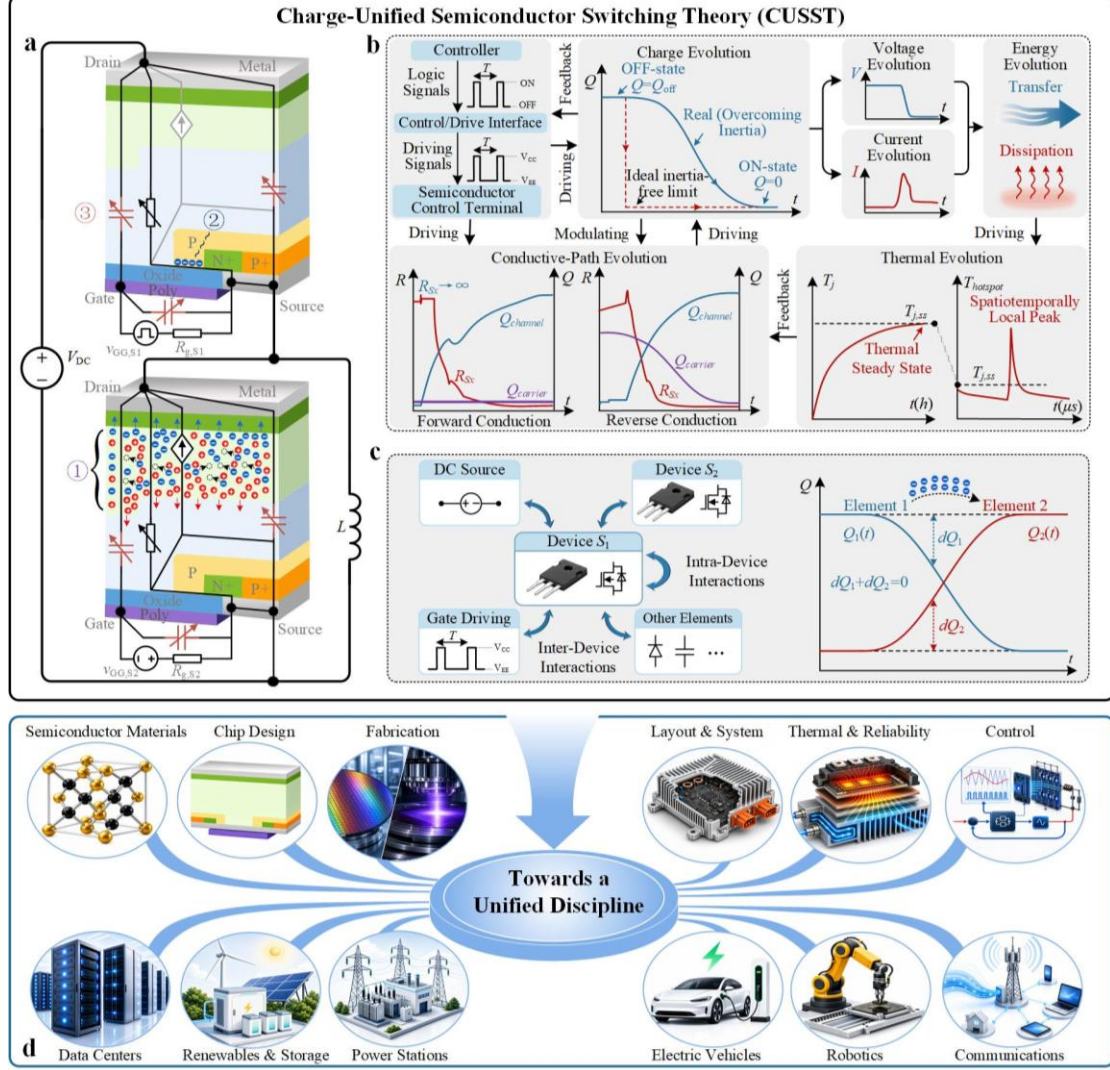


Fig. 1| CUSST concept: a unified, global, micro–macro spatiotemporal theory and one key implication: paving the way towards a unified discipline spanning the semiconductor value chain. **a**, Illustration of Switching Inertia Principle (P₁) using a MOSFET-based half-bridge, linking microscopic device structure and spatiotemporal charge evolution to the corresponding macroscopic equivalent-circuit formalism. **b**, Illustration of the Dynamical Evolution Principle (P₂) through the coupled evolution of charge, voltage, current, energy, conduction paths, and average junction and hotspot temperatures, with hotspot-temperature peaks localized to areas and intervals that can be orders of magnitude smaller than the die area and switching period, respectively. **c**, Illustration of Interaction Reciprocity Principle (P₃). **d**, One key implication of CUSST: formulating theoretical foundations for connecting the full semiconductor value chain—from upstream materials, chip design and fabrication to downstream circuit layout and system design, thermal management, reliability and control—across application domains, with examples shown here.

CUSST comprises three principles: Switching Inertia Principle, Dynamical Evolution Principle and Interaction Reciprocity Principle. While Fig. 1 shows a MOSFET-based half-bridge with a load inductor as a representative example, the theory is expected to generalize through the underlying switching dynamics, rather than being limited to a specific topology, device type, switching scenario or subinterval.

1st Principle (P₁)—Switching Inertia Principle: CUSST reveals a charge-unified view that identifies circuit elements, in their physical nature, as media for charge redistribution and transfer, thereby offering a unified conceptual foundation between microscopic semiconductor mechanisms and macroscopic circuit behavior. Particularly, semiconductor devices are identified as distributed charge-storing media whose internal charge distributions and dissipative conduction paths undergo a coupled spatiotemporal evolution between insulator-like blocking and conductor-like current-conducting states. Driven by relevant interactions, the underlying charge evolution manifests macroscopically as continuous voltage–current, energy and thermal evolutions; the equivalent resistance of the conduction path is governed by gate-induced charge and carrier-storage charge.

As detailed in the *Methods* section on the representative equivalent-circuit formalism, the MOSFET is formalized by a representative equivalent circuit^{7,8,53}. This formalism comprises a lumped variable resistor (e.g., R_{S1} and R_{S2}), lumped variable capacitors (e.g., $C_{oss,S1}$ and $C_{oss,S2}$) as well as a lumped current source to formalize the conductivity modulation mechanisms. As a semiconductor counterpart to the standard transformers equivalent-circuit formalism^{6,51}, this representative formalism captures switching dynamics across scenarios and subintervals for the MOSFET and is in principle generalizable across devices and circuits.

During switching, the conductive path evolves between high- and low-resistance states, accompanied by the spatiotemporal evolution of charge and energy in capacitive elements and carrier-storage regions. At any instant, these resistive, capacitive and carrier-storage states characterize the switching state. Such charge and energy storage gives rise to two forms of intrinsic switching inertia: capacitive-charge inertia and carrier inertia, both requiring finite-time charge and energy evolution and thus

precluding the discontinuous state transitions permitted in the ideal inertia-free limit.

2nd Principle (P₂)—Dynamical Evolution Principle: CUSST reveals the dynamical nature of semiconductor switching: stored charges act as momentum-like state variables, while transferred charge acts as an impulse-like quantity. The dimensional correspondence also reflects this shared dynamical nature between mechanics and state evolution of circuit elements.

As demonstrated in Fig.1, the gate current acts as an external gate-driving interaction, analogous to an external force in classical dynamics, while R_{S1} serves as a key switching-state variable to represent the conductive-path evolution. By overcoming switching inertia, this interaction initiates the variation of R_{S1} , establishing a causal chain from conductive-path evolution to charge, voltage–current, energy and thermal evolution. Integrating micro–macro spatiotemporal physical pictures, this dynamical evolution is governed by CUSST’s charge-unified framework and conservation laws, while being constrained by the R_{S1} characteristic, nonlinear capacitance characteristics and carrier dynamics, as demonstrated in the “Causal-Mechanistic Interpretations of Switching Dynamics” and relevant *Methods* sections.

3rd Principle (P₃)—Interaction Reciprocity Principle: No charge evolution is one-sided: universally across circuits, devices, scenarios and subintervals, charge evolution in one element or charge-storage region are accompanied by coupled responses in other element(s) and associated energy evolution under charge and energy conservation. Accordingly, a complete representation of switching dynamics requires all non-negligible interactions to be incorporated; omitting any relevant interaction yields only partial dynamics. Parasitic inductances are omitted from the formulation, as justified in *Methods*.

Unified formulation of semiconductor switching dynamics from charge and energy conservation laws and experimental validation

Within CUSST, an CUSST-based E_{on} model is derived in a representative iZVS scenario, independently from charge and energy conservation (detailed in *Methods*). Considering the same physical interactions, the analytical frameworks based on energy conservation and charge conservation converge to identical analytical expressions, thereby establishing their fundamental equivalence in semiconductor switching.

We further validate the CUSST-based model against experimental measurements and compare it with the conventional model¹⁴. The overall data comparison is visualized in Fig. 2, while the error-reduction factor is quantified for each condition in Table 2. Averaging these error-reduction factors across all conditions gives a 17-fold average error reduction relative to the conventional model¹⁴. This agreement with experimental measurements validates the equivalent applicability of the two analytical frameworks to semiconductor switching and supports the deterministic predictive capability of CUSST. These results further confirm CUSST's compatibility with charge and energy conservation laws, extending their applicability to semiconductor devices.

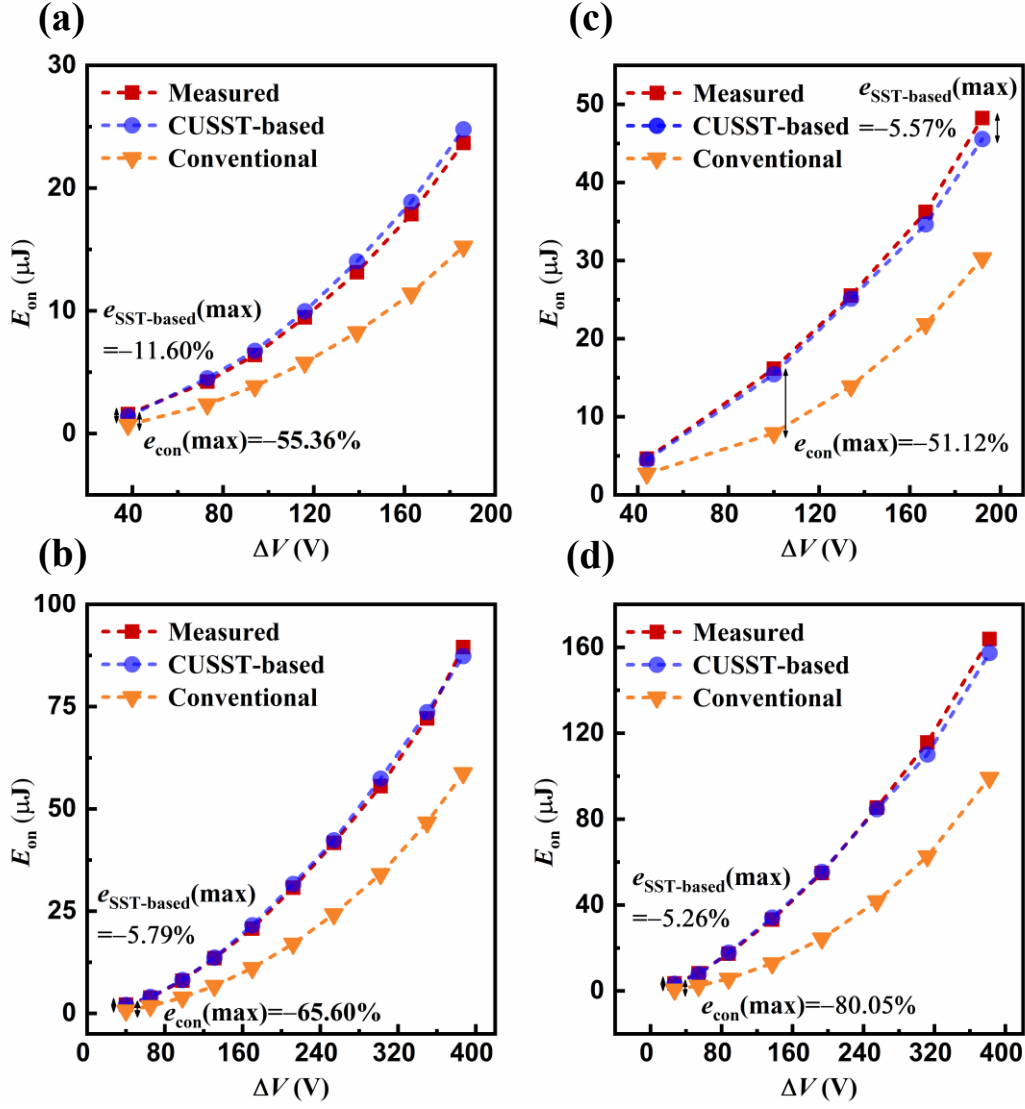


Fig. 2| Comparison of measured results (red) with calculated results from the CUSST-based model (blue) and the conventional model (orange) at room temperature. Measurements were performed using commercially available semiconductor devices. Results are shown for (a) $V_{DC}=200$ V with semiconductor device A⁵⁴; (b) $V_{DC}=400$ V with semiconductor device A⁵⁴; (c) $V_{DC}=200$ V with semiconductor device B⁵⁵ and (d) $V_{DC}=400$ V with semiconductor device B⁵⁵.

Revealing causal mechanisms and the dynamical nature of representative HS through CUSST-enabled causal-mechanistic interpretability

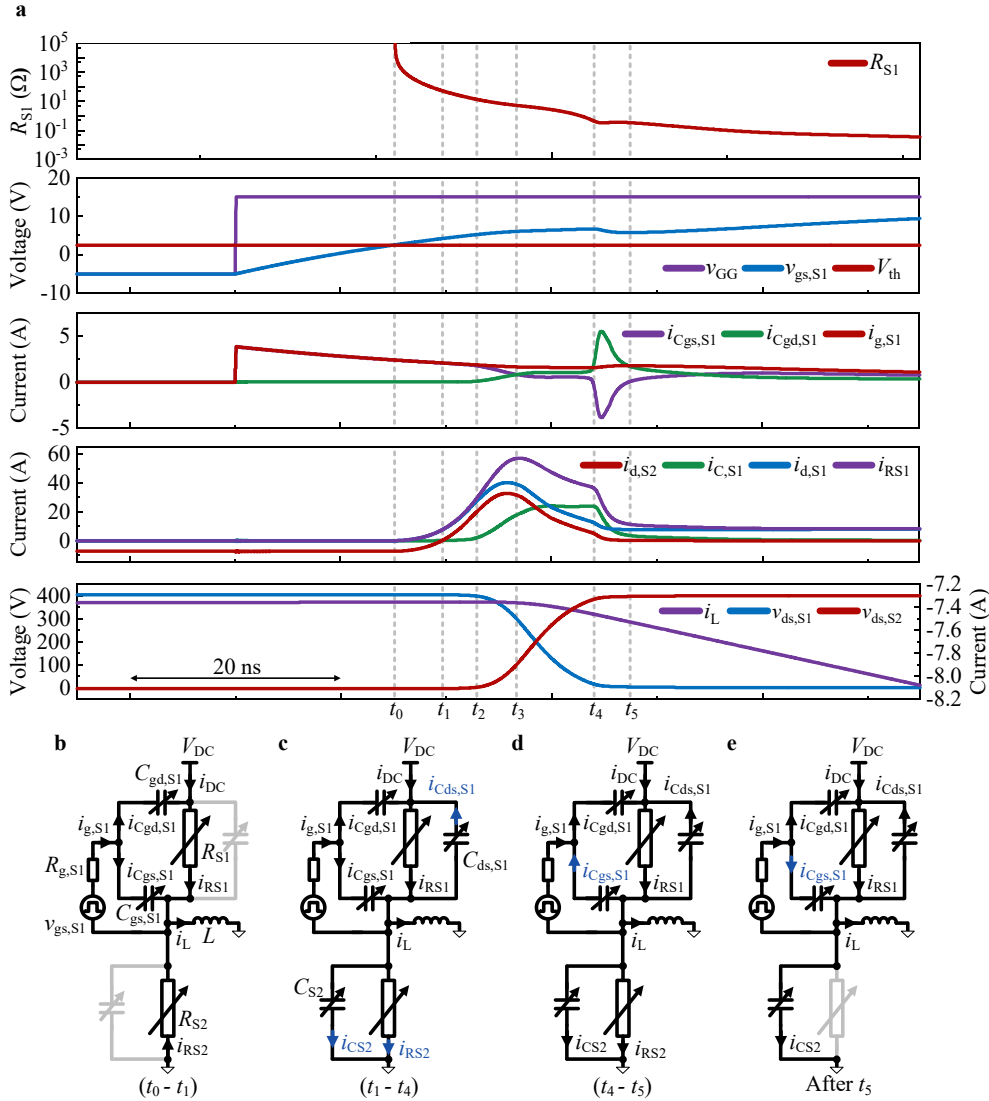


Fig. 3 | Revealing causal mechanisms and the dynamical nature of representative hard switching through CUSST-enabled causal-mechanistic interpretability **a**, switching waveforms within a representative HS. **b**, Operation mode during subinterval $(t_0 - t_1)$. **c**, Operation mode during subinterval $(t_1 - t_4)$. **d**, Operation mode during subinterval $(t_4 - t_5)$. **e**, Operation mode after t_5 . The equivalent-circuit formalism is obtained based on $\mathbf{P}_1$; the highlighted branches in **b-e** indicate the current paths; the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

At t_0 (the onset of HS), i_L is reverse-conducted by R_{S2} . During $[t_0 - t_1]$, while $v_{ds,S1}$ remains nearly constant, $v_{gs,S1}$ increases and R_{S1} therefore decreases rapidly accordingly; hence, i_{RS1} increases ($\mathbf{P}_2$). As a result, a lossy CC occurs, in which i_L gradually commutates from R_{S2} to R_{S1} , more specifically, from S_2 's diode to S_1 's channel ($\mathbf{P}_3$). As S_2 's diode current decreases, the reduced forward bias across the P-body/N-drift

junction raises the effective barrier and suppresses hole injection into the conductivity-modulated drift region. Owing to carrier inertia described by **P1**, the drift region initially retains the distribution established at the preceding higher-diode-current state. The hole concentration therefore falls more rapidly near the depletion-region boundary than deeper within the drift region, creating a gradient that drives stored holes toward the junction. These holes are then swept by the depletion-region electric field back into the P-body and source, which contributes to the carrier recovery current, namely $i_{\text{car},S2}$.

At t_1 , i_L is fully commutated to R_{S1} , which marks the end of CC and the onset of VF. After t_1 , as i_{RS1} increases, $i_{d,S2}$ reverses and rises (**P3**), where dv/dt is given by $|dv_{ds,S2}/dt| = |i_{d,S2} - i_{\text{car},S2}| / C_{\text{oss},S2}$, while the carrier recovery continues.

During $[t_1-t_2]$, $C_{\text{oss},S1}$ is discharged and $C_{\text{oss},S2}$ is charged via R_{S1} . Because of voltage-dependent nonlinearity, $C_{\text{oss},S2}$ is orders of magnitude larger than $C_{\text{oss},S1}$, despite the same dv/dt , and hence i_{C2} is significantly larger than i_{C1} . Meanwhile, only a small fraction of $i_{g,S1}$ is required by $C_{gd,S1}$ to follow S_2 's dv/dt ; consequently, most of $i_{g,S1}$ charges $C_{gs,S1}$ (**P3**). At t_2 , $v_{ds,S2}$ crosses zero; after t_2 , the PN junction is reverse-biased, which causes depletion-region expansion and deeper carrier removal from the conductivity-modulated drift region.

During $[t_2-t_3]$, a quicker relative drop in R_{S1} than in $v_{ds,S1}$ (i.e., $|dR_{S1}/R_{S1}| > |dv_{ds,S1}/v_{ds,S1}|$) causes a continued increase in i_{RS1} , which in turn increases $i_{d,S2}$; meanwhile, as $v_{gs,S1}$ increases, $|dR_{S1}/R_{S1}|$ decreases, which further leads to a reduced di/dt of i_{RS1} , which turns negative at t_3 (**P2**, **P3**).

During $[t_3-t_4]$, $C_{\text{oss},S1}$ and $C_{\text{oss},S2}$ transition into their high- and low-capacitance regions, respectively. As a result, $i_{Cds,S1}$ rises; meanwhile, a feedback mechanism arises through coupled charge redistribution (**P3**) to overcome the capacitive-charge inertia (**P1**), owing to an increased charge demand of $C_{gd,S1}$: most of $i_{g,S1}$ is diverted from $C_{gs,S1}$ to $C_{gd,S1}$ (**P3**). This leads to: (1) higher $i_{Cgd,S1}$, which increases $C_{gd,S1}$'s dv/dt ; and (2) lower $i_{Cgs,S1}$, which slows the rise of $v_{gs,S1}$ and the reduction of R_{S1} , and consequently reduces i_{RS1} (**P2**, **P3**). The decrease of i_{RS1} , together with the rise of $i_{C,S1}$, reduces $i_{d,S2}$, which in turn reduces S_2 's dv/dt . Through this feedback, $C_{gd,S1}$'s dv/dt dynamically follows S_2 's dv/dt , while $v_{gs,S1}$ remains nearly constant, thereby manifesting the Inertia

plateau.

During $[t_4-t_5]$, as $v_{ds,S1}$ falls, $C_{gd,S1}$ enters its high-capacitance region and increases sharply, while $C_{oss,S2}$ remains low as $v_{ds,S2}$ approaches V_{DC} . The resulting increase in the charge-rate requirement of $C_{gd,S1}$ represents increased capacitive-charge inertia (**P1**). With $i_{g,S1}$ limited, a stronger feedback through coupled interactions arises (**P3**) for $C_{gd,S1}$ dv/dt to track S_2 's dv/dt . Consequently, $v_{gs,S1}$ drops, which manifests the Inertia drop. This Inertia drop raises R_{S1} and boosts $i_{g,S1}$ (**P2**). The increased R_{S1} , together with the reduced $v_{ds,S1}$, lowers i_{RS1} , suppresses $i_{d,S2}$ and thus limits S_2 's dv/dt ; meanwhile, an additional charge impulse is drawn from $C_{gs,S1}$ to discharge $C_{gd,S1}$ via R_{S1} (**P2**, **P3**). Together, these effects satisfy the rapidly increasing charge demand of $C_{gd,S1}$ and maintain dv/dt tracking.

After t_5 , as $v_{gs,S1}$ increases, R_{S1} decreases slowly, which causes a continued decay of the half-bridge midpoint voltage and thus a minor discharge of $C_{oss,S1}$ and charge of $C_{oss,S2}$ via R_{S1} , respectively (**P2**, **P3**).

Revealing causal mechanisms and the dynamical nature of representative ZVS through CUSST-enabled causal-mechanistic interpretability

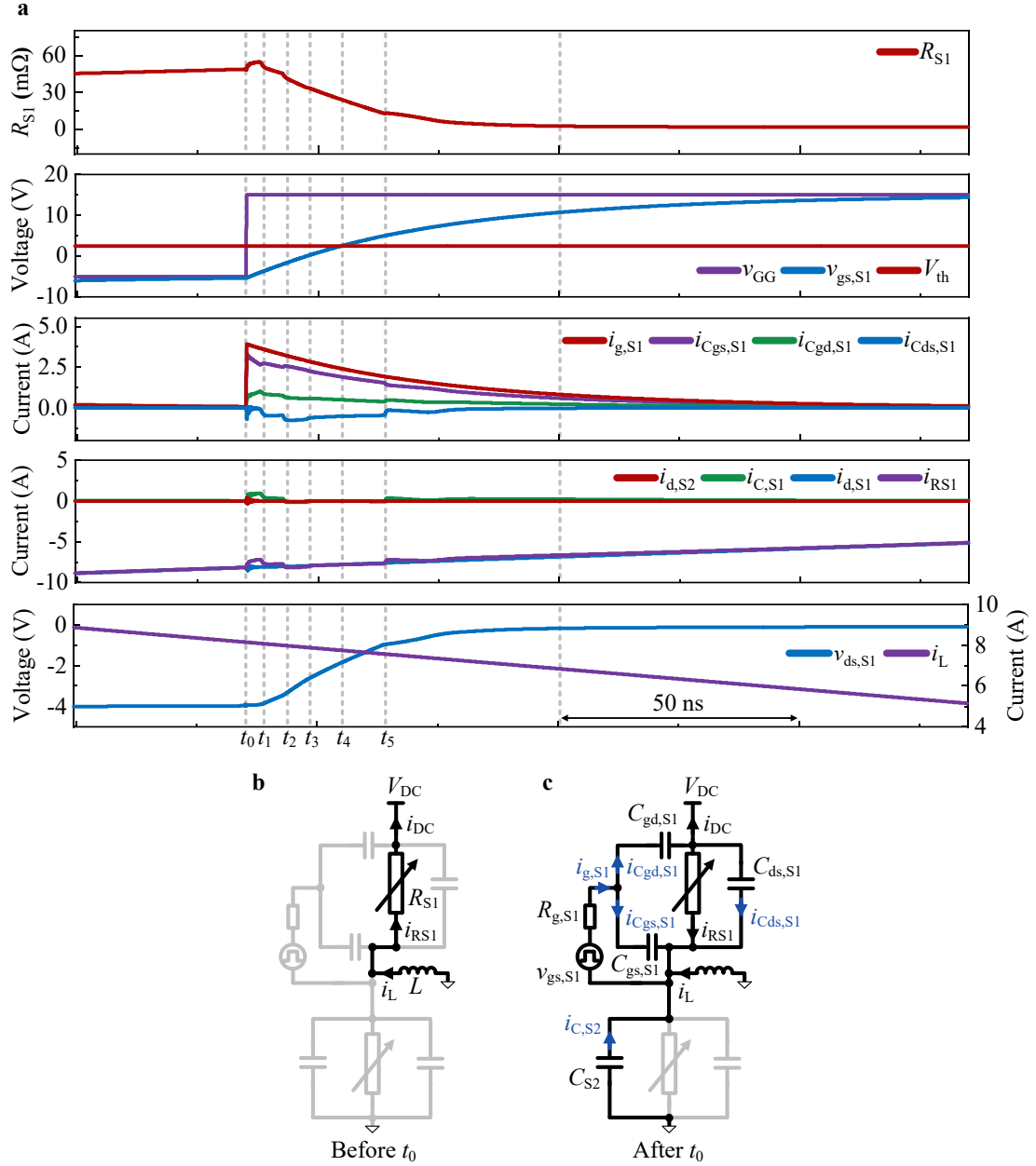


Fig. 4| Revealing causal mechanisms and the dynamical nature of representative ZVS through CUSST-enabled causal-mechanistic interpretability. **a**, Switching waveforms during a representative ZVS, obtained using LTspice. **b**, Operation mode before t_0 . **c**, Operation mode after t_0 . The equivalent-circuit formalism is obtained by **P1**; the highlighted branches in **b-c** indicate the current paths; the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

Before t_0 , i_L is reverse-conducted by R_{S1} . During $[t_0-t_1]$, as $v_{gs,S1} < -4$ V, its rise negligibly affects R_{S1} according to the R_{S1} - $v_{gs,S1}$ characteristic, which leads to negligible dv/dt ; $i_{g,S1}$ charges $C_{gs,S1}$ and discharges $C_{gd,S1}$ simultaneously (**P2**, **P3**). KCL at the half-bridge midpoint gives $|i_{RS1}| + |i_{Cgd,S1}| = |i_L| + |i_{Cds,S1}| + |i_{C,S2}|$. Therefore,

$|i_{C_{gd,S1}}| > |i_{C_{ds,S1}}| + |i_{C,S2}|$ yields $|i_{RS1}| < |i_L|$. This explains the brief reduction in $|i_{RS1}|$ relative to $|i_L|$, and the corresponding rise in R_{S1} .

After t_1 , $v_{gs,S1} > -4$ V and its rise significantly reduces R_{S1} , which in turn lowers the half-bridge midpoint voltage. As a result, $C_{ds,S1}$ is charged and $C_{oss,S2}$ is discharged via R_{S1} at the same time. During $[t_2-t_3]$, R_{S1} drops more rapidly, which produces a steep dv/dt and hence a higher $i_{C_{ds,S1}}$ to discharge $C_{ds,S1}$. During $[t_1-t_2]$ and $[t_3-t_4]$, R_{S1} decreases more slowly, which leads to a gentler dv/dt and hence a relatively lower $i_{C_{ds,S1}}$ (**P2**).

During $[t_4-t_5]$, as $v_{gs,S1} > V_{th,S1}$, S_1 's channel resistance decreases rapidly so that i_{RS1} is gradually commutated from S_1 's diode to S_1 's channel. As S_1 's diode current decreases, the reduced forward bias across the P-body/N-drift junction raises the effective barrier and suppresses hole injection into the conductivity-modulated drift region. Owing to carrier inertia described by **P1**, the drift region initially retains the distribution established at the preceding higher-diode-current state. The hole concentration therefore falls more rapidly near the depletion-region boundary than deeper within the drift region, creating a gradient that drives stored holes toward the junction. These holes are then swept by the depletion-region electric field back into the P-body and source, which contributes to the carrier recovery current, namely $i_{car,S1}$. There is no Inertia plateau or Inertia drop during the ZVS transition because the low dv/dt allows a fraction of $i_{g,S1}$ to satisfy $C_{gd,S1}$'s charge demand despite $C_{gd,S1}$ being in its high-capacitance region, thereby overcoming the capacitive-charge inertia (**P1**, **P3**).

At t_5 , the current commutation from S_1 's diode to S_1 's channel completes. After t_5 , as $i_{car,S1}$ decays, the half-bridge midpoint voltage decays toward V_{DC} , accompanied by minor discharges of $C_{ds,S1}$ and $C_{oss,S2}$ via R_{S1} simultaneously (**P2**, **P3**).

Discussion and outlook

We present CUSST, a general theory at conceptual, mechanistic, formal and analytical levels. CUSST reveals a charge-unified physical view of circuit elements, particularly semiconductor devices, as media for charge redistribution and transfer, thereby establishing a unified physical picture of switching across microscopic and macroscopic scales and throughout its spatial and temporal evolution. CUSST further

identifies switching as a dynamical process and reveals the origin of switching inertia, manifested as the Inertia plateau and Inertia drop arising from capacitive-charge inertia. Beyond revealing ZVS recovery, it identifies carrier inertia as the origin of recovery phenomena and unifies recovery mechanisms across scenarios, exemplifying the broader unity of their underlying carrier dynamics. To formalize CUSST-enabled insights, we present a representative physics-based equivalent-circuit formalism. CUSST further links switching dynamics to classical mechanics, suggesting that their dimensional correspondence is a manifestation of the underlying dynamical nature shared across disciplines. Therefore, CUSST establishes a unified, global, micro–macro spatiotemporal view of switching, moving beyond local and fragmented descriptions, while bridging circuit theory⁵³, conservation laws of energy and charge, and semiconductor physics. As a result, CUSST enables four fundamental unifications: in the nature of circuit elements via a charge-unified viewpoint; between charge- and energy-conservation frameworks; across macroscopic circuit-level and microscopic semiconductor-physics insights; and through three principles formulated to be generalizable across circuits, devices, scenarios and subintervals, providing a unifying basis under which equivalent-circuit formalisms can be constructed, with their applicability to other contexts open for future exploration. These unifications help to generalize circuit theory to all circuit elements, including semiconductor devices, while conferring unprecedented simplicity at the conceptual, formal and analytical levels and maintaining compatibility with existing theories and practical usability.

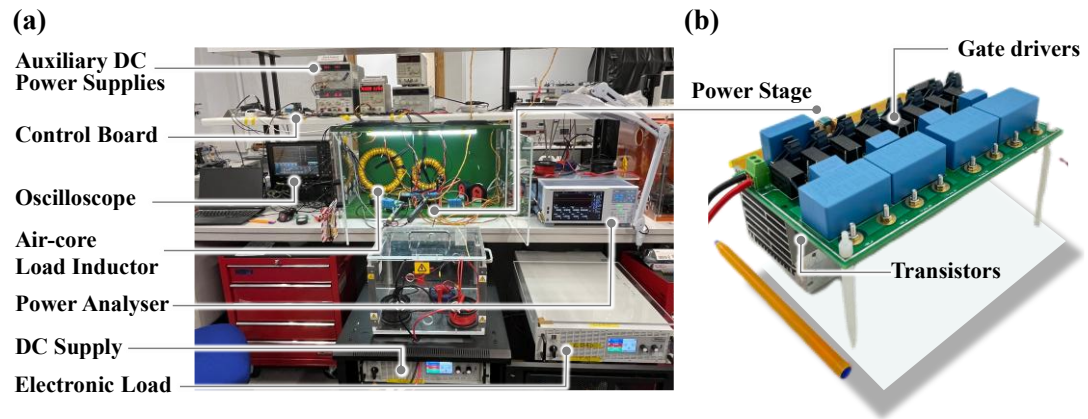
As demonstrated implications, we found that CUSST reveals the causal chain and dynamical mechanism underlying switching evolution across representative switching scenarios, with macro- and microscopic physical pictures unified and significant interactions accounted for. We further found that CUSST offers deterministic predictive capability through an CUSST-based E_{on} model, which achieves a 17-fold average error reduction compared to the conventional model¹⁴. In addition, we validated the fundamental applicability and equivalence of the energy- and charge-conservation frameworks in switching dynamics, revealing complementary perspectives on switching dynamics: energy conservation captures net energy redistribution and

dissipation, while charge conservation highlights the spatiotemporal charge evolution. These results confirm CUSST's compatibility with conservation laws, extending them to semiconductor devices. Together, these representative examples suggest that CUSST provides a basis for new theoretical systems.

Beyond the demonstrated examples, CUSST may have broader and longer-term implications whose full scope remains difficult to assess at this stage. For example, CUSST may help to identify directions across disciplines such as semiconductor materials²⁰, chip design²¹, packaging²², reliability^{23,24}, thermal engineering^{25,26}; in applications such as power electronics; and potentially across broader systems, including communications, computation devices and integrated circuits.^{27,28} More broadly, CUSST could support the design, optimization and standardization across semiconductor science, engineering and downstream applications, as illustrated by the related ZVS study¹³, which improved modelling accuracy 60-fold, now underpins ongoing international standardization and advances domains across the semiconductor value chain. Beyond this, CUSST could help unify these domains into a unified discipline across the semiconductor value chain including through enabling joint study, co-design, co-optimization, future full-chain causal feedback mechanisms and cross-domain research. For example, CUSST may translate application-level causal information such as constraints on loss, electrothermal stress and reliability into actionable priorities for upstream semiconductor materials, chip design, fabrication, packaging and reliability engineering, as well as downstream topology, layout, gate-drive, control and thermal co-design. CUSST-enabled, causally informed full-chain reliability co-design—guided by spatiotemporal thermal evolution and highly localized temperature peaks—could right-size die and cooling requirements, reducing overdesign while improving efficiency, environmental performance, lifespan and economic viability. As a specific case, CUSST may shift semiconductor optimization beyond conventional FOM optimization towards customized design weights. For example, in ZVS-capable applications, CUSST-informed weighting of residual switching and conduction losses may prioritize lower drift-region resistance in materials and chip design, alongside layouts that minimize parasitic capacitance. Besides, CUSST could

identify underlying causal mechanisms in loss- or electrothermal-stress-dominant switching subintervals and translate them into upstream materials, chip-design and packaging targets, while enabling reliability engineering to address associated electric-field, thermal-cycling and interface-degradation mechanisms beyond conventional average thermal metrics, thereby improving lifetime and cost-effectiveness. By enabling cross-domain causal links across the semiconductor value chain, CUSST could contribute to broader sustainability gains, as illustrated by prior achievements including a 50-fold increase in cooling coefficient of performance via electronics-thermal co-design²⁶, a 15.8-fold increase in thermal conductivity via materials-thermal-packaging-application co-design⁴¹, and a twofold increase in energy efficiency via device-circuit-architecture-algorithm research⁴², suggesting substantial opportunities across CUSST-enabled interfaces. We anticipate that CUSST, along with future developments, could extend to broader applications, including computing, communications and integrated circuits, supporting sustainable performance in systems key to AI, digitalization and electrification.

Extended Figure - Experimental platform



Extended Fig. 1. Experimental platform for E_{on} measurement, using a power electronic converter as the demonstrative example. **(a)** Overview picture of the entire experimental platform. **(b)** Close-up picture of the power electronic converter.

Table 2| Detailed data comparison of E_{on} measured results with calculated values using the CUSST-based model and conventional model, respectively

Device	V_{DC}	ΔV	Measured	Calculated	values	using	Calculated	values	using	Error reduction
conduction	(V)	(V)	results (μJ)	conventional model (μJ)	with		CUSST-based model (μJ)			$ e_{con}/e_{CUSST-based} $
resistance ($m\Omega$)				error (e_{con})			with error ($e_{CUSST-based}$)			
25	200	44	4.65	2.74	(-41.11%)		4.49	(-3.57%)		11.50
25	200	100	16.17	7.91	(-51.12%)		15.45	(-4.50%)		11.35
25	200	134	25.53	13.91	(-45.52%)		25.14	(-1.53%)		29.67
25	200	167	36.25	21.88	(-39.64%)		34.65	(-4.41%)		8.98
25	200	192	48.25	30.31	(-37.19%)		45.57	(-5.57%)		6.68
25	400	27	3.52	0.70	(-80.05%)		3.33	(-5.26%)		15.21
25	400	54	8.25	2.39	(-71.02%)		7.87	(-4.58%)		15.49
25	400	88	17.36	5.75	(-66.91%)		17.88	(2.95%)		22.66
25	400	137	33.21	12.91	(-61.11%)		34.14	(2.82%)		21.67
25	400	193	54.94	24.46	(-55.48%)		55.46	(0.94%)		58.75
25	400	255	85.42	41.79	(-51.08%)		84.67	(-0.88%)		57.75
25	400	312	115.68	62.76	(-45.75%)		110.10	(-4.82%)		9.49
25	400	382	163.86	99.24	(-39.44%)		157.42	(-3.93%)		10.02
80	200	38	1.59	0.709	(-55.36%)		1.40	(-11.60%)		4.77
80	200	73	4.24	2.38	(-43.78%)		4.50	(6.10%)		7.17
80	200	94	6.40	3.85	(-39.77%)		6.74	(5.40%)		7.37
80	200	116	9.47	5.78	(-38.91%)		9.96	(5.18%)		7.51
80	200	139	13.14	8.26	(-37.13%)		14.02	(6.70%)		5.54
80	200	163	17.88	11.42	(-36.11%)		18.87	(5.56%)		6.49
80	200	186	23.68	15.23	(-35.69%)		24.79	(4.69%)		7.61
80	400	40	2.17	0.748	(-65.60%)		2.05	(-5.79%)		11.33
80	400	65	3.89	1.82	(-53.14%)		4.06	(4.50%)		11.81
80	400	98	8.03	3.92	(-51.21%)		8.20	(2.12%)		24.13
80	400	131	13.50	6.77	(-49.82%)		13.66	(1.25%)		39.99
80	400	170	20.77	11.13	(-46.40%)		21.54	(3.73%)		12.45
80	400	212	30.73	17.05	(-44.53%)		31.65	(2.98%)		14.93
80	400	254	41.71	24.28	(-41.79%)		42.34	(1.51%)		27.70
80	400	302	55.54	34.10	(-38.61%)		57.40	(3.34%)		11.54
80	400	350	72.14	46.67	(-35.31%)		73.67	(2.11%)		16.70
80	400	387	89.57	58.75	(-34.41%)		87.35	(-2.49%)		13.85

Table 3| CUSST's charge-unified framework for semiconductor switching dynamics

Dynamical role	Charge Unified framework	Linear or nonlinear capacitive storage	Carrier-storage region
Momentum-like state variable	Stored charge Q as general state variable	$Q_x = \int C_x dv$	Stored carrier charge
Force-like state rate	$i_x = dQ_x/dt$	$i_x = dQ_x/dt = C_x(v)dv/dt$	$dQ_x/dt = i_{inj} - i_{ext} - i_{rec}$
Impulse-like state change	$\Delta Q_x = \int i_x dt$	$\Delta Q_x = \int C_x dv$	$\Delta Q_x = \int (i_{inj} - i_{ext} - i_{rec}) dt$
Underlying mechanism	Charge transfer or recombination	Charge transfer changes capacitive voltage	Injected, extracted or recombined charge changes
Energy association	Energy exchange or dissipation	$E_x = \int v dQ_x = \int v C_x(v) dv$	Energy exchange or dissipation
Associated state variables	All state variables	Variable Capacitances	Variable resistance (combined with gate-induced charge storage)
Role in CUSST	Unified and more fundamental framework	Generalized capacitive case	Generalized carrier-storage case

Methods

A representative equivalent-circuit formalism for switching dynamics

Taking a MOSFET-based half-bridge as an example, the conductive current path of S_1 is formalized by a single lumped variable resistor,^{7,8,53} defined by Ohm's law as $R_{S1} = v_{ds,S1} / i_{RS1}$. Here i_{RS1} denotes the current through this resistive path; i_{RS1} may include $C_{oss,S1}$ -related current components and recovery current when these currents circulate internally within the chip.

R_{S1} represents the lumped resistance of the conductive path(s), aggregating the channel resistance associated with the gate-induced charge, accumulation-, JFET- and drift-region resistances, contact resistance and other resistive components, some of which may be modulated by stored conductivity-modulation carriers. Its I–V characteristic follows the corresponding static output characteristic in forward conduction and third-quadrant characteristic in reverse conduction. At any operating point, R_{S1} equals the reciprocal slope of the line connecting that point to the origin of the I–V plane. The same formalism applies to R_{S2} . During half-bridge shoot-through, for example, the additional shoot-through current flows through both conductive paths formalized by R_{S1} and R_{S2} .

While C_{gs} is nearly constant, variable-capacitance formalisms are used for C_{gd} and C_{ds} .^{7,8,53} For example, in a MOSFET-based half-bridge, the displacement current components associated with $C_{ds,S1}$ and $C_{gd,S1}$ traverse the channel, accumulation, JFET and drift regions. Since R_{S1} primarily formalizes the aggregate resistance of these regions, $C_{ds,S1}$ and $C_{gd,S1}$ can be approximated as capacitive elements in parallel with R_{S1} . For simplicity, they may be combined into a single lumped output capacitance in parallel with R_{S1} in this representative formalism. The same applies to R_{S2} .

Whereas unipolar conduction in MOSFET does not involve minority-carrier injection or conductivity modulation, conduction through its body diode can involve both. Accordingly, during HS of S_1 , S_1 intrinsically contains no stored minority-carrier charge, whereas the body diode of S_2 may contain stored charge following prior bipolar conduction. The subsequent reverse bias of S_2 then induces reverse recovery, in addition

to the displacement current through $C_{oss,S2}$. This recovery component is therefore formalized by a current source in parallel with R_{S2} . During ZVS of S_1 , by contrast, its body diode may have conducted before channel turn-on and thus contain stored minority-carrier charge. As the diode current decreases, this charge is removed, producing a carrier-removal current—termed here the ZVS-recovery current—through the conductive path represented by R_{S1} and formalized by a current source in parallel with R_{S1} .

This representative formalism is demonstrated for MOSFETs; its extension to other device types, conduction modes and gate-bias conditions—including forward conduction in bipolar or conductivity-modulated devices such as IGBTs—is conceptually applicable in principle but requires future validation.

Omission of parasitic inductances from the CUSST formulation

Parasitic inductances inevitably exist in semiconductor devices, layouts and other circuit elements, and their inclusion would provide a closer representation of practical conditions. Their omission from the CUSST formulation is analogous to the idealized formulation of inertial motion in classical mechanics, where resistive effects such as air resistance exist in practice but are omitted to reveal the intrinsic dynamics of motion. This treatment isolates intrinsic switching dynamics and avoids obscuring the underlying switching causality. Furthermore, the parasitic inductances associated with packages and layouts are typically orders of magnitude larger than the parasitic inductance associated with the semiconductor device itself, and therefore usually dominate the overall parasitic inductance. Significant advances in packaging and layout technologies have nevertheless pushed the overall parasitic inductance towards increasingly low levels, with reported values already below 1 nH in recent literature^{22,56,57}, and future technologies are expected to reduce their influence further.

Criterion for turn-on onset

The absence of such criterion can lead to ambiguity in identifying the number and onset of turn-on events, potentially causing misinterpretation in situations involving crosstalk-induced gate spikes^{17,19}, multiple threshold crossings and multi-level gate-driving⁵⁸. Within CUSST, the onset of a turn-on event is explicitly defined as the instant

at which a threshold crossing of $v_{gs,S1}$ triggers the onset of a gate-induced decrease in R_{S1} , corresponding to the beginning of the gate-controlled conductive-path evolution toward the on state. Each threshold crossing that triggers such conductive-path evolution is counted as a distinct turn-on event. As the subsequent switching evolution follows this onset of gate-induced conductive-path evolution, this instant also defines the starting point of the corresponding spatiotemporal evolution.

Derivation of CUSST-based E_{on} model in the representative iZVS scenario

Derivation from charge conservation

With energy dissipation in C_{S1} is negligible relative to dissipation along the i_{RS1} paths^{59,60}, $E_{on,S1}$ is attributed entirely to R_{S1} :

$$E_{on,S1} = \int_{\text{switching-ON}} v_{ds,S1}(t) i_{RS1}(t) dt. \quad (1)$$

Applying KCL at $S1$'s drain terminal, gives

$$i_{RS1}(t) = i_{d,S1}(t) + i_{C_{gd,S1}}(t) + i_{C_{ds,S1}}(t) + i_{par,C_{gd,S1}}(t) + i_{par,C_{ds,S1}}(t). \quad (2)$$

Substituting (2) into (1), gives $E_{on,S1}$ as

$$E_{on,S1} = E_1 + E_2 + E_3 + E_4 + E_5, \quad (3)$$

where

$$\left. \begin{aligned} E_1 &= \int_{\text{switching-ON}} v_{ds,S1}(t) i_{d,S1}(t) dt, E_2 = \int_{\text{switching-ON}} v_{ds,S1}(t) i_{C_{gd,S1}}(t) dt, \\ E_3 &= \int_{\text{switching-ON}} v_{ds,S1}(t) i_{C_{ds,S1}}(t) dt, E_4 = \int_{\text{switching-ON}} v_{ds,S1}(t) i_{par,C_{gd,S1}}(t) dt, \\ E_5 &= \int_{\text{switching-ON}} v_{ds,S1}(t) i_{par,C_{ds,S1}}(t) dt, \end{aligned} \right\} \quad (4)$$

Since $v_{gs,S1}$ during (t_0-t_3) is negligible relative to the residual drain-source voltage at t_0 , denoted by ΔV , $v_{gs,S1}$ can be approximated as the constant V_{gp} . Consequently, $\Delta V - V_{gp} \approx \Delta V$ and $0 V - V_{gp} \approx 0 V$. Consequently,

$$\left. \begin{aligned} E_2 + E_3 &= E_{oss,S1}(\Delta V), \\ E_4 + E_5 &\approx \frac{1}{2} C_{par,S1} \Delta V^2, \end{aligned} \right\} \quad (5)$$

where

$$\left. \begin{aligned} E_4 &= \int_{0V-V_{gp}}^{\Delta V-V_{gp}} v_{ds,S1} C_{par,gd,S1}(v_{gd,S1}) dv_{gd,S1} \approx \underbrace{\int_0^{\Delta V} v_{ds,S1} C_{par,gd,S1}(v_{gd,S1}) dv_{gd,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{gd,S1}}, \\ E_5 &= \underbrace{\int_0^{\Delta V} v_{ds,S1} C_{par,ds,S1} dv_{ds,S1}}_{\text{Energy dissipated by capacitance in parallel with } C_{ds,S1}}, \end{aligned} \right\} \quad (6)$$

In addition, during (t_0-t_3) , the charges transferred to $C_{gd,S2}$, $C_{ds,S2}$ and their corresponding parallel capacitances, $C_{par,gd,S2}$ and $C_{par,ds,S2}$, are denoted as $\Delta Q_{gd,S2}$, $\Delta Q_{ds,S2}$, $\Delta Q_{par,gd,S2}$ and $\Delta Q_{par,ds,S2}$, respectively. Denoting $\Delta Q_{C,S2}$ as the total charge transferred to $C_{gd,S2}$, $C_{ds,S2}$ and their parallel capacitances, yields

$$\Delta Q_{C,S2} = \int_{\text{switching-ON}} i_{C,S2}(t) dt = \Delta Q_{S2} + C_{par,S2} \Delta V \quad (7)$$

where

$$\left. \begin{aligned} \Delta Q_{S2} &= \Delta Q_{gd,S2} + \Delta Q_{ds,S2} \approx Q_{oss,S2}(V_{DC}) - Q_{oss,S2}(V_{DC} - \Delta V), \\ \Delta Q_{par,S2} &= \Delta Q_{par,gd,S2} + \Delta Q_{par,ds,S2} \approx C_{par,gd,S2} \Delta V + C_{par,ds,S2} \Delta V, \end{aligned} \right\} \quad (8)$$

where

$$\left. \begin{aligned} \Delta Q_{gd,S2} &= \int_{\text{switching-ON}} i_{C_{gd,S2}}(t) dt = \int_{V_{DC}-\Delta V-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{gd,S2} dv_{gd,S2} \\ &\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2} dv_{gd,S2} = \int_{0V}^{V_{DC}} C_{gd,S2} dv_{gd,S2} - \int_{0V}^{V_{DC}-\Delta V} C_{gd,S2} dv_{gd,S2} \\ &= Q_{gd,S2}(V_{DC}) - Q_{gd,S2}(V_{DC} - \Delta V), \\ \Delta Q_{ds,S2} &= \int_{\text{switching-ON}} i_{C_{ds,S2}}(t) dt = \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} \\ &= \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} = \int_{0V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} - \int_{0V}^{V_{DC}-\Delta V} C_{ds,S2} dv_{ds,S2} \\ &= Q_{ds,S2}(V_{DC}) - Q_{ds,S2}(V_{DC} - \Delta V), \\ \Delta Q_{par,gd,S2} &= \int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{par,gd,S2}(v_{gd}) dv_{gd} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2}(v_{gd}) dv_{gd} \\ &= \left[\int_{0V}^{V_{DC}} C_{par,gd,S2}(v_{gd}) dv_{gd} - \int_{0V}^{V_{DC}-\Delta V} C_{par,gd,S2}(v_{gd}) dv_{gd} \right] = C_{par,gd,S2} \Delta V, \\ \Delta Q_{par,ds,S2} &= \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds}) dv_{ds} = \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds}) dv_{ds} \\ &= \left[\int_{0V}^{V_{DC}} C_{par,ds,S2}(v_{ds}) dv_{ds} - \int_{0V}^{V_{DC}-\Delta V} C_{par,ds,S2}(v_{ds}) dv_{ds} \right] = C_{par,ds,S2} \Delta V, \end{aligned} \right\} \quad (9)$$

Applying KVL across the loop incorporating the DC source, S_1 and S_2 yields

$$V_{DC} = v_{ds,S1}(t) + v_{ds,S2}(t). \quad (10)$$

Applying KCL at the source terminal of S_2 yields

$$i_{DC}(t) = i_{d,S2}(t) - i_L(t) = i_{RS2}(t) + i_{C,S2}(t) - i_L(t). \quad (11)$$

Substituting (10) and (11) into the expression of E_1 , yields

$$E_1 = E_{DC} - E_{1,1} + E_{AC-link}, \quad (12)$$

where the energy transferred from the DC source, denoted by E_{DC} , as well as two energy terms arising from breakdown of E_1 , denoted by $E_{1,1}$ and $E_{AC-link}$ are given by

$$\left. \begin{aligned}
E_{DC} &= \int_{\text{switching-ON}} V_{DC} i_{DC}(t) dt = V_{DC} \int_{\text{switching-ON}} [i_{RS2}(t) + i_{C,S2}(t) - i_L(t)] dt \\
&= V_{DC} \left[\int_{\text{switching-ON}} i_{RS2}(t) dt + \Delta Q_{S2} + C_{par,S2} \Delta V \right], \\
E_{1,1} &= \int_{\text{switching-ON}} v_{ds,S2}(t) i_{d,S2}(t) dt = \Delta E_{gd,S2} + \Delta E_{ds,S2} + \Delta E_{par,gd,S2} + \Delta E_{par,ds,S2} + \Delta E_{RS2}, \\
E_{AC-link} &= \int_{\text{switching-ON}} v_{ds,S2}(t) i_L(t) dt,
\end{aligned} \right\} \quad (13)$$

where $\Delta E_{gd,S2}$, $\Delta E_{ds,S2}$, $\Delta E_{par,gd,S2}$ and $\Delta E_{par,ds,S2}$ denote transferred energies associated with $C_{gd,S2}$, $C_{ds,S2}$, and their parallel capacitances, respectively; ΔE_{RS2} denotes the energy dissipation incurred in R_{S2} in case of a shoot-through event. These energy terms are given by

$$\left. \begin{aligned}
\Delta E_{gd,S2} &= \int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2} C_{gd,S2}(v_{gd,S2}) dv_{gd,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S2} C_{gd,S2}(v_{gd,S2}) dv_{gd,S2}, \\
\Delta E_{ds,S2} &= \int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2} C_{ds,S2}(v_{ds,S2}) dv_{ds,S2}, \\
\Delta E_{par,gd,S2} &= \int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2} C_{par,gd,S2}(v_{gd,S2}) dv_{gd,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S2} C_{par,gd,S2}(v_{gd,S2}) dv_{gd,S2}, \\
\Delta E_{par,ds,S2} &= \int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2} C_{ds,S2}(v_{ds,S2}) dv_{ds,S2}, \\
\Delta E_{RS2} &= \int_{\text{switching-ON}} v_{ds,S2}(t) i_{RS2}(t) dt,
\end{aligned} \right\} \quad (14)$$

Substituting (14) into (12) yields

$$\begin{aligned}
E_{1,1} &\approx \underbrace{E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC} - \Delta V)}_{\text{Energy stored by } C_{oss,S2}} + \underbrace{\frac{1}{2} C_{par,S2} [V_{DC}^2 - (V_{DC} - \Delta V)^2]}_{\text{Energy stored by the paralleled capacitance of } S2} \\
&+ \underbrace{\int_{\text{switching-ON}} v_{ds,S2}(t) i_{RS2}(t) dt}_{\text{Energy dissipation in } S2 \text{ due to shoot-through}}
\end{aligned} \quad (15)$$

Combining (1)(3)(4)(5)(8)(9)(12)(13)(14)(15) yields the $E_{on,S1}$ model derived from the perspective of charge conservation:

$$E_{on,S1} = E_{DC} + E_{AC-link} - E_{1,1} + E_2 + E_3 + E_4 + E_5, \quad (16)$$

In detail, the $E_{on,S1}$ model is expressed as follows, with interpretations provided for each energy term:

$$\begin{aligned}
E_{\text{on},S1} \approx & V_{DC} \left[\underbrace{\int_{\text{switching-ON}} i_{RS2}(t) dt + \Delta Q_{S2} + C_{\text{par},S2} \Delta V}_{\text{Energy provided by DC source to the half-bridge}} - \underbrace{\int_{\text{switching-ON}} i_L(t) dt}_{\text{Energy stored by the paralleled capacitances of } S2} \right] \\
& + \underbrace{\int_{\text{switching-ON}} v_{ds,S2}(t) i_L(t) dt}_{\text{Energy provided by the overall AC-link impedance to the half-bridge}} - \frac{1}{2} C_{\text{par},S2} [V_{DC}^2 - (V_{DC} - \Delta V)^2] \\
& - \underbrace{[E_{\text{oss},S2}(V_{DC}) - E_{\text{oss},S2}(V_{DC} - \Delta V)]}_{\text{Energy stored by output capacitance of } S2} - \underbrace{\int_{\text{switching-ON}} v_{ds,S2}(t) i_{RS2}(t) dt}_{\text{Energy dissipated in } RS2 \text{ due to shoot-through}} \\
& + \underbrace{E_{\text{oss},S1}(\Delta V) + \frac{1}{2} C_{\text{par},S1} \Delta V^2}_{\text{Energy dissipated in } RS1 \text{ due to discharge of } S1\text{'s output capacitance and paralleled capacitances}}.
\end{aligned} \tag{17}$$

Derivation from energy conservation

During the S_1 's switching-on process, the half-bridge is taken as the study object. For simplicity reasons, the analysis is limited to (t_0-t_3) as vast majority of the energy dissipation during S_1 's turn-on is incurred during this interval. According to the law of energy conservation, the overall energy initially stored in the study object, minus the various dissipated energies incurred during the turn-on process and the energy delivered to the external circuit, yields the remaining stored energy at the end of the turn-on process. The general mathematical expression is given by

$$E_{\text{initial}} - E_{\text{dissipated}} - E_{\text{delivered}} = E_{\text{final}} \tag{18}$$

where E_{initial} denotes the overall energy stored in the study object at the initial instant; $E_{\text{dissipated}}$ denotes the total energy losses during S_1 's turn-on process, including but not limited to turn-on loss and ESR losses; $E_{\text{delivered}}$ denotes the energy delivered to the external circuit; E_{final} denotes the total energy stored in the study object at the end of the process. Among them, E_{initial} is given by

$$E_{\text{initial}} = E_{\text{initial},S1} + E_{\text{initial},S2}, \tag{19}$$

where

$$\left. \begin{aligned} E_{\text{initial},S1} &= E_{\text{initial,Cgd},S1} + E_{\text{initial,Cds},S1} + E_{\text{initial,par,gd},S1} + E_{\text{initial,par,ds},S1}, \\ E_{\text{initial},S2} &= E_{\text{initial,Cgd},S2} + E_{\text{initial,Cds},S2} + E_{\text{initial,par,gd},S2} + E_{\text{initial,par,ds},S2}, \end{aligned} \right\} \tag{20}$$

where $E_{\text{initial},Sx}$, $E_{\text{initial,Cgd},Sx}$, $E_{\text{initial,Cds},Sx}$, $E_{\text{initial,par,gd},Sx}$, $E_{\text{initial,par,ds},Sx}$ denote the total initial energy stored in the parasitic capacitances of S_x (with $x=1,2$ representing the upper and lower devices, respectively), including the energies stored in $C_{\text{gd},Sx}$, $C_{\text{ds},Sx}$, as well as

their corresponding parallel capacitances $C_{\text{par,gd},Sx}$ and $C_{\text{par,gd},Sx}$, respectively, given by:

$$\left. \begin{aligned} E_{\text{initial,Cgd},S1} &= E_{\text{gd},S1} (\Delta V - v_{\text{gs},S1}(t_0)), E_{\text{initial,Cds},S1} = E_{\text{ds},S1} (\Delta V), \\ E_{\text{initial,par,gd},S1} &= \frac{1}{2} C_{\text{par,gd},S1} (\Delta V - v_{\text{gs},S1}(t_0))^2, E_{\text{initial,par,ds},S1} = \frac{1}{2} C_{\text{par,ds},S1} (\Delta V)^2, \\ E_{\text{initial,Cgd},S2} &= E_{\text{gd},S2} (V_{\text{DC}} - \Delta V - v_{\text{gs},S2}(t_0)), E_{\text{initial,Cds},S2} = E_{\text{ds},S2} (V_{\text{DC}} - \Delta V), \\ E_{\text{initial,par,gd},S2} &= \frac{1}{2} C_{\text{par,gd},S2} (V_{\text{DC}} - \Delta V - v_{\text{gs},S2}(t_0))^2, \\ E_{\text{initial,par,ds},S2} &= \frac{1}{2} C_{\text{par,ds},S2} (V_{\text{DC}} - \Delta V)^2, \end{aligned} \right\} \quad (21)$$

where $v_{\text{gs},S1}(t_0) = V_{\text{th},S1}$.

Similarly, E_{final} is given by

$$E_{\text{final}} = E_{\text{final},S1} + E_{\text{final},S2}, \quad (22)$$

where

$$\left. \begin{aligned} E_{\text{final},S1} &= E_{\text{final,Cgd},S1} + E_{\text{final,Cds},S1} + E_{\text{final,par,gd},S1} + E_{\text{final,par,ds},S1}, \\ E_{\text{final},S2} &= E_{\text{final,Cgd},S2} + E_{\text{final,Cds},S2} + E_{\text{final,par,gd},S2} + E_{\text{final,par,ds},S2}, \end{aligned} \right\} \quad (23)$$

where

$$\left. \begin{aligned} E_{\text{final,Cgd},S1} &= E_{\text{gd},S1} (0V - v_{\text{gs},S1}(t_3)), E_{\text{final,Cds},S1} = E_{\text{ds},S1} (0V), \\ E_{\text{final,par,gd},S1} &= \frac{1}{2} C_{\text{par,gd},S1} (0V - v_{\text{gs},S1}(t_3))^2, E_{\text{final,par,ds},S1} = \frac{1}{2} C_{\text{par,ds},S1} (0V)^2, \\ E_{\text{final,Cgd},S2} &= E_{\text{gd},S2} (V_{\text{DC}} - 0V - v_{\text{gs},S2}(t_3)), E_{\text{final,Cds},S2} = E_{\text{ds},S2} (V_{\text{DC}} - 0V), \\ E_{\text{final,par,gd},S2} &= \frac{1}{2} C_{\text{par,gd},S2} (V_{\text{DC}} - 0V - v_{\text{gs},S2}(t_3))^2, E_{\text{final,par,ds},S2} = \frac{1}{2} C_{\text{par,ds},S2} (V_{\text{DC}} - 0V)^2, \end{aligned} \right\} \quad (24)$$

Since both $v_{\text{gs},S1}$ and $v_{\text{gs},S2}$ at any instant during the switching-on process are negligible relative to ΔV or $V_{\text{DC}} - \Delta V$, both $v_{\text{gs},S1}$ and $v_{\text{gs},S2}$ can be approximated to 0 V, which yields

$$\left. \begin{aligned} E_{\text{initial,Cgd},S1} &\approx E_{\text{gd},S1} (\Delta V), E_{\text{initial,Cds},S1} = E_{\text{ds},S1} (\Delta V), \\ E_{\text{initial,par,gd},S1} &\approx \frac{1}{2} C_{\text{par,gd},S1} (\Delta V)^2, E_{\text{initial,par,ds},S1} = \frac{1}{2} C_{\text{par,ds},S1} (\Delta V)^2, \\ E_{\text{initial,Cgd},S2} &\approx E_{\text{gd},S2} (V_{\text{DC}} - \Delta V), E_{\text{initial,Cds},S2} = E_{\text{ds},S2} (V_{\text{DC}} - \Delta V), \\ E_{\text{initial,par,gd},S2} &\approx \frac{1}{2} C_{\text{par,gd},S2} (V_{\text{DC}} - \Delta V)^2, E_{\text{initial,par,ds},S2} = \frac{1}{2} C_{\text{par,ds},S2} (V_{\text{DC}} - \Delta V)^2, \\ E_{\text{final,Cgd},S1} &\approx E_{\text{gd},S1} (0V) = 0J, E_{\text{final,Cds},S1} = E_{\text{ds},S1} (0V) = 0J, \\ E_{\text{final,par,gd},S1} &\approx \frac{1}{2} C_{\text{par,gd},S1} (0V)^2 = 0J, E_{\text{final,par,ds},S1} = \frac{1}{2} C_{\text{par,ds},S1} (0V)^2 = 0J, \\ E_{\text{final,Cgd},S2} &\approx E_{\text{gd},S2} (V_{\text{DC}} - 0V), E_{\text{final,Cds},S2} = E_{\text{ds},S2} (V_{\text{DC}} - 0V), \\ E_{\text{final,par,gd},S2} &\approx \frac{1}{2} C_{\text{par,gd},S2} (V_{\text{DC}} - 0V)^2, E_{\text{final,par,ds},S2} = \frac{1}{2} C_{\text{par,ds},S2} (V_{\text{DC}} - 0V)^2, \end{aligned} \right\} \quad (25)$$

Consequently, E_{initial} and E_{final} can be approximated as

$$\left. \begin{aligned} E_{\text{initial}} &\approx \left[E_{\text{oss},S1} (\Delta V) + \frac{1}{2} C_{\text{par},S1} (\Delta V)^2 \right] + \left[E_{\text{oss},S2} (V_{\text{DC}} - \Delta V) + \frac{1}{2} C_{\text{par},S2} (V_{\text{DC}} - \Delta V)^2 \right], \\ E_{\text{final}} &\approx E_{\text{oss},S2} (V_{\text{DC}}) + \frac{1}{2} C_{\text{par},S2} V_{\text{DC}}^2. \end{aligned} \right\} \quad (26)$$

During S_1 's turn-on process, the dominant energy dissipation in the study object is $E_{\text{on},S1}$ and the dissipation incurred within R_{S2} in the case of a shoot-through event. Hence, $E_{\text{dissipated}}$ can be approximated as comprising only these two components, namely

$$E_{\text{dissipated}} \approx E_{\text{on},S1} + E_{\text{dissipated},S2}, \quad (27)$$

where

$$E_{\text{dissipated},S2} = \underbrace{\int_{\text{switching-ON}} v_{\text{ds},S2}(t) i_{\text{RS2}}(t) dt}_{\text{Energy dissipated in } R_{S2} \text{ in the event of shoot through}}. \quad (28)$$

The energy delivered to the external circuit by the study object, namely $E_{\text{delivered}}$ could be derived as

$$E_{\text{delivered}} = -(W_{\text{DC}} + W_{\text{L}}), \quad (29)$$

where W_{DC} and W_{L} denote the work done by the DC source and load inductor to the study object, respectively. In order to obtain W_{DC} , it is important to determine the total charge transferred by the DC source, denoted as ΔQ_{DC} over the turn-on process, while the charges transferred to $C_{\text{gd},S2}$, $C_{\text{ds},S2}$ and their corresponding parallel capacitances are denoted as $\Delta Q_{\text{gd},S2}$, $\Delta Q_{\text{ds},S2}$, $\Delta Q_{\text{par,gd},S2}$ and $\Delta Q_{\text{par,ds},S2}$, respectively, together with their sum denoted as $\Delta Q_{\text{C},S2}$; ΔQ_{RS2} and ΔQ_{L} denote the charge through R_{S2} and load inductor, respectively.

Applying KCL at S_2 's source terminal yields

$$i_{\text{DC}}(t) = i_{\text{d},S2}(t) - i_{\text{L}}(t) = i_{\text{C},S2}(t) + i_{\text{RS2}}(t) - i_{\text{L}}(t). \quad (30)$$

Integrating both sides of (30) yields

$$\Delta Q_{\text{DC}} = \Delta Q_{\text{C},S2} + \Delta Q_{\text{RS2}} - \Delta Q_{\text{L}}, \quad (31)$$

where

$$\left. \begin{aligned} \Delta Q_{\text{DC}} &= \int_{\text{switching-ON}} i_{\text{DC}}(t) dt, \Delta Q_{\text{C},S2} = \int_{\text{switching-ON}} i_{\text{C},S2}(t) dt, \\ \Delta Q_{\text{RS2}} &= \int_{\text{switching-ON}} i_{\text{RS2}}(t) dt, \Delta Q_{\text{L}} = \int_{\text{switching-ON}} i_{\text{L}}(t) dt, \end{aligned} \right\} \quad (32)$$

where

$$\Delta Q_{\text{C},S2} = \Delta Q_{\text{gd},S2} + \Delta Q_{\text{ds},S2} + \Delta Q_{\text{par,gd},S2} + \Delta Q_{\text{par,ds},S2}, \quad (33)$$

where

$$\left. \begin{aligned}
\Delta Q_{gd,S2} &= \int_{\text{switching-ON}} i_{C_{gd,S2}}(t) dt = \int_{\text{switching-ON}} C_{gd,S2} \frac{dv_{gd,S2}}{dt} dt \\
&= \int_{V_{DC}-\Delta V - v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{gd,S2} dv_{gd,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2} dv_{gd,S2}, \\
\Delta Q_{ds,S2} &= \int_{\text{switching-ON}} i_{C_{ds,S2}}(t) dt = \int_{\text{switching-ON}} C_{ds,S2} \frac{dv_{ds,S2}}{dt} dt \\
&= \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2}, \\
\Delta Q_{par,gd,S2} &= \int_{\text{switching-ON}} i_{C_{par,gd,S2}}(t) dt = \int_{\text{switching-ON}} C_{par,gd,S2} \frac{dv_{gd,S2}}{dt} dt \\
&= \int_{V_{DC}-\Delta V - v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{par,gd,S2} dv_{gd,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2} dv_{gd,S2}, \\
\Delta Q_{par,ds,S2} &= \int_{\text{switching-ON}} i_{C_{par,ds,S2}}(t) dt = \int_{\text{switching-ON}} C_{par,ds,S2} \frac{dv_{ds,S2}}{dt} dt \\
&= \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2} dv_{ds,S2} \approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2} dv_{ds,S2},
\end{aligned} \right\} \quad (34)$$

Consequently, $\Delta Q_{C,S2}$ can be approximated as

$$\Delta Q_{C,S2} \approx Q_{oss,S2}(V_{DC}) - Q_{oss,S2}(V_{DC} - \Delta V) + (C_{par,gd,S2} + C_{par,ds,S2})\Delta V = \Delta Q_{S2} + C_{par,S2}\Delta V, \quad (35)$$

Hence, W_{DC} can be determined as

$$\begin{aligned}
W_{DC} &= \int_{\text{switching-ON}} V_{DC} i_{DC}(t) dt = V_{DC} \Delta Q_{DC} \\
&= V_{DC} \left[\Delta Q_{S2} + C_{par,S2} \Delta V + \int_{\text{switching-ON}} i_{RS2}(t) dt - \int_{\text{switching-ON}} i_L(t) dt \right].
\end{aligned} \quad (36)$$

The work done by the load inductor, denoted by W_L can be determined as

$$W_L = \int_{\text{switching-ON}} v_L(t) i_L(t) dt = \int_{\text{switching-ON}} v_{ds,S2}(t) i_L(t) dt. \quad (37)$$

Substituting (36) and (37) into (29) yields

$$\begin{aligned}
E_{\text{delivered}} &= -(W_{DC} + W_L) \\
&= -V_{DC} \left[\Delta Q_{S2} + C_{par,S2} \Delta V + \int_{\text{switching-ON}} i_{RS2}(t) dt - \int_{\text{switching-ON}} i_L(t) dt \right] - \int_{\text{switching-ON}} v_{ds,S2}(t) i_L(t) dt.
\end{aligned} \quad (38)$$

Combining (26)(27)(28)(38) yields the $E_{on,S1}$ model from perspective of energy conservation:

$$\begin{aligned}
E_{\text{on},S1} \approx & V_{\text{DC}} \left[\underbrace{\int_{\text{switching-ON}} i_{\text{RS2}}(t) dt + \Delta Q_{S2} + C_{\text{par},S2} \Delta V}_{\text{Energy provided by DC source to the half-bridge}} - \underbrace{\int_{\text{switching-ON}} i_L(t) dt}_{\text{Energy stored by output capacitance of } S_2} \right] \\
& + \underbrace{\int_{\text{switching-ON}} v_{\text{ds},S2}(t) i_L(t) dt}_{\text{Energy provided by the load inductor to the half-bridge}} - \underbrace{\left[E_{\text{oss},S2}(V_{\text{DC}}) - E_{\text{oss},S2}(V_{\text{DC}} - \Delta V) \right]}_{\text{Energy stored by output capacitance of } S_2} \\
& - \underbrace{\int_{\text{switching-ON}} v_{\text{ds},S2}(t) i_{\text{RS2}}(t) dt}_{\text{Energy dissipated in } S_2 \text{ due to shoot-through}} - \underbrace{\frac{1}{2} C_{\text{par},S2} \left[V_{\text{DC}}^2 - (V_{\text{DC}} - \Delta V)^2 \right]}_{\text{Energy stored by the paralleled capacitance of } S_2} \\
& + \underbrace{E_{\text{oss},S1}(\Delta V) + \frac{1}{2} C_{\text{par},S1} \Delta V^2}_{\text{Energy dissipated in } S1 \text{ due to discharge of } S1\text{'s output capacitance and paralleled capacitance}}
\end{aligned} \tag{39}$$

Notably, (39) is identical to (17), which demonstrates that the energy- and charge-conservation derivations yield the same CUSST-based E_{on} model. This confirms the equivalent applicability of both conservation laws to semiconductor switching and extends their applicability to semiconductor devices. The equivalence further reveals two complementary physical views in the switching dynamics: energy conservation highlights the net energy redistribution and dissipation, while charge conservation elucidates the spatiotemporal charge evolution.

Revealing causal mechanisms and the dynamical nature of representative iZVS through CUSST-enabled causal-mechanistic interpretability

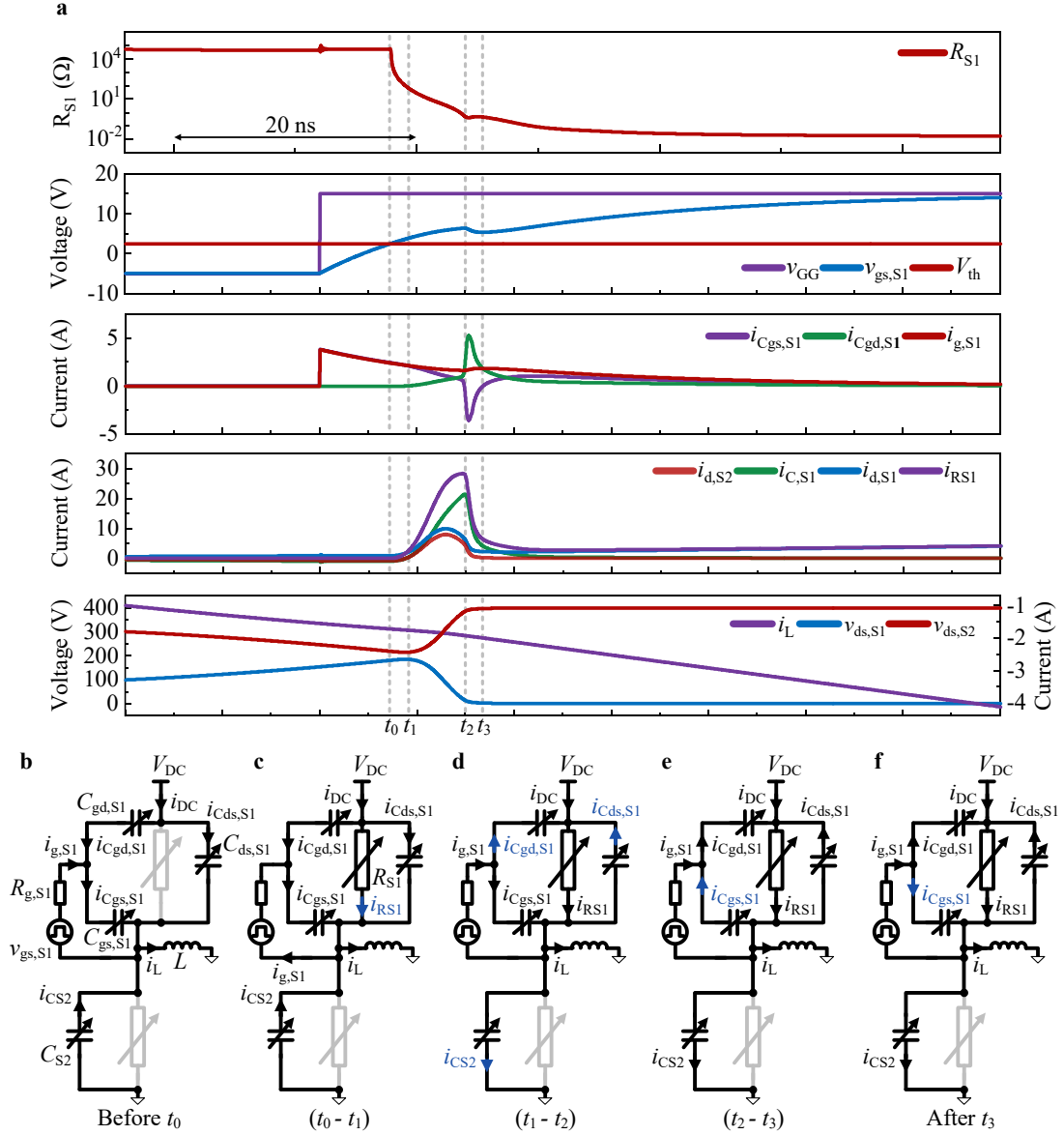


Fig. 5| Causal-Mechanistic Interpretability of Switching Dynamics in a Representative iZVS Scenario. **a**, Switching waveforms in a representative iZVS scenario (i_L flows out from the half-bridge midpoint throughout the entire iZVS). **b**, Operation mode before t_0 . **c**, Operation mode during subinterval $(t_0 - t_1)$. **d**, Operation mode during subinterval $(t_1 - t_2)$. **e**, Operation mode $(t_2 - t_3)$. **f**, Operation mode after t_3 . The equivalent-circuit formalism is obtained based on $\mathbf{P}_1$; the highlighted branches in **b-f** indicate the current paths; the current components that differ from those in the immediately preceding sub-figure are highlighted in blue.

Before t_0 (i.e., the onset of the iZVS), i_L charges $C_{oss,S1}$ and discharges $C_{oss,S2}$ simultaneously, while $i_{g,S1}$ charges $C_{gs,S1}$ ($\mathbf{P}_3$). During $[t_0 - t_1]$, i_L continues to charge $C_{oss,S1}$ and discharge $C_{oss,S2}$ simultaneously; as $v_{gs,S1}$ rises above $V_{th,S1}$, R_{S1} decreases rapidly, which increases i_{RS1} and progressively commutates i_L from $C_{oss,S1}$ and $C_{oss,S2}$ to

R_{S1} until full conduction at t_1 (**P2, P3**).

During $[t_1-t_2]$, initially, as $v_{gs,S1}$ increases, R_{S1} decreases, which increases i_{RS1} (**P2**). As a result, i_{CS2} increases (**P3**); together with a decrease of $C_{oss,S2}$, it leads to an increase in S_2 's dv/dt . As $C_{gd,S1}$ requires a large charge rate to follow the dv/dt evolution, a feedback mechanism arises, through the coupled interactions described by **P3**, to overcome S_1 's capacitive-charge inertia identified by **P1**. In this feedback, more $i_{g,S1}$ diverts to $C_{gd,S1}$, which increases $i_{Cgd,S1}$, and thus promotes $C_{gd,S1}$'s dv/dt , while $i_{Cgs,S1}$ decreases (**P3**), which slows the rise of $v_{gs,S1}$, the reduction of R_{S1} , and thus the increase of i_{RS1} (**P2**). Given a rapid rise of i_{CS1} , the slower i_{RS1} rise suppresses di/dt of $i_{d,S2}$ (**P3**), which is initially positive, but becomes negative before t_2 , and thus limits S_2 's dv/dt , despite the decrease of $C_{oss,S2}$ (**P2**). This feedback satisfies $C_{gd,S1}$'s charge-rate requirement to follow S_2 's dv/dt evolution.

During $[t_2-t_3]$, $C_{oss,S2}$ remains low as $v_{ds,S2}$ approaches V_{DC} ; S_2 's dv/dt remains significant despite limited $i_{d,S2}$. As $v_{ds,S1}$ decreases, $C_{gd,S1}$ enters its high-capacitance region, and increases further; therefore, a greater charge rate is required by $C_{gd,S1}$ to follow S_2 's dv/dt (**P1**). As $i_{g,S1}$ alone cannot satisfy $C_{gd,S1}$'s higher charge-rate requirement, a further feedback mechanism arises through coupled interactions (**P3**) to overcome S_1 's increased capacitive-charge inertia (**P1**). In this feedback, $C_{gs,S1}$ transfers a charge impulse to discharge $C_{gd,S1}$ via S_1 's channel, which causes an Inertia drop in $v_{gs,S1}$ (**P2, P3**). This raises $i_{g,S1}$, increases $i_{Cgd,S1}$, and increases R_{S1} ; together with the fall of $v_{ds,S1}$, i_{RS1} rapidly decreases (**P2**). Consequently, $i_{d,S2}$ is suppressed (**P3**), which directly limits S_2 's dv/dt . This feedback satisfies $C_{gd,S1}$'s charge-rate requirement to follow S_2 's dv/dt evolution.

After t_3 , $C_{gs,S1}$ no longer discharges; instead, $i_{g,S1}$ charges both $C_{gs,S1}$ and $C_{gd,S1}$ simultaneously (**P3**). As $v_{gs,S1}$ further increases, R_{S1} decays further, which causes $v_{ds,S1}$ to decay further (**P2**). As a result, the half-bridge midpoint voltage gradually approaches V_{DC} , accompanied by minor discharge of $C_{oss,S1}$ and charge of $C_{oss,S2}$ via R_{S1} (**P2, P3**).

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Data availability

The data presented in this study are available in this manuscript.

Code availability

No custom code was used in this study.

Reference

- 1 International Energy Agency. Net Zero by 2050: A Roadmap for the Global Energy Sector. (2021).
- 2 Bardeen, J. B., W. H. The Transistor, A Semi-Conductor Triode. *Physical Review* (1948).
- 3 IEEE International Roadmap for Devices and Systems: Beyond CMOS and Emerging Materials Integration. (IEEE, Piscataway, NJ, 2023).
- 4 Chua, L. O. Memristor—The Missing Circuit Element. *IEEE Transactions on Circuit Theory* **18**, 507-519, doi:10.1109/TCT.1971.1083337 (1971).
- 5 Baliga, B. J. *Fundamentals of Power Semiconductor Devices*. (Springer, 2008).
- 6 Robert W. Erickson, D. M. *Fundamentals of Power Electronics*. (Springer New York, NY).
- 7 Horowitz, P. & Hill, W. *The Art of Electronics*. (Cambridge University Press, 2015).
- 8 Powell, E. I. R. G. in *Introduction to Electric Circuits* (ed Eur Ing R. G. Powell) 10-39 (Butterworth-Heinemann, 1995).
- 9 IEC 60747-9: Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors. *International Electrotechnical Commission (IEC)*.
- 10 IEC 60747-8: Semiconductor devices – Discrete devices – Part 8: Field-effect transistors. *International Electrotechnical Commission (IEC)*.
- 11 Wu, Y., Wang, L., Wang, J., Shi, Z. & Zhang, J. Comparison and Optimization of Datasheet-Driven Extraction of Gate-Drain Overlap Oxide Capacitance in IGBT Modeling. *IEEE Transactions on Power Electronics* **37**, 14023-14027, doi:10.1109/TPEL.2022.3194023 (2022).
- 12 Li, X. *et al.* A SiC Power MOSFET Loss Model Suitable for High-Frequency Applications. *IEEE Transactions on Industrial Electronics* **64**, 8268-8276, doi:10.1109/TIE.2017.2703910 (2017).
- 13 Ying, W. *et al.* Towards the True Zero-Voltage-Switching Boundary. *IEEE Transactions on Power Electronics*, 1-6, doi:10.1109/TPEL.2025.3592857 (2025).
- 14 Kasper, M., Burkart, R. M., Deboy, G. & Kolar, J. W. ZVS of Power MOSFETs Revisited. *IEEE Transactions on Power Electronics* **31**, 8063-8067, doi:10.1109/TPEL.2016.2574998 (2016).
- 15 Chen, K., Zhao, Z., Yuan, L., Lu, T. & He, F. The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET. *IEEE Transactions on Electron Devices* **62**, 333-338, doi:10.1109/TED.2014.2362657 (2015).
- 16 Wang, L. *et al.* A Brief Review of SiC MOSFET Transient Analytical Modeling Methods: Principles, Current Status, and Parameters Modeling. *IEEE Transactions on Power Electronics* **40**, 5177-5189, doi:10.1109/TPEL.2024.3439364 (2025).
- 17 Zhang, Z. *et al.* Methodology for Wide Band-Gap Device Dynamic Characterization. *IEEE Transactions on Power Electronics* **32**, 9307-9318, doi:10.1109/TPEL.2017.2655491 (2017).

- 18 Zhang, Z., Guo, B. & Wang, F. Evaluation of Switching Loss Contributed by Parasitic Ringing for Fast Switching Wide Band-Gap Devices. *IEEE Transactions on Power Electronics* **34**, 9082-9094, doi:10.1109/TPEL.2018.2883454 (2019).
- 19 Ahmed, M. R., Todd, R. & Forsyth, A. J. Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions. *IEEE Transactions on Industrial Electronics* **64**, 9001-9011, doi:10.1109/TIE.2017.2721882 (2017).
- 20 Kang, H. & Udrea, F. True Material Limit of Power Devices—Applied to 2-D Superjunction MOSFET. *IEEE Transactions on Electron Devices* **65**, 1432-1439, doi:10.1109/TED.2018.2808181 (2018).
- 21 He, Q. *et al.* Numerical Simulation and Analytical Modeling of Multichannel AlGaN/GaN Devices. *IEEE Transactions on Electron Devices* **71**, 1710-1717, doi:10.1109/TED.2024.3359165 (2024).
- 22 Janabi, A. *et al.* Substrate Embedded Power Electronics Packaging for Silicon Carbide mosfets. *IEEE Transactions on Power Electronics* **39**, 9614-9628, doi:10.1109/TPEL.2024.3396779 (2024).
- 23 Yu, L. C. *et al.* Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments. *IEEE Transactions on Device and Materials Reliability* **10**, 418-426, doi:10.1109/TDMR.2010.2077295 (2010).
- 24 Lutz, J., Schlangenotto, H., Scheuermann, U. & De Doncker, R. *Semiconductor Power Devices: Physics, Characteristics, Reliability*. (Springer Cham, 2018).
- 25 Zhang, Y., Wang, H., Wang, Z., Yang, Y. & Blaabjerg, F. Simplified Thermal Modeling for IGBT Modules With Periodic Power Loss Profiles in Modular Multilevel Converters. *IEEE Transactions on Industrial Electronics* **66**, 2323-2332, doi:10.1109/TIE.2018.2823664 (2019).
- 26 van Erp, R., Soleimanzadeh, R., Nela, L., Kampitsis, G. & Matioli, E. Co-designing electronics with microfluidics for more sustainable cooling. *Nature* **585**, 211-216, doi:10.1038/s41586-020-2666-1 (2020).
- 27 Cao, W. *et al.* The future transistors. *Nature* **620**, 501-515, doi:10.1038/s41586-023-06145-x (2023).
- 28 Rezaei, M., Esteghamat, A. & Matioli, E. Terahertz Electronic Metadevices: Principles Behind the Ultra-High Cutoff Frequency. *IEEE Electron Device Letters* **46**, 1986-1989, doi:10.1109/LED.2025.3606749 (2025).
- 29 International Energy Agency. World Energy Outlook 2025. (IEA, Paris, 2025).
- 30 *Future Jobs: Robots, Artificial Intelligence, and Digital Platforms*. (World Bank, 2025).
- 31 International Energy Agency. Global EV Outlook 2025. (2025).
- 32 International Energy Agency. The Future of Heat Pumps. (2022).
- 33 International Energy Agency. Global Hydrogen Review 2025. (2025).
- 34 U.S. Department of Energy. ADEPT: Efficient Power Conversion. (U.S. Department of Energy, Advanced Research Projects Agency–Energy (ARPA-E), Washington, DC, United States, 2011).
- 35 Aczel, M., Chamanara, S., Matin, M., Farsi, A., Marwala, T., Madani, K. Environmental Cost of AI's Energy Use: Carbon, Water and Land Footprints. (United Nations University Institute for Water, Environment and Health (UNU-INWEH), Richmond Hill, Ontario, Canada, 2026).
- 36 onsemi. *Meeting the AI Data Center Power Challenge*, <<https://www.onsemi.com/company/news-media/blog/industrial/en-us/meeting-the-ai-data-center-power-challenge>> (2024).
- 37 Emberson, L. & Cottier, B. GPUs account for about 40% of power usage in AI data centers. *Epoch*

- AI Data Insights* (2025).
- 38 Swiss Federal Office of Energy. Swiss Electricity Statistics 2025. (Bern, 2026).
- 39 International Energy Agency. Energy and AI. (2025).
- 40 Zhang, B. & Wang, S. A Survey of EMI Research in Power Electronics Systems With Wide-Bandgap Semiconductor Devices. *IEEE Journal of Emerging and Selected Topics in Power Electronics* **8**, 626-643, doi:10.1109/JESTPE.2019.2953730 (2020).
- 41 Zhou, X. *et al.* Insulating electromagnetic-shielding silicone compound enables direct potting electronics. *Science* **385**, 1205-1210, doi:10.1126/science.adp6581 (2024).
- 42 Wan, W. *et al.* A compute-in-memory chip based on resistive random-access memory. *Nature* **608**, 504-512, doi:10.1038/s41586-022-04992-8 (2022).
- 43 Baliga, B. J. Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters* **10**, 455-457, doi:10.1109/55.43098 (1989).
- 44 Huang, A. Q. New unipolar switching power device figures of merit. *IEEE Electron Device Letters* **25**, 298-301, doi:10.1109/LED.2004.826533 (2004).
- 45 Porter, M. *et al.* Switching figure-of-merit, optimal design, and power loss limit of (ultra-) wide bandgap power devices: A perspective. *Applied Physics Letters* **125**, 110501, doi:10.1063/5.0222105 (2024).
- 46 Anderson, J. A., Zulauf, G., Kolar, J. W. & Deboy, G. New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties. *IEEE Open Journal of Power Electronics* **1**, 322-338, doi:10.1109/OJPEL.2020.3018220 (2020).
- 47 Pavlidis, G., Kendig, D., Heller, E. R. & Graham, S. Transient Thermal Characterization of AlGaIn/GaN HEMTs Under Pulsed Biasing. *IEEE Transactions on Electron Devices* **65**, 1753-1758, doi:10.1109/TED.2018.2818621 (2018).
- 48 d'Alessandro, V. & Rinaldi, N. A critical review of thermal models for electro-thermal simulation. *Solid-State Electronics* **46**, 487-496, doi:[https://doi.org/10.1016/S0038-1101\(01\)00323-9](https://doi.org/10.1016/S0038-1101(01)00323-9) (2002).
- 49 Blaabjerg, F. *et al.* Advances in Reliability and Artificial Intelligence for Power Electronic Systems. *IEEE Transactions on Power Electronics* **41**, 12386-12409, doi:10.1109/TPEL.2026.3675661 (2026).
- 50 Andresen, M. & Liserre, M. Impact of active thermal management on power electronics design. *Microelectronics Reliability* **54**, doi:10.1016/j.microrel.2014.07.069 (2014).
- 51 Umans, S. D. *Fitzgerald & Kingsley's Electric Machinery*. 7th edn, (2014).
- 52 International Electrotechnical Commission. IEC TR 63604 ED1: Performance of power electronic transformer for flexible transmission and distribution systems [forthcoming; available upon request]. (International Electrotechnical Commission, 2026).
- 53 Nilsson, J. W. & Riedel, S. A. *Electric Circuits*. 12th edn, (Pearson, 2024).
- 54 Wolfspeed, I. C2M0080120D Silicon Carbide MOSFET Datasheet. (Wolfspeed, Inc.).
- 55 Wolfspeed, I. C2M0025120D Silicon Carbide MOSFET Datasheet. (Wolfspeed, Inc.).
- 56 Du, Y. *et al.* Reducing Near-Field Magnetic Radiation and Parasitic Inductance in SiC Half-Bridge Modules via Optimized Shielding Design. *IEEE Transactions on Power Electronics* **40**, 12003-12010, doi:10.1109/TPEL.2025.3571008 (2025).
- 57 Shillaber, L., Jiang, Y., Ran, L. & Long, T. Ultrafast Current Shunt (UFCS): A Gigahertz Bandwidth Ultra-Low-Inductance Current Sensor. *IEEE Transactions on Power Electronics* **37**, 15493-15504, doi:10.1109/TPEL.2022.3184638 (2022).

- 58 Shelton, E., Rogers, D. & Palmer, P. *Fast Switching of GaN Transistors using a Boosted Gate Voltage*. Vol. 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe) (IEEE, 2023).
- 59 Li, X. *et al.* Achieving Zero Switching Loss in Silicon Carbide MOSFET. *IEEE Transactions on Power Electronics* **34**, 12193-12199, doi:10.1109/TPEL.2019.2906352 (2019).
- 60 Jafari, A. *et al.* Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies. *IEEE Transactions on Power Electronics* **35**, 12595-12600, doi:10.1109/TPEL.2020.2990628 (2020).

Competing Interests Statement

The authors declare no competing interests.

Supplementary Information

N/A