Towards the True Switching-ON of Transistors

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Abstract

Transistors are core component across all domains of electrical and electronic engineering (EEE), such as data centers,[1,2] electrified transportation,[3,4] robotics,[5] renewables[6,7] and grid applications,[8-10] etc. Transistors' switching behavior governs energy loss, carbon emissions, cooling demand, water use, lifetime, material use and cost etc. throughout EEE. Despite near a century since the transistor's invention,[11,12] the understanding of transistor switching remains fragmented: switching is treated as a black box relying on observed waveforms, cannot be explained using physical laws alone, and is not integrated into circuit theory. This forms one of the most critical barriers to recognizing the true physical boundaries, prohibiting more sustainable solutions. For example, the conventional E_{on} prediction model, derived from the conventional switching analysis, exhibits significant prediction errors (ranging from 34.41% to 80.05%). Here we present a unified first-principles paradigm to explain the switching phenomena. Using this paradigm, we revealed the physical origins and mechanisms of switching-ON phenomena across scenarios, and derived the proposed E_{on} prediction model, with error ranging from 0.88% to 11.60%, achieving a 17-fold

average improvement. These results demonstrate the unprecedented power of the proposed paradigm: textbook-level foundations are established, transforming the fundamental understanding of transistor switching from empirical to first-principles analysis, and simultaneously stimulating follow-up research and applications for sustainable development across disciplines including materials science,[13,14] semiconductor physics,[15,16] device engineering,[17,18] packaging,[19,20] reliability,[21,22] thermal management,[2,23] power electronics,[24,25] and even sustainability sciences,[2,26,27] standards,[28] economics,[29] policy[30,31] and education.[32,33]

Keyword: transistors' switching behavior, switching phenomena, first-principles paradigm, switching loss, switching loss prediction, sustainability, electrical and electronic engineering

Introduction

Electrification, digitalization, and intelligentization are global megatrends placing unprecedented demands on electrical and electronic engineering (EEE). Across domains such as AI-driven data centers,[1,2] electrified transportation,[3,4] robotics,[5,34] renewable energy systems[6,7] and grid applications,[8,9] global electricity consumption and associated carbon emissions are projected to over double within the next two decades,[35] creating urgent challenges and calling for fundamentally more sustainable solutions. For example, energy supplies alone account for approximately 75% of global carbon emissions.[24] Nearly all of these developments are ultimately underpinned by transistors – transistors' switching behaviors define the fundamental boundaries of efficiency, reliability, and sustainability etc., thereby shaping nearly all applications.[36-40]

Consequently, most research and applications rely on accurate switching analysis, with E_{on} as a key metric.[32,33,37,41,42] Despite the central role, the understanding of switching behaviors has remained fragmented for nearly a century, dating back to the invention of the transistor.[11,12] To our knowledge, no equivalent-circuit model unifies semiconductor physics with circuit laws whilst reflecting true physical insights and energy dissipation. As circuit laws alone cannot explain the switching phenomena,

switching is treated as a black box, with analyses relying on inputs of observed waveforms, typically linearized waveforms approximated from empirical waveforms,[32,33,41,43,44]. Consequently, the physical origins and fundamental mechanisms of switching phenomena remain only partially understood. For example, the cause of the well-known 'Miller platform'[32,33,41-50] as well as the voltage drop at the end of 'Miller platform' remains unresolved.

A key reason is the lack of recognition of the influence of the complementary switch (CS)'s non-linear dynamics - switching is typically analyzed on the switch under study (SUS) alone.[32,33,41,43] Whilst prior works[44,45] identified the CS's overvoltage caused by HS of the SUS, the influence of CS's non-linear dynamics on the SUS's HS behavior is unrecognized. Moreover, the unrecognized causal role of R_{SI} variation in the causal reasoning contributes to the fragmented understanding of switching phenomena, but also leaves the switching-ON event without a defined criterion, causing confusion in certain cases.

Perera et al.[47] and Kasper et al.[46] identified the SUS discharging and CS charging currents in ZCS and iZVS, respectively, pointing out the role of output capacitances in E_{on} modelling. Zhang et al.[42] pointed out the load inductor's contribution in the energy balance in double-pulse tests, whilst Kasper et al.[46] derived the conventional iZVS E_{on} model from energy conservation. However, the influence of load current in iZVS, as well as the existence of CC and its associated dissipated energy remain beyond recognition, leading to their absence from the conventional E_{on} model[46]; the intrinsic unification of energy and charge conservation remain unresolved.

Under these contexts, we propose a first-principles unified paradigm that transforms the understanding of switching phenomena relying on empirical observation to one derivable from fundamental physical laws solely—achieving, for the first time, a true and intrinsic unification of transistor switching behavior with physical laws. The paradigm offers unprecedented explanatory and predictive power: it reveals the physical origins and fundamental mechanisms of switching-ON across scenarios for the first time, including the physical insights into the famous "Miller platform"[32,33,41-50]; it also yields a new E_{on} prediction model with a 17-fold accuracy improvement over the

conventional model[46]—a breakthrough that identifies the physical boundaries and opens new directions for both fundamental research and practical applications.

The proposed paradigm establishes a textbook-level foundation with transformative implications from fundamental sciences and research to global sustainability. Its implication spans disciplines from semiconductor materials science,[13,14] semiconductor physics[15,16] and device engineering[17,18] to packaging,[19,20] reliability,[21,22] thermal management,[2,23] power electronics[24,25] and even sustainability sciences,[2,26,27] standards,[28] economics,[29] policy[30,31] and education.[32,33] It supports global sustainability by improving energy efficiency, cutting carbon emissions, extending lifetime, reducing material use and costs etc. across all domains of EEE.

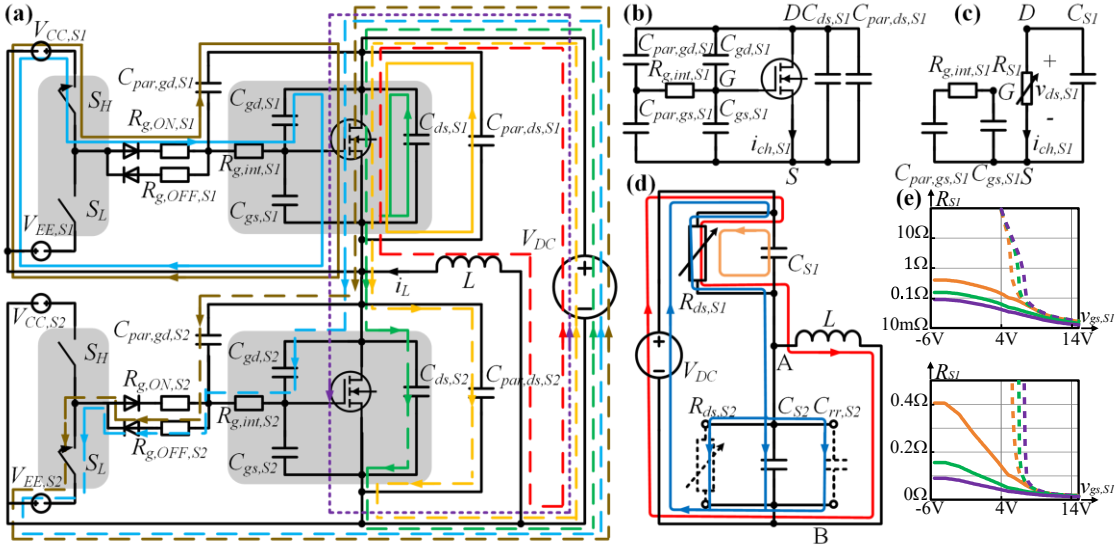


Figure 1. **(a)** Illustration of individual current components during VF when the load current flows out from the mid-point of the half-bridge during the entire iZVS process. **(b)** Conventional equivalent-circuit model of S_1. **(c)** Proposed equivalent-circuit model of S_1. **(d)** Simplified equivalent circuit of **(a)** using the proposed equivalent-circuit model for switching-ON analysis. Potentially, when there is a shoot-through, $R_{ds,S2}$ is present; when there is a RR occurring in the VF, $C_{rr,S2}$ is present. **(e)** R_{S1} versus $v_{gs,S1}$ in forward (dashed) and reverse conduction (solid); orange, green and purple are for 10A, 30A and 60A conducting current, respectively: the upper sub-figure shows the behavior over the large gate-voltage range and the lower sub-figure highlights the low-resistance behavior.

The proposed first-principles unified paradigm

We propose a first-principles unified paradigm that derives and explains switching phenomena solely from fundamental physical laws—including circuit laws and conservation laws—enabling causal reasoning without relying on inputs from observed waveforms, and universally applicable across device types and switching scenarios.

The key elements of the proposed paradigm include:

1. **Unified equivalent-circuit modeling across device types, switching scenarios and switching phases** (detailed in *Methods*) — including a non-linear equivalent resistance (e.g., R_{S1} model), consistent with both semiconductor physics and Ohm's law, and equivalent capacitance models (e.g., $C_{rr,S2}$ model) to represent reverse-recovery charge.
2. ***R_{S1}* variation as the primary cause** — defining the switching-ON criterion (the initial rapid drop of R_{S1} when $v_{gs,S1}$ exceeds the threshold; detailed in *Methods*), and governing the entire turn-on process as the main driver.
3. **Coupling effects of the complementary switch's non-linear dynamics** — incorporating non-linear junction-capacitance transitions of the complementary switch as essential inputs beyond the recognition of the conventional analysis.
4. **Revealing the role of load current** — exemplified by explicit recognition of the existence of CC in iZVS and its associated dissipated energy, as well as the participation and work done by the load inductor throughout the process, both beyond recognition of conventional analysis.

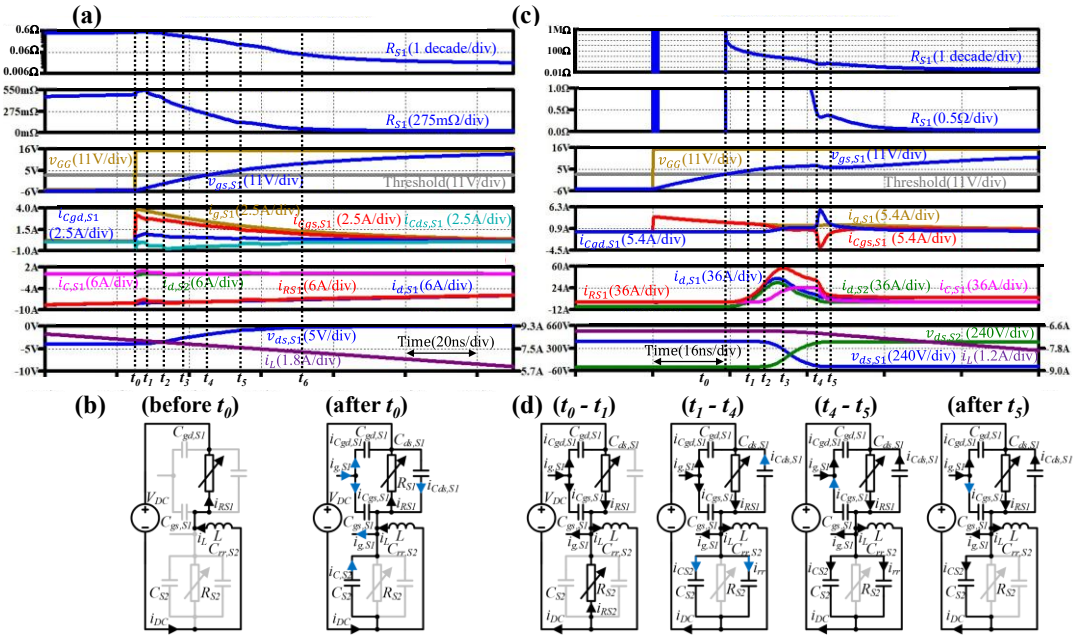


Figure 2. **(a)** Simulated waveforms during a typical ZVS process in LTspice. **(b)** The operation modes during a typical ZVS process. **(c)** Simulated waveforms during a typical hard switching-ON process in LTspice. **(d)** The operation modes during a typical hard switching-ON process.

Revealing the Physical Origin and Fundamental Mechanism of the Zero-Voltage-

Switching-ON (ZVS) process using the proposed paradigm

Before t_0, i_L is reverse-conducted by S_1. During (t_0-t_1), as $v_{gs,S1}$<-4V, $v_{gs,S1}$ increase has negligible influence on R_{S1}; $i_{g,S1}$ charges $C_{gs,S1}$ and discharges $C_{gd,S1}$ simultaneously. Applying KCL at the mid-point yields $|i_{RS1}|+|i_{Cgd,S1}|=|i_L|+|i_{Cds,S1}|$. Since $|i_{Cgd,S1}|>|i_{Cds,S1}|$, $|i_{RS1}|<|i_L|$, explaining the observed drop in $|i_{RS1}|$, which causes a rise in R_{S1}. As $C_{ds,S1}$ is high and $i_{Cds,S1}$ is low, S_1's *dv/dt* of is low - $v_{ds,S1}$ remains nearly constant.

After t_1, as $v_{gs,S1}$>-4V, its increase causes R_{S1} to decrease, decreasing $v_{ds,S1}$, thereby building up both $i_{Cds,S1}$ and $i_{C,S2}$ via S_1's channel. During (t_2-t_3), R_{S1} falls most rapidly per unit rise in $v_{gs,S1}$, causing the quickest fall in $v_{ds,S1}$ and hence the peak $i_{Cds,S1}$. During (t_1-t_2) and (t_3-t_5), R_{S1} falls more slowly, leading to a slower fall in $v_{ds,S1}$ and secondary peaks in $i_{Cds,S1}$. After t_5, increasing $v_{gs,S1}$'s influence on reducing R_{S1} weakens further. As R_{S1} flattens, the midpoint voltage drops slightly, with a minor discharge of $C_{oss,S1}$ and C_{S2} via R_{S1}.

Revealing the Physical Origin and Fundamental Mechanism of the Hard Switching-ON (HS) process using the proposed paradigm

At t_0, i.e., the onset of HS, i_L is reverse-conducted by R_{S2}. During (t_0 - t_1), whilst $v_{ds,S1}$ remains nearly constant, with increasing $v_{gs,S1}$, R_{S1} decreases rapidly, increasing i_{RS1}. As a result, a lossy CC occurs during which i_L gradually commutates from R_{S2} to R_{S1}.

At t_1, i_L is entirely conducted by R_{S1}, indicating completion of the CC; a RR and a VF commence simultaneously, where the excessive carriers in S_2 is removed by the combined effects of recombination and $i_{d,S2}$, also known as reverse-recovery current. After t_1, $i_{d,S2}$ charges C_{S2} via R_{S1}, increasing $v_{ds,S2}$ and raising midpoint voltage. As S_1's drain voltage remains at the positive DC rail, $v_{ds,S1}$ drops, resulting in a discharging current through C_{S1} via R_{S1}. Notably, during (t_1-t_5), $|dv_{ds,S2}/dt|=i_{d,S2}/(C_{S2}+C_{rr,S2})$.

During (t_1-t_3), a quicker relative drop in R_{S1} compared to $v_{ds,S1}$ ($|dR_{S1}/R_{S1}|>|dv_{ds\_S1}/v_{ds\_S1}|$) causes a continued increase in i_{RS1}, increasing $i_{d,S2}$; meanwhile, as $v_{gs,S1}$ increases, $|dR_{S1}/R_{S1}|$ decreases, leading to a reduced *di/dt* of i_{RS1}.

During (t_1-t_2), although $C_{oss,S2}$ decreases and $i_{d,S2}$ increases, causing an increase in S_2's *dv/dt*, *dv/dt* remains low due to high $C_{oss,S2}$. Therefore, only a small portion of i_g is required by $C_{gd,S1}$ to track S_2's *dv/dt*, allowing most of i_g to charge $C_{gs,S1}$.

During (t_2-t_3), $C_{oss,S2}$ transitions from its high- to low-capacitance region, leading to an increase in S_2's *dv/dt*. As negative feedback, more i_g is diverted to $C_{gd,S1}$, leading to: (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, which slows the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction and consequently slowing i_{RS1} increase. The slower i_{RS1} increase, combined with a significant increase in i_{CS1}, reduces the *di/dt* of $i_{d,S2}$ – initially positive then turning negative before t_3 – thus limiting increase in S_2's *dv/dt* despite decreasing $C_{oss,S2}$. As a result of the feedback, $C_{gd,S1}$'s *dv/dt* follows S_2's *dv/dt*.

During (t_3-t_4), the quicker relative reduction in $v_{ds,S1}$ than the relative reduction in R_{S1}, causes a decrease in i_{RS1}. Initially, as $C_{ds,S1}$ and $C_{gd,S1}$ increase whilst *dv/dt* changes insignificantly, $i_{C,S1}$ has a brief increase; more i_g is diverted to $C_{gd,S1}$. Both decreasing i_{RS1} and increasing $i_{C,S1}$ contribute to a decrease in $i_{d,S2}$. After that, i_{RS1} continues to drop, decreasing $i_{d,S2}$, which leads to a decreasing *dv/dt*. As *dv/dt* decreases whilst $C_{ds,S1}$ and $C_{gd,S1}$ increase, $i_{Cds,S1}$ and $i_{Cgd,S1}$ nearly stabilize.

During (t_4-t_5), as $v_{ds,S1}$ falls, $C_{gd,S1}$ enters its high-capacitance region and rises sharply. In contrast, as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low, yet $i_{d,S2}$ sustains a significant *dv/dt*. Hence, $i_{Cgd,S1}$ must be sufficient to sustain a comparable *dv/dt* for $C_{gd,S1}$. Consequently, limited i_g causes further negative feedback – a drop in $v_{gs,S1}$, which boosts i_g, strengthening $i_{Cgd,S1}$; simultaneously it causes R_{S1}'s rise, combined with $v_{ds,S1}$ reduction, lowering i_{RS1}, and suppressing $i_{d,S2}$ and thus S_2's *dv/dt*. Besides, a complementary current pulse from $C_{gs,S1}$ results to help discharge $C_{gd,S1}$ via R_{S1}. These effects ensure that $C_{gd,S1}$'s *dv/dt* follows S_2's *dv/dt*.

After t_5, as $v_{gs,S1}$ further increases, R_{S1} decreases slowly, causing a slight drop in mid-point voltage and consequently a minor discharge and charge of C_{S1} and C_{S2} via R_{S1}, respectively.

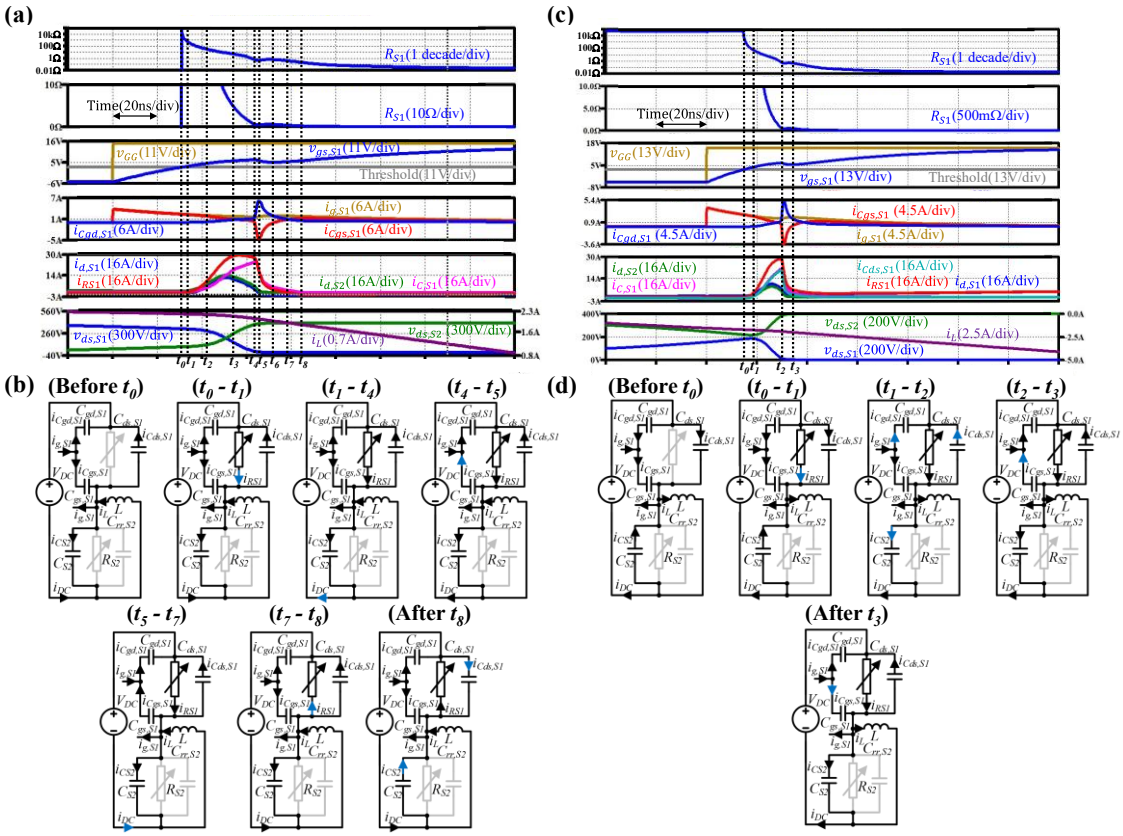


Figure 3. **(a)** Simulated waveforms during a typical iZVS process (case 1) in LTspice. **(b)** The operation modes during a typical iZVS process (case 1). **(c)** Simulated waveforms during a typical iZVS process (case 2) in LTspice. **(d)** The operation modes during a typical iZVS process (case 2).

Revealing the Physical Origin and Fundamental Mechanism of Incomplete Zero-Voltage-Switching-ON (iZVS) process using the proposed paradigm

Case 1: i_L flows into the half-bridge midpoint throughout the entire iZVS process

Before t_0, i.e., the onset, i_L discharges C_{S1} and charges C_{S2} simultaneously. During (t_0-t_1), the low $i_{d,S2}$ results in a low S_2's *dv/dt*, despite the low $C_{oss,S2}$. Consequently, only a small portion of i_g discharging $C_{gd,S1}$ is required to follow S_2's *dv/dt*, allowing most of i_g to charge $C_{gs,S1}$. This leads to a significant increase in $v_{gs,S1}$, sharply reducing R_{S1}, consequently increasing i_{RS1} significantly. As a result, a lossy CC occurs, where the C_{S1}-conducted share of i_L commutates to C_{S2}. Unlike the near-zero *dv/dt* in the CC of HS, this CC features a non-zero *dv/dt* that increases with time due to the increasing i_{CS2} and decreasing $C_{oss,S2}$. At t_1, i_{RS1} exceeds $i_{C,S1}$, indicating the completion of the CC and triggering a reversal of i_{DC}'s direction.

During (t_1-t_2), $i_{RS1}+i_L=i_{d,S2}+i_{C,S1}$. Due to the initially high R_{S1}, i_{RS1} and thus $i_{d,S2}$ are low. As $v_{gs,S1}$ increases, R_{S1} decreases, increasing i_{RS1} and consequently $i_{d,S2}$. Unlike in

(t_1-t_2) of the HS, the much lower $C_{oss,S2}$ leads to a higher *dv/dt*, which combined with the higher $C_{oss,S1}$, results in higher $i_{C,S1}$. This, in turn, limits $i_{d,S2}$'s increase, thereby slowing *dv/dt* rise. Consequently, only a small portion of i_g is diverted to discharge $C_{gd,S1}$ to follow S_2's *dv/dt*, whilst the majority charges $C_{gs,S1}$.

During (t_2-t_3), the continued increase in i_{RS1} leads to an increase in $i_{d,S2}$, consequently an increase in *dv/dt*. As negative feedback, more i_g is diverted to $C_{gd,S1}$, leading to two consequences: (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, which slows the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction and consequently slowing i_{RS1} increase. The slower increase in i_{RS1}, combined with a significant increase in $i_{C,S1}$, reduces the *di/dt* of $i_{d,S2}$ – initially positive in (t_2-t_3), eventually becoming negative before t_3 - limiting increase in *dv/dt* despite the decreasing $C_{oss,S2}$. As a result of these combined effects, $C_{gd,S1}$ manages to follow S_2's *dv/dt*.

During (t_3-t_4), the quicker relative reduction in $v_{ds,S1}$ than the relative reduction in R_{S1}, causes a slight decrease in i_{RS1}, contributing to a decreasing $i_{d,S2}$. A significant increase in $C_{gd,S1}$ and $C_{ds,S1}$ causes an increase in $i_{Cgd,S1}$ and $i_{Cds,S1,}$ respectively, and thus the increase in $i_{C,S1}$, also contributing to the decrease in $i_{d,S2}$. Despite a slower relative drop in $C_{oss,S2}$, the significant decrease in $i_{d,S2}$ leads to a slight decrease in S_2's *dv/dt* and consequently a slight decrease in S_1's *dv/dt*. Hence, more i_g is diverted to discharge $C_{gd,S1}$, further slowing the increase of $v_{gs,S1}$ and thus slowing the reduction in R_{S1}.

During (t_4-t_6), $C_{gd,S1}$ is in its high-capacitance region, increasing rapidly as $v_{ds,S1}$ decreases; as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low; as $i_{d,S2}$ remains significant, S_2's *dv/dt* remains significant. Consequently, $C_{gd,S1}$'s *dv/dt* has to remain significant. The insufficient i_g to maintain $C_{gd,S1}$'s *dv/dt* to track S_2's *dv/dt*, triggers further negative feedback – a drop in $v_{gs,S1}$. This boosts i_g, enhancing $i_{Cgd,S1}$, but also increases R_{S1}, which combined with decreasing $v_{ds,S1}$, leads to a rapid reduction in i_{RS1}, and consequently a decreasing $i_{d,S2}$, thereby a lower *dv/dt*. Meanwhile, $C_{gs,S1}$ supplies a pulse current to help discharge $C_{gd,S1}$ via R_{S1}. Together, these effects enable $C_{gd,S1}$'s *dv/dt* to follow S_2's. Notably, at t_5, i_{RS1} drops below i_{CS1}, causing a direction reversal of i_{DC}.

During (t_6-t_8), $C_{gs,S1}$ stops supplying charge and is instead charged by i_g, which supplies charge to both $C_{gs,S1}$ and $C_{gd,S1}$. Notably, the mid-point voltage remains below

V_{DC} before t_7 keeping I_{RS1} positive; after t_7, the mid-point voltage exceeds V_{DC}, reversing I_{RS1}'s direction. Meantime, the C_{S2}-conducted share of i_L gradually commutates to S_1. At t_8, the current commutation is completed and C_{S2} is fully charged, raising the mid-point voltage to $V_{DC}+R_{S1}(t_8)i_L(t_8)$. After t_8, as $v_{gs,S1}$ further increases, R_{S1} decreases slowly, causing a slight drop in mid-point voltage and consequently a minor discharge of C_{S1} and C_{S2} via R_{S1}.

Case 2: i_L flows out from the half-bridge midpoint throughout the entire iZVS process

Before t_0, i.e., the onset, i_L charges C_{S1} and discharges C_{S2} simultaneously. During (t_0-t_1), i_L continues to charge C_{S1} and discharge C_{S2} simultaneously; as $v_{gs,S1}>v_{th}$ and continues to increase, R_{S1} decreases, increasing i_{RS1}. Consequently, i_L gradually commutates to R_{S1}. At t_1, the entire i_L is conducted by R_{S1}.

During (t_1-t_2), initially, as $v_{gs,S1}$ continues to increase, R_{S1} decreases, increasing i_{RS1}, which increases i_{CS2}. Combined with lower $C_{oss,S2}$, it leads to a higher S_2's *dv/dt*. This triggers negative feedback: more i_g is diverted to $C_{gd,S1}$, causing (1) higher $i_{Cgd,S1}$, promoting $C_{gd,S1}$'s *dv/dt*; (2) lower $i_{Cgs,S1}$, slowing the increase in $v_{gs,S1}$, thereby slowing R_{S1} reduction and consequently slowing i_{RS1} increase. The slower increase in i_{RS1}, combined with a rapid increase in i_{CS1}, reduces the *di/dt* of $i_{d,S2}$ – initially positive, turning negative before t_3 - limiting *dv/dt* despite decreasing $C_{oss,S2}$. These combined effects enable $C_{gd,S1}$ to follow S_2's *dv/dt*.

During (t_2-t_3), $C_{gd,S1}$ is in the high-capacitance region, increasing rapidly as $v_{ds,S1}$ decreases; as $v_{ds,S2}$ approaches V_{DC}, $C_{oss,S2}$ remains low; as $i_{d,S2}$ remains significant, S_2's *dv/dt* remains significant. Consequently, $C_{gd,S1}$'s *dv/dt* has to remain significant. The insufficient i_g to maintain $C_{gd,S1}$'s *dv/dt* to track S_2's *dv/dt*, triggers further negative feedback – a drop in $v_{gs,S1}$. This boosts i_g, enhancing $i_{Cgd,S1}$, but also increases R_{S1}, and with decreasing $v_{ds,S1}$, leading to a rapid reduction in i_{RS1}, and consequently a lower $i_{d,S2}$, thereby a lower *dv/dt*. Meanwhile, $C_{gs,S1}$ supplies a pulse current to help discharge $C_{gd,S1}$ via S_1's channel. Together, these effects enable $C_{gd,S1}$'s *dv/dt* to follow S_2's.

After t_3, $C_{gs,S1}$ stops supplying charge and is instead charged by i_g, which charges $C_{gs,S1}$ and $C_{gd,S1}$ simultaneously. As $v_{gs,S1}$ further increases, R_{S1} decreases slowly, causing a slight rise in midpoint voltage and consequently a minor discharge of C_{S1} and charge

of C_{S2} via R_{S1}.

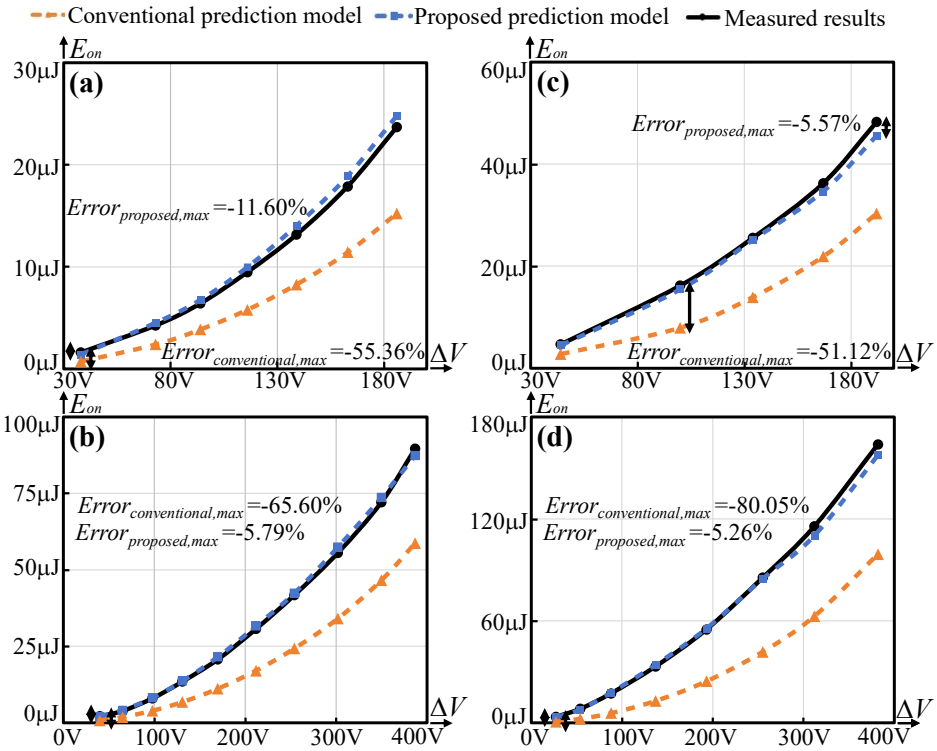


Figure 4. Comparison of measure results with calculated values with the proposed and conventional prediction models, when CREE C2M0080120D is used; **(a)** V_{DC}=200 V. **(b)** V_{DC}=400 V. Comparison of measure results with calculated values with the proposed and conventional prediction models, when CREE C2M0025120D is used; **(c)** V_{DC}=200 V. **(d)** V_{DC}=400 V.

Experimental validation

Enabled by the revealed insights into the switching behavior under the proposed paradigm, derivations grounded in both laws of charge conservation and energy conservation are presented in the *Methods*. The proposed E_{on} prediction model case-2 iZVS scenario is provided as a showcase. Experimental validation was performed by comparing measured results with calculated values obtained from both the proposed and conventional prediction models. Particularly, the proposed model incorporates previously unaccounted-for contributions, including the existence of the CC in iZVS process, dissipated energies incurred in the CC, and load inductor's role throughout the process – mechanisms beyond the recognition of the conventional model. As a result, the proposed prediction model achieves, on average, a 17-fold reduction in error compared to the conventional model.

Table 1. Detailed comparison of E_{on} measured results with calculated values using conventional and proposed prediction models, respectively

CREE 1.2Kv 2nd -gen SiC MOSFET (mΩ)	V_{DC} (V)	ΔV (V)	Measured results (μJ)	Calculated values using conventional prediction (μJ) (*Error*(conventional))	Calculated values using proposed prediction (μJ) (*Error*(proposed))	Error reduction *Error*(conventional)/ *Error*(proposed)
25	200	44	4.65	2.74 (-41.11%)	4.49 (-3.57%)	11.50
25	200	100	16.17	7.91 (-51.12%)	15.45 (-4.50%)	11.35
25	200	134	25.53	13.91 (-45.52%)	25.14 (-1.53%)	29.67
25	200	167	36.25	21.88 (-39.64%)	34.65 (-4.41%)	8.98
25	200	192	48.25	30.31 (-37.19%)	45.57 (-5.57%)	6.68
25	400	27	3.52	0.70 (-80.05%)	3.33 (-5.26%)	15.21
25	400	54	8.25	2.39 (-71.02%)	7.87 (-4.58%)	15.49
25	400	88	17.36	5.75 (-66.91%)	17.88 (2.95%)	22.66
25	400	137	33.21	12.91 (-61.11%)	34.14 (2.82%)	21.67
25	400	193	54.94	24.46 (-55.48%)	55.46 (0.94%)	58.75
25	400	255	85.42	41.79 (-51.08%)	84.67 (-0.88%)	57.75
25	400	312	115.68	62.76 (-45.75%)	110.10 (-4.82%)	9.49
25	400	382	163.86	99.24 (-39.44%)	157.42 (-3.93%)	10.02
80	200	38	1.59	0.709 (-55.36%)	1.40 (-11.60%)	4.77
80	200	73	4.24	2.38 (-43.78%)	4.50 (6.10%)	7.17
80	200	94	6.40	3.85 (-39.77%)	6.74 (5.40%)	7.37
80	200	116	9.47	5.78 (-38.91%)	9.96 (5.18%)	7.51
80	200	139	13.14	8.26 (-37.13%)	14.02 (6.70%)	5.54
80	200	163	17.88	11.42 (-36.11%)	18.87 (5.56%)	6.49
80	200	186	23.68	15.23 (-35.69%)	24.79 (4.69%)	7.61
80	400	40	2.17	0.748 (-65.60%)	2.05 (-5.79%)	11.33
80	400	65	3.89	1.82 (-53.14%)	4.06 (4.50%)	11.81
80	400	98	8.03	3.92 (-51.21%)	8.20 (2.12%)	24.13
80	400	131	13.50	6.77 (-49.82%)	13.66 (1.25%)	39.99
80	400	170	20.77	11.13 (-46.40%)	21.54 (3.73%)	12.45
80	400	212	30.73	17.05 (-44.53%)	31.65 (2.98%)	14.93
80	400	254	41.71	24.28 (-41.79%)	42.34 (1.51%)	27.70
80	400	302	55.54	34.10 (-38.61%)	57.40 (3.34%)	11.54
80	400	350	72.14	46.67 (-35.31%)	73.67 (2.11%)	16.70
80	400	387	89.57	58.75 (-34.41%)	87.35 (-2.49%)	13.85

Discussion

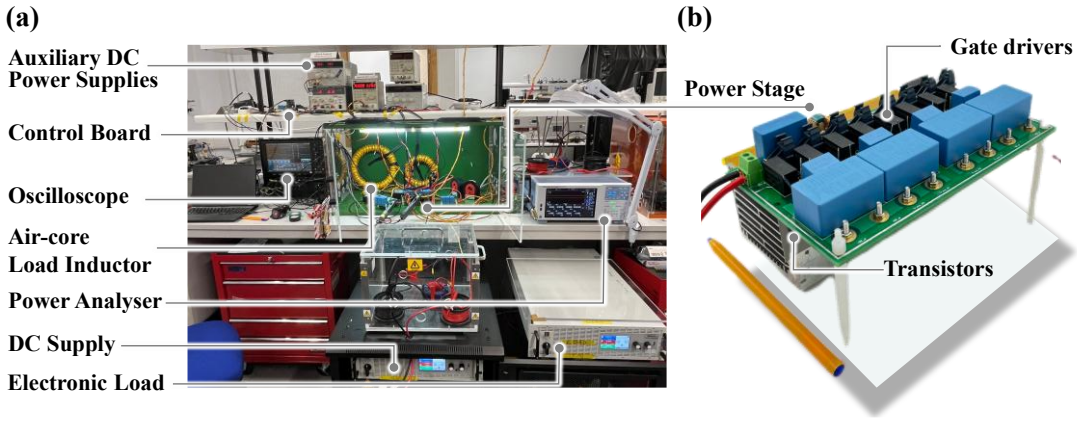
Grounded in the proposed unified equivalent-circuit modelling of S_1 and S_2, the proposed paradigm incorporates previously unrecognized factors into the causal analysis of switching behavior: the gate-driving variations in R_{S1}; coupling effects of S_2's dynamics; the influence of load current; the proposed definition of the switching-on criterion. Together, these considerations establish the proposed first-principles unified paradigm that yields unprecedented insights into transistor switching

phenomena.

Using this paradigm, the physical origins and fundamental mechanisms of ZVS, HS(ON), case-1 iZVS, and case-2 iZVS are revealed, including their distinct causes of the Miller platform. For the case-2 iZVS scenario, the proposed E_{on} prediction model achieves, on average, a 17-fold error reduction compared to the conventional model, exceeding the cumulative progress made in the field. Together, these insights and prediction advances demonstrate the proposed paradigm's transformative power.

At the heart of textbook-level foundations, the proposed paradigm explains switching phenomena solely from fundamental physical laws and, integrates transistor switching behaviors into circuit theory for the first time. It opens broad research directions and enables breakthroughs, exemplified by a 17-fold average error reduction in E_{on} prediction. As transistors are the fundamental building blocks of EEE, switching analysis is central to the operation and performance of EEE. Hence, the proposed paradigm is universally relevant: it informs and immediately drives advances in research, design and optimization. Its long-lasting impacts include stimulating follow-up studies and applications, spanning materials science,[13,14] semiconductor physics,[15,16] device engineering,[17,18] packaging,[19,20] reliability,[21,22] thermal management,[2,23] power electronics,[24,25] and even sustainability sciences,[2,26,27] standards,[28] economics,[29] policy[30,31] and education.[32,33] Together, the immediate and far-reaching impacts drive more sustainable EEE development - minimizing energy loss and carbon emissions, cutting cooling demand and water consumption, extending the lifetime and reducing material use and cost etc.

Extended Data Figure - Experimental platform



Extended Data Fig. 1. Experimental platform for E_{on} measurement, using a power electronic converter as the demonstrative example. **(a)** Overview picture of the entire experimental platform for E_{on} measurement. **(b)** Close-up picture of converter power stage.

Methods

Nomenclature

Table 2. NOMENCLATURE

Symbol	Unit	Definition
S_x	N/A	Switch number, e.g., S_1 denotes the upper switch and S_2 denotes the lower switch
R_{Sx}	Ω	Equivalent resistance of S_x
$R_{drift,Sx}$	Ω	Drift-region resistance of S_x
$R_{ch,Sx}$	Ω	Channel resistance of S_x
$v_{ds,Sx}$	V	Drain-source voltage of S_x
v_{GG}	V	Output voltage of the gate driver of S_1
$V_{gs,Sx}$	V	Gate-source voltage of S_x
$V_{th,Sx}$	V	Threshold voltage of S_x
$C_{oss,Sx}$	pF	Output capacitance of S_x
C_{Sx}	pF	Overall equivalent capacitance of S_x
$C_{gs,Sx}$	pF	Gate-source capacitance of S_x
$C_{gd,Sx}$	pF	Gate-drain capacitance of S_x
$C_{ds,Sx}$	pF	Drain-source capacitance of S_x
$C_{par,Sx}$	pF	The equivalent capacitance of the associated parallel capacitances of $C_{oss,Sx}$
$C_{par,gs,Sx}$	pF	The equivalent capacitance of the associated parallel capacitances of $C_{gs,Sx}$
$C_{par,ds,Sx}$	pF	The equivalent capacitance of the associated parallel capacitances of $C_{oss,ds,Sx}$
$C_{par,gd,Sx}$	pF	The equivalent capacitance of the associated parallel capacitances of $C_{oss,gd,Sx}$
$i_{d,Sx}$	A	The drain current of S_x
$i_{g,Sx}$	A	Gate driving current of S_x
i_L	A	Load current
i_{RSx}	A	Instantaneous current through R_{Sx}
i_{DC}	A	DC-source current
$i_{Cgs,Sx}$	A	Displacement current of $C_{gs,Sx}$
$i_{Cgd,Sx}$	A	Displacement current of $C_{gd,Sx}$
$i_{Cds,Sx}$	A	Displacement current of $C_{ds,Sx}$

$i_{C,Sx}$	A	Displacement current of C_{Sx}
V_{DC}	V	DC-link voltage
T_{diss}	ns	Duration in which the dissipated energy is incurred
$E_{gd,Sx}(v)$	μJ	The energy stored in $C_{gd,Sx}$ at drain-gate voltage of v
$E_{ds,Sx}(v)$	μJ	The energy stored in $C_{ds,Sx}$ at drain-source voltage of v
$E_{oss,Sx}(v)$	μJ	The energy stored in the output capacitance of S_x at drain-source voltage of v
$Q_{oss,Sx}(v)$	nC	The charge stored in the output capacitance of S_x at drain-source voltage of v
Error(proposed)	N/A	Error of the proposed model's prediction results compared to the measured results
Error(conventional)	N/A	Error of the conventional model's prediction results compared to the measured results

The equivalent non-linear resistance model, i.e., R_{S1} model adopted in the proposed paradigm

In the proposed paradigm, a unified equivalent-circuit model incorporating only equivalent non-linear resistance(s) and equivalent non-linear capacitances is proposed for the transistor. Taking the MOSFET as an example, a non-linear equivalent resistance is defined by Ohm's Law, $R_{S1}=v_{ds,S1}/i_{RS1}$ is proposed for S_1, where i_{RS1} includes all the current components except displacement currents across junction capacitances; R_{S1} incorporates all resistive components along the i_{RS1} paths, including equivalent resistance of body diode current path (during reverse conduction), JFET resistance, $R_{drift,S1}$, $R_{ch,S1}$ etc.

The R_{S1} model applies to all device types in both forward and reverse conduction operations, at any gate voltage. Its I-V characteristics in forward and reverse conduction follow the output characteristic and third-quadrant or body-diode characteristic of the transistor, respectively. At any given operating point, R_{S1} is given by the reciprocal of the slope of the line connecting the operating point and the origin of the I-V characteristic. The same R_{S2} model applies to S_2 - during shoot-through, an extra current component flows through R_{S2}.

The equivalent non-linear junction capacitances model adopted in the proposed paradigm

As the displacement current of $C_{gd,S1}$ flows through the drift region but not the channel, whereas that of $C_{ds,S1}$ flows through both, $C_{gd,S1}$ is modelled in parallel with $R_{drift,S1}$ whilst $C_{ds,S1}$ is modelled in parallel with R_{S1}. For simplicity, they are combined into a single lumped capacitance $C_{oss,S1}$ in parallel with R_{S1}. Their parallel capacitances

are grouped into another lumped capacitance in parallel with $C_{oss,S1}$, forming a single C_{S1} and C_{S2} for S_1 and S_2, respectively. The reverse-recovery effect is represented by a lumped non-linear capacitance, $C_{rr,S1}$ and $C_{rr,S2}$ in parallel with C_{S1} and C_{S2}, respectively. As no RR occurs in S_1 during its switching-ON, $C_{rr,S1}$ is zero (open circuit); when RR of S_2 is absent, $C_{rr,S2}$ is also zero.

Defining criterion for the Switching-ON event

Existing literature[32,33,41-43,51] lacks a clear criterion to identify switching-ON events, potentially leading to mis-interpretation in scenarios including crosstalk-induced gate spikes[42,51], multiple threshold crossings and multi-level gate-driving[52] etc. Hence, a criterion consistent with the proposed paradigm is introduced here - the onset is defined as the event that v_{gs} exceeds the threshold, triggering the initial dramatic reduction in R_{S1}. As all switching phenomena fundamentally originate from this $v_{gs,S1}$-driven R_{S1} reduction, the initial rapid drop of R_{S1} from infinity is identified as the starting point of the causal reasoning.

Case-2 iZVS E_{on} prediction model derivation based on the switching behavior revealed using the proposed paradigm

Derivation of the proposed E_{on} prediction model using the law of charge conservation

In all the switching-ON scenarios, since the energy dissipated in the ESR of C_{S1} is negligible compared to that along the i_{RS1} paths[50,53] it is valid to assume that the entire $E_{on,S1}$ is incurred in R_{S1}. Hence, $E_{on,S1}$ is given by

$$E_{on,S1} = \int_{switching-ON} v_{ds,S1}(t) i_{RS1}(t) dt \,. \tag{1}$$

In case-2 iZVS process, as vast majority of the energy dissipation during S_1's switching-ON is incurred during ($t_0 - t_3$), it is valid to assume the dissipated energy incurred during ($t_0 - t_3$) is $E_{on,S1}$.

Applying Kirchhoff's Current Law (KCL) at S_1's drain terminal, yielding

$$i_{RS1}(t) = i_{d,S1}(t) + i_{C_{gd},S1}(t) + i_{C_{ds},S1}(t) + i_{par,C_{gd},S1}(t) + i_{par,C_{ds},S1}(t) \,. \tag{2}$$

Substitute (2) into (1), yielding the expression of $E_{on,S1}$, given by

$$\begin{aligned} E_{on,S1} = & \int_{switching-ON} v_{ds,S1}(t) i_{d,S1}(t) dt + \int_{switching-ON} v_{ds,S1}(t) i_{C_{gd},S1}(t) dt + \int_{switching-ON} v_{ds,S1}(t) i_{C_{ds},S1}(t) dt \\ & + \int_{switching-ON} v_{ds,S1}(t) i_{par,C_{gd},S1}(t) dt + \int_{switching-ON} v_{ds,S1}(t) i_{par,C_{ds},S1}(t) dt \end{aligned} \,. \tag{3}$$

As $v_{gs,S1}$ during ($t_0 - t_3$) is negligibly small compared to ΔV, it can be approximated as a constant V_{gp}; ΔV-V_{gp} can be approximated to ΔV and 0 V-V_{gp} can be approximated to 0 V. Therefore, the summation of 2nd, 3rd, 4th and 5th terms of the expression of $E_{on,S1}$ could be approximated as

$$\begin{aligned}
&\int_{switching-ON} v_{ds,S1}(t) i_{C_{gd},S1}(t)dt + \int_{switching-ON} v_{ds,S1}(t) i_{C_{ds},S1}(t)dt + \int_{switching-ON} v_{ds,S1}(t) i_{C_{par,gd},S1}(t)dt + \int_{switching-ON} v_{ds,S1}(t) i_{C_{par,ds},S1}(t)dt \\
&= \underbrace{E_{oss,S1}(\Delta V)}_{Energy\ dissipated\ by\ output\ capacitance\ of\ S1} + \underbrace{\int_{0-V_{gp}}^{\Delta V - V_{gp}} v_{ds,S1} C_{par,gd,S1}(v_{gd,S1})dv_{gd,S1}}_{Energy\ dissipated\ by\ capacitance\ in\ parallel\ with\ C_{gd,S1}} + \underbrace{\int_{0}^{\Delta V} v_{ds,S1} C_{par,ds,S1} dv_{ds,S1}}_{Energy\ dissipated\ by\ capacitance\ in\ parallel\ with\ C_{ds,S1}} \\
&\approx \underbrace{E_{oss,S1}(\Delta V)}_{Energy\ dissipated\ by\ output\ capacitance\ of\ S1} + \underbrace{\int_{0}^{\Delta V} v_{ds,S1} C_{par,gd,S1}(v_{gd,S1})dv_{gd,S1}}_{Energy\ dissipated\ by\ capacitance\ in\ parallel\ with\ C_{gd,S1}} + \underbrace{\int_{0}^{\Delta V} v_{ds,S1} C_{par,ds,S1} dv_{ds,S1}}_{Energy\ dissipated\ by\ capacitance\ in\ parallel\ with\ C_{ds,S1}} \\
&= \underbrace{E_{oss,S1}(\Delta V)}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1's\ output\ capacitance} + \underbrace{\frac{1}{2} C_{par,S1} \Delta V^2}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1's\ paralleled\ capacitance}
\end{aligned} \quad .(4)$$

Besides, the charge obtained by $C_{gd,S2}$, $C_{ds,S2}$ and the charge obtained by their paralleled capacitances during ($t_0 - t_3$), are given by

$$\begin{aligned}
\Delta Q_{S2} &= \int_{switching-ON} i_{Cgd,S2}(t)dt + \int_{switching-ON} i_{Cds,S2}(t)dt \\
&= \int_{V_{DC}-\Delta V-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{gd,S2} dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} \quad ; \\
&\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2} dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2} dv_{ds,S2} \\
&= Q_{oss,S2}(V_{DC}) - Q_{oss,S2}(V_{DC} - \Delta V)
\end{aligned} \quad (5)$$

$$\begin{aligned}
&\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} C_{par,gd,S2}(v_{gd})dv_{gd} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds})dv_{ds} \\
&\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2}(v_{gd})dv_{gd} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}(v_{ds})dv_{ds} \\
&= \left[\int_{0}^{V_{DC}} C_{par,gd,S2}(v_{gd})dv_{gd} - \int_{0}^{V_{DC}-\Delta V} C_{par,gd,S2}(v_{gd})dv_{gd}\right] + \left[\int_{0}^{V_{DC}} C_{par,ds,S2}(v_{ds})dv_{ds} - \int_{0}^{V_{DC}-\Delta V} C_{par,ds,S2}(v_{ds})dv_{ds}\right] \\
&= C_{par,gd,S2}\Delta V + C_{par,ds,S2}\Delta V \\
&= C_{par,S2}\Delta V
\end{aligned} \quad .(6)$$

Applying Kirchhoff's Voltage Law (KVL) across the loop incorporating the DC source, S1 and S2, yielding

$$V_{DC} = v_{ds,S1}(t) + v_{ds,S2}(t). \quad (7)$$

Applying KCL at the source terminal of S_2, yielding

$$i_{DC}(t) = i_{d,S2}(t) - i_L(t) = i_{RS2}(t) + i_{C,S2}(t) - i_L(t). \quad (8)$$

Hence, the 1st term of the expression of $E_{on,S1}$ could be derived as

$$\begin{aligned}
&\int_{switching-ON} v_{ds,S1}(t) i_{d,S1}(t)dt \\
&= \int_{switching-ON} V_{DC} i_{DC}(t)dt - \int_{switching-ON} v_{ds,S2}(t)\left[i_{d,S2}(t) - i_L(t)\right]dt \\
&= V_{DC} \int_{switching-ON} \left[i_{RS2}(t) + i_{C,S2}(t) - i_L(t)\right]dt - \int_{switching-ON} v_{ds,S2}(t) i_{d,S2}(t)dt + \int_{switching-ON} v_{ds,S2}(t) i_L(t)dt
\end{aligned} \quad . \quad (9)$$

where

$$\int_{switching-ON} v_{ds,S2}(t)i_{d,S2}(t)dt = \underbrace{\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2}C_{gd,S2}\left(v_{gd,S2}\right)dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{ds,S2}\left(v_{ds,S2}\right)dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}} + \underbrace{\int_{(V_{DC}-\Delta V)-(-V_{EE})}^{V_{DC}-(-V_{EE})} v_{gd,S2}C_{par,gd,S2}\left(v_{gd,S2}\right)dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}\text{'s paralleled capacitance}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{ds,S2}\left(v_{ds,S2}\right)dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}\text{'s paralleled capacitance}} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through} \quad .(10)$$

(10) could be approximated to

$$\begin{aligned}
&\int_{switching-ON} v_{ds,S2}(t)i_{d,S2}(t)dt \\
&\approx \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S1}C_{gd,S2}\left(v_{gd,S2}\right)dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{ds,S2}\left(v_{ds,S2}\right)dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}} + \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{gd,S1}C_{par,gd,S2}\left(v_{gd,S2}\right)dv_{gd,S2}}_{Energy\ stored\ by\ C_{gd,S2}\text{'s paralleled capacitance}} \\
&+ \underbrace{\int_{V_{DC}-\Delta V}^{V_{DC}} v_{ds,S2}C_{par.ds,S2}\left(v_{ds,S2}\right)dv_{ds,S2}}_{Energy\ stored\ by\ C_{ds,S2}\text{'s paralleled capacitance}} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through} \\
&= \underbrace{E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)}_{Energy\ stored\ by\ C_{oss,S2}} + \underbrace{\frac{1}{2}(C_{par,gd,S2}+C_{par,ds,S2})\left[{V_{DC}}^2-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through} \\
&= \underbrace{E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)}_{Energy\ stored\ by\ C_{oss,S2}} + \underbrace{\frac{1}{2}C_{par,S2}\left[{V_{DC}}^2-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipation\ in\ S2\ due\ to\ shoot-through}
\end{aligned} \quad .(11)$$

It is important to note that

$$\int_{switching-ON} i_{C,S2}(t)dt = \Delta Q_{S2} + C_{par,S2}\Delta V \ . \quad (12)$$

Combining (3)(4)(5)(6)(7)(8)(9)(10)(11)(12), yielding the $E_{on,S1}$ prediction model derived from the perspective of charge conservation, given by

$$\begin{aligned}
E_{on,S1} \approx\ & \underbrace{V_{DC}\left[\int_{switching-ON} i_{RS2}(t)dt + \Delta Q_{S2} + C_{par,S2}\Delta V - \int_{switching-ON} i_L(t)dt\right]}_{Energy\ provided\ by\ DC\ source\ to\ the\ half-bridge} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_L(t)dt}_{Energy\ provided\ by\ the\ overall\ AC-link\ impedance\ to\ the\ half-bridge} \\
& - \underbrace{\left[E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)\right]}_{Energy\ stored\ by\ output\ capacitance\ of\ S2} - \underbrace{\int_{switching-ON} v_{ds,S2}(t)i_{RS2}(t)dt}_{Energy\ dissipated\ in\ S2\ due\ to\ shoot-through} - \underbrace{\frac{1}{2}C_{par,S2}\left[{V_{DC}}^2-(V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} \\
& + \underbrace{E_{oss,S1}(\Delta V) + \frac{1}{2}C_{par,S1}\Delta V^2}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1\text{'s output capacitance and paralleled capacitance}}
\end{aligned} \quad .(13)$$

Derivation of the proposed E_{on} prediction model using the law of energy conservation

The half-bridge during the S1's switching-ON process is taken as the study object. For simplicity reasons, the analysis is limited to (t_0 – t_3) as vast majority of the energy dissipation during S_1's switching-ON is incurred during this interval. According to the law of energy conservation, the overall energy initially stored in the study object, minus the various dissipated energies incurred during the switching-ON process and the energy delivered to the external circuit, yields the remaining stored energy at the end of the interval. The general mathematical expression is given by

$$E_{initial} - E_{dissipated} - E_{delivered} = E_{final}\,, \tag{14}$$

where $E_{initial}$ denotes the overall energy stored in the study object at the initial instant; $E_{dissipated}$ denotes the total energy losses during S_1's switching-ON process, including but not limited to switching-ON loss and ESR losses; $E_{delivered}$ denotes the energy delivered to the external circuit; E_{final} denotes the total energy stored in the study object at the end of the process. Among them, $E_{initial}$ and E_{final} are given by

$$\begin{aligned}
E_{initial} &= \left[E_{gd,S1}\left(\Delta V - v_{gs,S1}\left(t_0\right)\right) + E_{ds,S1}\left(\Delta V\right) + \frac{1}{2}C_{par,gd,S1}\left(\Delta V - v_{gs,S1}\left(t_0\right)\right)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\
&+ \left[E_{gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}\left(t_0\right)\right) + E_{ds,S2}\left(V_{DC} - \Delta V\right) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}\left(t_0\right)\right)^2 + \frac{1}{2}C_{par,ds,S2}\left(V_{DC} - \Delta V\right)^2 \right]; \\
&= \left[E_{gd,S1}\left(\Delta V - V_{th,S1}\right) + E_{ds,S1}\left(\Delta V\right) + \frac{1}{2}C_{par,gd,S1}\left(\Delta V - V_{th,S1}\right)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\
&+ \left[E_{gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}\left(t_0\right)\right) + E_{ds,S2}\left(V_{DC} - \Delta V\right) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - \Delta V - v_{gs,S2}\left(t_0\right)\right)^2 + \frac{1}{2}C_{par,ds,S2}\left(V_{DC} - \Delta V\right)^2 \right]
\end{aligned} \tag{15}$$

$$\begin{aligned}
E_{final} &= \left[E_{gd,S1}\left(-V_{th,S1}\right) + E_{ds,S1}\left(0\right) + \frac{1}{2}C_{par,gd,S1}\left(0 - V_{th,S1}\right)^2 + \frac{1}{2}C_{par,ds,S1}0^2 \right] \\
&+ \left[E_{gd,S2}\left(V_{DC} - v_{gs,S2}\left(t_0\right)\right) + E_{ds,S2}\left(V_{DC}\right) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - v_{gs,S2}\left(t_0\right)\right)^2 + \frac{1}{2}C_{par,ds,S2}{V_{DC}}^2 \right],
\end{aligned} \tag{16}$$

where $v_{gs,S1}(t_0)=V_{th,S1}$. As both $v_{gs,S1}$ and $v_{gs,S2}$ during the process are negligibly small compared to ΔV and V_{DC}-ΔV, both $v_{gs,S1}$ and $v_{gs,S2}$ can be approximated to 0 V, yielding

$$\begin{aligned}
E_{initial} &\approx \left[E_{gd,S1}\left(\Delta V\right) + E_{ds,S1}\left(\Delta V\right) + \frac{1}{2}C_{par,gd,S1}\left(\Delta V\right)^2 + \frac{1}{2}C_{par,ds,S1}\Delta V^2 \right] \\
&+ \left[E_{gd,S2}\left(V_{DC} - \Delta V\right) + E_{ds,S2}\left(V_{DC} - \Delta V\right) + \frac{1}{2}C_{par,gd,S2}\left(V_{DC} - \Delta V\right)^2 + \frac{1}{2}C_{par,ds,S2}\left(V_{DC} - \Delta V\right)^2 \right]; \\
&= \left[E_{oss,S1}\left(\Delta V\right) + \frac{1}{2}C_{par,S1}\left(\Delta V\right)^2 \right] + \left[E_{oss,S2}\left(V_{DC} - \Delta V\right) + \frac{1}{2}C_{par,S2}\left(V_{DC} - \Delta V\right)^2 \right]
\end{aligned} \tag{17}$$

$$\begin{aligned}
E_{final} &\approx E_{gd,S2}\left(V_{DC}\right) + E_{ds,S2}\left(V_{DC}\right) + \frac{1}{2}C_{par,gd,S2}{V_{DC}}^2 + \frac{1}{2}C_{par,ds,S2}{V_{DC}}^2 \\
&= E_{oss,S2}\left(V_{DC}\right) + \frac{1}{2}C_{par,S2}{V_{DC}}^2
\end{aligned}. \tag{18}$$

During S_1's iZVS process , the energy dissipation caused by ESR is negligible compared to $E_{dissipated}$. The dominant dissipated energy arises from $E_{on,S1}$ and the dissipated energy within S_2 due to the shoot-through effect. Hence, $E_{dissipated}$ can be approximated as consisting only of these two components, namely

$$E_{dissipated} \approx E_{on,S1} + E_{dissipated,S2}\,, \tag{19}$$

where $E_{dissipated,S2} = \underbrace{\int_{switching-ON} v_{ds,S2}\left(t\right) i_{RS2}\left(t\right) dt}_{Energy\ \ dissipated\ \ \text{in}\ \ S2\ \ due\ \ to\ \ shoot-through}$. (20)

Regarding the energy delivered to the external circuit, $E_{delivered}$ could be obtained as

$$E_{delivered} = -\left(W_{DC} + W_L\right) \tag{21}$$

where W_{DC} and W_L denote the work done by the DC source and load inductor to the study object, respectively.

In order to obtain W_{DC}, it is important to obtain the total charge obtained by the DC source, denoted ΔQ_{DC} during the process. Applying KCL at S_2's source terminal, yielding

$$i_{DC}(t) = i_{d,S2}(t) - i_L(t) = i_{C,S2}(t) + i_{RS2}(t) - i_L(t). \tag{22}$$

Integrating both sides of (22), yielding

$$\Delta Q_{DC} = \int_{switching-ON} i_{DC}(t)dt = \int_{switching-ON} i_{C,S2}(t)dt + \int_{switching-ON} i_{R,S2}(t)dt - \int_{switching-ON} i_L(t)dt, \tag{23}$$

where

$$\begin{aligned}
&\int_{switching-ON} i_{C,S2}(t)dt \\
&= \int_{switching-ON} i_{Cgd,S2}(t)dt + \int_{switching-ON} i_{Cds,S2}(t)dt + \int_{switching-ON} i_{Cpar,gd,S2}(t)dt + \int_{switching-ON} i_{Cpar,ds,S2}(t)dt \\
&= \int_{switching-ON} C_{gd,S2}\frac{dv_{gd,S2}}{dt}dt + \int_{switching-ON} C_{ds,S2}\frac{dv_{ds,S2}}{dt}dt \\
&+ \int_{switching-ON} C_{par,gd,S2}\frac{dv_{gd,S2}}{dt}dt + \int_{switching-ON} C_{par,ds,S2}\frac{dv_{ds,S2}}{dt}dt \\
&= \int_{V_{DC}-\Delta V-v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{gd,S2}dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}dv_{ds,S2} \\
&+ \int_{V_{DC}-\Delta V-v_{gs,S2}(t_0)}^{V_{DC}-v_{gs,S2}(t_3)} C_{par,gd,S2}dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}dv_{ds,S2}
\end{aligned} \tag{24}$$

As $v_{gs,S2}$ is negligibly small compared to V_{DC}-ΔV during the process, (24) could be approximated to

$$\begin{aligned}
&\int_{switching-ON} i_{C,S2}(t)dt \\
&\approx \int_{V_{DC}-\Delta V}^{V_{DC}} C_{gd,S2}dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{ds,S2}dv_{ds,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,gd,S2}dv_{gd,S2} + \int_{V_{DC}-\Delta V}^{V_{DC}} C_{par,ds,S2}dv_{ds,S2} \\
&= Q_{oss,S2}(V_{DC}) - Q_{oss,S2}(V_{DC}-\Delta V) + \left(C_{par,gd,S2} + C_{par,ds,S2}\right)\Delta V \\
&= \Delta Q_{S2} + C_{par,S2}\Delta V
\end{aligned} \tag{25}$$

Therefore, ΔQ_{DC} is obtained as

$$\Delta Q_{DC} \approx \Delta Q_{S2} + C_{par,S2}\Delta V + \int_{switching-ON} i_{RS2}(t)dt - \int_{switching-ON} i_L(t)dt. \tag{26}$$

Hence, W_{DC} is obtained as

$$\begin{aligned}
W_{DC} &= \int_{switching-ON} V_{DC}i_{DC}(t)dt = V_{DC}\Delta Q_{DC} \\
&= V_{DC}\left[\Delta Q_{S2} + C_{par,S2}\Delta V + \int_{switching-ON} i_{RS2}(t)dt - \int_{switching-ON} i_L(t)dt\right].
\end{aligned} \tag{27}$$

In terms of the work done by the load inductor W_L, it could be obtained as

$$W_L = \int_{switching-ON} v_L(t)i_L(t)dt = \int_{switching-ON} v_{ds,S2}(t)i_L(t)dt \tag{28}$$

Substituting (27) and (28) into (21), yielding

$$E_{delivered} = -\left(W_{DC} + W_L\right) =$$
$$= -V_{DC}\left[\Delta Q_{S2} + C_{par,S2}\Delta V + \int_{switching-ON} i_{RS2}(t)\,dt - \int_{switching-ON} i_L(t)\,dt\right] - \int_{switching-ON} v_{ds,S2}(t)\,i_L(t)\,dt \quad (29)$$

Substituting (17),(18),(19),(20),(29) into (14), yielding the $E_{on,S1}$ prediction model, given by

$$E_{on,S1} \approx \underbrace{V_{DC}\left[\int_{switching-ON} i_{RS2}(t)dt + \Delta Q_{S2} + C_{par,S2}\Delta V - \int_{switching-ON} i_L(t)\,dt\right]}_{Energy\ provided\ by\ DC\ source\ to\ the\ half-bridge} + \underbrace{\int_{switching-ON} v_{ds,S2}(t)\,i_L(t)\,dt}_{Energy\ provided\ by\ the\ load\ inductor\ to\ the\ half-bridge}$$
$$-\underbrace{\left[E_{oss,S2}(V_{DC}) - E_{oss,S2}(V_{DC}-\Delta V)\right]}_{Energy\ stored\ by\ output\ capacitance\ of\ S2} - \underbrace{\int_{switching-ON} v_{ds,S2}(t)\,i_{RS2}(t)\,dt}_{Energy\ dissipated\ in\ S2\ due\ to\ shoot-through} - \underbrace{\frac{1}{2}C_{par,S2}\left[V_{DC}{}^2 - (V_{DC}-\Delta V)^2\right]}_{Energy\ stored\ by\ the\ paralleled\ capacitance\ of\ S2} \quad (30)$$
$$+ \underbrace{E_{oss,S1}(\Delta V) + \frac{1}{2}C_{par,S1}\Delta V^2}_{Energy\ dissipated\ in\ RS1\ due\ to\ discharge\ of\ S1's\ output\ capacitance\ and\ paralleled\ capacitance}$$

It is noteworthy that (30) is identical to (13), indicating that the proposed prediction model derived from the law of energy conservation is fundamentally equivalent to that obtained from the law of charge conservation, both grounded in the physical insights of the proposed paradigm. For the first time, this equivalence cross-validates the proposed E_{on} prediction model and establishes a foundational unification of the laws of charge and energy conservation within a closed-form framework. It showcases the universal applicability of both fundamental laws to the analysis of transistor switching, and simultaneously validates the proposed paradigm in achieving a true and intrinsic unification of switching behavior with classical circuit theory and fundamental physical laws, such as energy conservation.

Summary of switching-ON scenarios

Table 3. Summary of switching behaviors in switching scenarios

Switching scenario	ZVS	HS(ON)	Case-1 iZVS	Case-2 iZVS
1st phase	CC	CC	CC	CC
2nd phase	N/A	VF and RR	VF	VF
Miller platform existence	NO	YES	YES	YES
1st sub-phase of Miller platform; associated physical origin	N/A	(t_1-t_2); high $C_{oss,S2}$ and low $i_{d,S2}$, causing low dv/dt, thus low $i_{Cgd,S1}$	(t_1-t_2); high $C_{oss,S2}$ and low $i_{d,S2}$, causing low dv/dt; as $C_{gd,S1}$ is also low, $i_{Cgd,S1}$ is low	(t_1-t_2); medium-to-low $C_{oss,S2}$ and high $i_{d,S2}$, causing high dv/dt; as $C_{gd,S1}$ is medium-to-high, $i_{Cgd,S1}$ is high
2nd sub-phase of Miller platform; associated physical origin	N/A	(t_2-t_3); medium $C_{oss,S2}$ and high $i_{d,S2}$, causing medium dv/dt; given low $C_{gd,S1}$, low-to-medium $i_{Cgd,S1}$ results	(t_2-t_3); medium $C_{oss,S2}$ and high $i_{d,S2}$, causing medium dv/dt; given low-to-medium $C_{gd,S1}$, low-to-medium $i_{Cgd,S1}$ results	(t_2-t_3); low $C_{oss,S2}$ and decreasing $i_{d,S2}$, causing high-to-low dv/dt; as $C_{gd,S1}$ is high, $i_{Cgd,S1}$ is high-to-low

3rd sub-phase of Miller platform; associated physical origin	N/A	(t_3-t_4); $\lvert dR_{S1}/R_{S1}\rvert > \lvert dv_{ds\_S1}/v_{ds\_S1}\rvert$ causes decreasing i_{RS1}, and thus a decreasing $i_{d,S2}$, leading to a decreasing dv/dt, whilst $C_{gd,S1}$ increases, causing nearly unchanged $i_{Cgd,S1}$ at medium level	(t_3-t_4); medium-to-low $C_{oss,S2}$ and decreasing $i_{d,S2}$, causing decreasing dv/dt; given increasing $C_{gd,S1}$, nearly unchanged $i_{Cgd,S1}$ results
4th sub-phase of Miller platform; associated physical origin	N/A	(t_4-t_5); high $C_{gd,S1}$ and medium dv/dt, causing high $i_{Cgd,S1}$	(t_4-t_6); high $C_{gd,S1}$ and medium dv/dt, causing high $i_{Cgd,S1}$

Data availability

The data presented in this study are available in this manuscript.

Code availability

No custom code was used in this study.

Reference

1 Wang, P., Sanusi, B. N., Zsurzsan, T. G., Andersen, M. A. E. & Ouyang, Z. Three-Dimensional Interconnect LLC-DCX Converter for Datacenter Application. *IEEE Transactions on Power Electronics* **40**, 15306-15315, doi:10.1109/TPEL.2025.3574041 (2025).

2 van Erp, R., Soleimanzadeh, R., Nela, L., Kampitsis, G. & Matioli, E. Co-designing electronics with microfluidics for more sustainable cooling. *Nature* **585**, 211-216, doi:10.1038/s41586-020-2666-1 (2020).

3 Link, S., Stephan, A., Speth, D. & Plötz, P. Rapidly declining costs of truck batteries and fuel cells enable large-scale road freight electrification. *Nature Energy* **9**, 1032-1039, doi:10.1038/s41560-024-01531-9 (2024).

4 Huang, Z., Yang, T., Giangrande, P., Galea, M. & Wheeler, P. Technical Review of Dual Inverter Topologies for More Electric Aircraft Applications. *IEEE Transactions on Transportation Electrification* **8**, 1966-1980, doi:10.1109/TTE.2021.3113606 (2022).

5 Li, S. L. *et al.* Controlling diverse robots by inferring Jacobian fields with deep networks. *Nature* **643**, 89-95, doi:10.1038/s41586-025-09170-0 (2025).

6 Shen, Y., Wang, H., Shen, Z., Yang, Y. & Blaabjerg, F. A 1-MHz Series Resonant DC–DC Converter With a Dual-Mode Rectifier for PV Microinverters. *IEEE Transactions on Power Electronics* **34**, 6544-6564, doi:10.1109/TPEL.2018.2876346 (2019).

7 Chen, Z., Guerrero, J. M. & Blaabjerg, F. A Review of the State of the Art of Power Electronics for Wind Turbines. *IEEE Transactions on Power Electronics* **24**, 1859-1875, doi:10.1109/TPEL.2009.2017082 (2009).

8 Xia, Y., Wei, W., Yu, M., Wang, X. & Peng, Y. Power Management for a Hybrid AC/DC Microgrid With Multiple Subgrids. *IEEE Transactions on Power Electronics* **33**, 3520-3533, doi:10.1109/TPEL.2017.2705133 (2018).

9 Zhao, B. *et al.* High-Frequency-Link DC Transformer Based on Switched Capacitor for Medium-Voltage DC Power Distribution Application. *IEEE Transactions on Power Electronics* **31**, 4766-

4777, doi:10.1109/TPEL.2015.2483543 (2016).

10 Zhao, B., Song, Q., Liu, W. & Xiao, Y. Next-Generation Multi-Functional Modular Intelligent UPS System for Smart Grid. *IEEE Transactions on Industrial Electronics* **60**, 3602-3618, doi:10.1109/TIE.2012.2205356 (2013).

11 Bardeen, J. & Brattain, W. H. The Transistor, A Semi-Conductor Triode. *Physical Review* **74**, 230-231, doi:10.1103/PhysRev.74.230 (1948).

12 Committee, N. P. *The Nobel Prize in Physics 1956 – Press Release*, <https://www.nobelprize.org/prizes/physics/1956/summary/> (1956).

13 Cao, R. *et al.* Softening of the optical phonon by reduced interatomic bonding strength without depolarization. *Nature* **634**, 1080-1085, doi:10.1038/s41586-024-08099-0 (2024).

14 Cheema, S. S. *et al.* Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors. *Nature* **604**, 65-71, doi:10.1038/s41586-022-04425-6 (2022).

15 Burroughes, J. H., Jones, C. A. & Friend, R. H. New semiconductor device physics in polymer diodes and transistors. *Nature* **335**, 137-141, doi:10.1038/335137a0 (1988).

16 Kang, H. & Udrea, F. True Material Limit of Power Devices—Applied to 2-D Superjunction MOSFET. *IEEE Transactions on Electron Devices* **65**, 1432-1439, doi:10.1109/TED.2018.2808181 (2018).

17 Si, M. *et al.* A ferroelectric semiconductor field-effect transistor. *Nature Electronics* **2**, 580-586, doi:10.1038/s41928-019-0338-7 (2019).

18 He, Q. *et al.* Numerical Simulation and Analytical Modeling of Multichannel AlGaN/GaN Devices. *IEEE Transactions on Electron Devices* **71**, 1710-1717, doi:10.1109/TED.2024.3359165 (2024).

19 Janabi, A. *et al.* Substrate Embedded Power Electronics Packaging for Silicon Carbide mosfets. *IEEE Transactions on Power Electronics* **39**, 9614-9628, doi:10.1109/TPEL.2024.3396779 (2024).

20 Mu, W., Janabi, A., Hu, B., Shillaber, L. & Long, T. Liquid Metal Fluidic Connection and Floating Die Structure for Ultralow Thermomechanical Stress of SiC Power Electronics Packaging. *IEEE Transactions on Power Electronics* **39**, 7808-7814, doi:10.1109/TPEL.2024.3379121 (2024).

21 Zhang, Y. *et al.* Power Cycling Testing for Power Semiconductor Switches: Methods, Standards, Limitations, and Outlooks. *IEEE Transactions on Power Electronics*, 1-21, doi:10.1109/TPEL.2025.3595180 (2025).

22 Xu, C. *et al.* Full-Time Junction Temperature Extraction of IGCT Based on Electrothermal Model and TSEP Method for High-Power Applications. *IEEE Transactions on Industrial Electronics* **68**, 47-58, doi:10.1109/TIE.2019.2962423 (2021).

23 Wang, H., Zhu, R., Wang, H., Liserre, M. & Blaabjerg, F. A Thermal Modeling Method Considering Ambient Temperature Dynamics. *IEEE Transactions on Power Electronics* **35**, 6-9, doi:10.1109/TPEL.2019.2924723 (2020).

24 Zhang, Y. *et al.* Wide-bandgap semiconductors and power electronics as pathways to carbon neutrality. *Nature Reviews Electrical Engineering* **2**, 155-172, doi:10.1038/s44287-024-00135-5 (2025).

25 Zhao, H. *et al.* A Single- and Three-Phase Grid Compatible Converter for Electric Vehicle On-Board Chargers. *IEEE Transactions on Power Electronics* **35**, 7545-7562, doi:10.1109/TPEL.2019.2956653 (2020).

26 Vauche, L., Guillemaud, G., Lopes Barbosa, J.-C. & Di Cioccio, L. Cradle-to-Gate Life Cycle Assessment (LCA) of GaN Power Semiconductor Device. *Sustainability* **16** (2024).

27 Spejo, L., Thekemuriyil, T. & Minamisawa, R. Estimation of Energy-Saving Potential Using Commercial SiC Power Converters. *Energies* **17**, 4570, doi:10.3390/en17184570 (2024).

28 (IEC), I. E. C. *Semiconductor devices – Discrete devices – Part 8: Field-effect transistors*. (2010).

29 Research, T. M. *Wide Band Gap Semiconductor Market Outlook 2030*, <https://www.transparencymarketresearch.com/wide-band-gap-semiconductor-market.html> (

30 Commission, E. AdvanSiC - Advances in Cost-Effective HV SiC Power Devices for Europe's Medium Voltage Grids.

31 PowerAmerica. *The U.S. Department of Energy has committed $32 million over five years to support dozens of projects managed by PowerAmerica.*, <https://poweramericainstitute.org/poweramerica/> (

32 Baliga, B. J. Fundamentals of Power Semiconductor Devices. *Springer* (2008).

33 Erickson, R. W. & Maksimovic, D. Fundamentals of Power Electronics. *Springer*.

34 NEWS, B. *Musk says Tesla to use humanoid robots next year*, <https://www.bbc.co.uk/news/articles/cz5reve8476o> (

35 Electricity 2024. *International Energy Agency*.

36 Zhao, B., Song, Q. & Liu, W. Experimental Comparison of Isolated Bidirectional DC–DC Converters Based on All-Si and All-SiC Power Devices for Next-Generation Power Conversion Application. *IEEE Transactions on Industrial Electronics* **61**, 1389-1393, doi:10.1109/TIE.2013.2258304 (2014).

37 Zhao, S., Yang, X., Wu, X. & Liu, G. Investigation on Creep-Fatigue Interaction Failure of Die-Attach Solder Layers in IGBTs Under Power Cycling. *IEEE Transactions on Power Electronics* **40**, 7261-7274, doi:10.1109/TPEL.2025.3530991 (2025).

38 Mou, D., Luo, Q., Li, J., Wei, Y. & Sun, P. Five-Degree-of-Freedom Modulation Scheme for Dual Active Bridge DC–DC Converter. *IEEE Transactions on Power Electronics* **36**, 10584-10601, doi:10.1109/TPEL.2021.3056800 (2021).

39 Everts, J., Krismer, F., Keybus, J. V. d., Driesen, J. & Kolar, J. W. Optimal ZVS Modulation of Single-Phase Single-Stage Bidirectional DAB AC–DC Converters. *IEEE Transactions on Power Electronics* **29**, 3954-3970, doi:10.1109/TPEL.2013.2292026 (2014).

40 Wang, H. & Li, Z. A PWM LLC Type Resonant Converter Adapted to Wide Output Range in PEV Charging Applications. *IEEE Transactions on Power Electronics* **33**, 3791-3801, doi:10.1109/TPEL.2017.2713815 (2018).

41 Li, X. *et al.* A SiC Power MOSFET Loss Model Suitable for High-Frequency Applications. *IEEE Transactions on Industrial Electronics* **64**, 8268-8276, doi:10.1109/TIE.2017.2703910 (2017).

42 Zhang, Z. *et al.* Methodology for Wide Band-Gap Device Dynamic Characterization. *IEEE Transactions on Power Electronics* **32**, 9307-9318, doi:10.1109/TPEL.2017.2655491 (2017).

43 Xiong, Y., Sun, S., Jia, H., Shea, P. & Shen, Z. J. New Physical Insights on Power MOSFET Switching Losses. *IEEE Transactions on Power Electronics* **24**, 525-531, doi:10.1109/TPEL.2008.2006567 (2009).

44 Qian, C., Wang, Z., Xin, G. & Shi, X. Datasheet Driven Switching Loss, Turn-ON/OFF Overvoltage, di/dt, and dv/dt Prediction Method for SiC MOSFET. *IEEE Transactions on Power Electronics* **37**, 9551-9570, doi:10.1109/TPEL.2022.3152529 (2022).

45 Zhang, Z. Characterization and Realization of High Switching-speed Capability of SiC Power Devices in Voltage Source Converter. *University of Tennessee, Knoxville*.

46 Kasper, M., Burkart, R. M., Deboy, G. & Kolar, J. W. ZVS of Power MOSFETs Revisited. *IEEE Transactions on Power Electronics* **31**, 8063-8067, doi:10.1109/TPEL.2016.2574998 (2016).

47 Perera, N. *et al.* Hard-Switching Losses in Power FETs: The Role of Output Capacitance. *IEEE Transactions on Power Electronics* **37**, 7604-7616, doi:10.1109/TPEL.2021.3130831 (2022).

48 Li, X. *et al.* in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD).* 231-234.

49 Qi, J. *et al.* Temperature Dependence of Dynamic Performance Characterization of 1.2-kV SiC Power mosfets Compared With Si IGBTs for Wide Temperature Applications. *IEEE Transactions on Power Electronics* **34**, 9105-9117, doi:10.1109/TPEL.2018.2884966 (2019).

50 Li, X. *et al.* Achieving Zero Switching Loss in Silicon Carbide MOSFET. *IEEE Transactions on Power Electronics* **34**, 12193-12199, doi:10.1109/TPEL.2019.2906352 (2019).

51 Zhang, Z., Wang, F., Tolbert, L. M. & Blalock, B. J. Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration. *IEEE Transactions on Power Electronics* **29**, 1986-1997, doi:10.1109/TPEL.2013.2268058 (2014).

52 Shelton, E., Rogers, D. & Palmer, P. in *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe).* 1-10.

53 Jafari, A. *et al.* Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies. *IEEE Transactions on Power Electronics* **35**, 12595-12600, doi:10.1109/TPEL.2020.2990628 (2020).

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Competing Interests Statement

The authors declare no competing interests.

Supplementary Information

N/A