Hardware-Efficient Neural Network Implementation: A Power-Accuracy Trade-off Analysis for Quantized Classification Neural Network

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***Abstract*—This paper presents a comprehensive analysis of power-accuracy trade-offs in quantized neural network implementations for Application-Specific Integrated Circuit (ASIC) design. A three-layer feedforward neural network trained on the Wisconsin Breast Cancer dataset is implemented using a complete design flow from PyTorch model training to ASIC synthesis. The study evaluates 14-bit, 16-bit, and 18-bit uniform post-training quantization schemes and their impact on classification accuracy, power consumption, and area utilization. A lookup table (LUT) based sigmoid activation function is employed to reduce computational complexity in hardware implementation. The design is synthesized using Cadence Stratus High-Level Synthesis (HLS) tool targeting 500 MHz operation frequency on GPDK 45nm technology. Results demonstrate that 18-bit quantization achieves 95.6% accuracy with 2.44 mW power consumption and 183,963 GE (Gate Equivalent) area, representing an optimal balance between computational precision and hardware efficiency. The 16-bit implementation provides a reasonable compromise with 89.4% accuracy, 1.819 mW power, and 162,379 GE area, while the 14-bit version shows significant accuracy degradation to 64.9% despite lower power consumption of 1.924 mW.**

***Index Terms*—Neural networks, quantization, ASIC implementation, power optimization, hardware acceleration, breast cancer classification**

I. Introduction

THE proliferation of artificial intelligence applications in resource-constrained environments has driven significant research into efficient neural network implementations. Healthcare applications, particularly medical diagnosis systems, require high accuracy while operating under strict power and area constraints for portable and implantable devices. The implementation of neural networks on Application-Specific Integrated Circuits (ASICs) offers superior performance and energy efficiency compared to general-purpose processors, making them ideal for edge computing applications in medical diagnostics.

Quantization has emerged as a critical technique for reducing the computational and memory requirements of neural networks while maintaining acceptable accuracy levels. Post-training quantization, in particular, offers the advantage of applying compression techniques to pre-trained models without requiring extensive retraining procedures. However, the selection of appropriate quantization bit-widths involves complex trade-offs between accuracy preservation, hardware complexity, power consumption, and implementation area.

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This work addresses the challenge of optimal quantization bit-width selection for neural network ASIC implementations through a systematic analysis of power-accuracy trade-offs. The research contributes a complete design methodology from algorithmic development to physical implementation, demonstrating the practical implications of quantization choices on real hardware metrics. The study focuses on breast cancer classification as a representative medical diagnosis application requiring high reliability and efficiency.

The main contributions of this work include: (1) A comprehensive power-accuracy analysis across multiple quantization bit-widths for neural network ASIC implementation, (2) An efficient LUT-based sigmoid activation function implementation optimized for hardware synthesis, (3) A complete design flow from PyTorch model training to ASIC physical design using industry-standard tools, and (4) Quantitative analysis of area, power, and accuracy trade-offs to guide practical implementation decisions.

II. Related Work

A. Neural Network Quantization Techniques

Quantization techniques for neural networks have been extensively studied to address the computational and memory limitations of deep learning models. Jacob et al. [1] introduced quantization-aware training methods that simulate quantization effects during the training process, achieving minimal accuracy loss even with 8-bit representations. However, post-training quantization approaches offer greater flexibility for existing trained models.

Nagel et al. [2] presented a comprehensive analysis of post-training quantization methods, demonstrating that careful calibration of quantization parameters can maintain high accuracy with minimal computational overhead. Their work established the theoretical foundation for uniform quantization schemes employed in this study.

B. Hardware Implementation of Neural Networks

The hardware implementation of neural networks has evolved from traditional digital signal processors to specialized accelerators and ASICs. Chen et al. [3] demonstrated early ASIC implementations of convolutional neural networks, establishing design methodologies that have influenced subsequent research in the field.

More recent work by Sze et al. [4] provided a comprehensive survey of efficient processing techniques for deep neural networks, highlighting the importance of co-design approaches that consider both algorithmic and hardware optimization. Their analysis emphasizes the critical role of activation function implementation in overall system efficiency.

C. LUT-Based Activation Functions

Lookup table implementations of nonlinear activation functions have gained attention as an efficient alternative to direct mathematical computation. Maher [5] analyzed various approximation techniques for sigmoid and tanh functions, demonstrating that LUT-based approaches can achieve high accuracy with significantly reduced hardware complexity.

Wang et al. [6] specifically addressed sigmoid function approximation in neural network accelerators, showing that 256-entry LUTs provide sufficient precision for most classification tasks while minimizing area and power overhead.

D. Medical Diagnosis Applications

Neural network applications in medical diagnosis have shown significant promise, particularly for cancer detection and classification. Wolberg et al. [7] originally established the Wisconsin Breast Cancer dataset used in this study, demonstrating the effectiveness of machine learning approaches for diagnostic applications.

Recent work by Kourou et al. [8] surveyed machine learning applications in cancer prognosis and prediction, highlighting the importance of efficient implementations for practical clinical deployment. Their analysis emphasizes the need for high-accuracy, low-power solutions suitable for point-of-care devices.

III. Methodology

A. Dataset and Model Architecture

The Wisconsin Breast Cancer dataset from scikit-learn is employed for this study, containing 569 samples with 30 features describing cell nuclei characteristics. The dataset is split into training (80%) and testing (20%) sets using a fixed random seed for reproducible results.

The neural network architecture consists of three fully connected layers with ReLU activation functions in the hidden layers and sigmoid activation in the output layer. The network topology is configured as 30-64-32-1, where the input layer accepts 30 features, followed by hidden layers of 64 and 32 neurons, and a single output neuron for binary classification.

B. PyTorch Model Training

The baseline floating-point model is implemented using PyTorch framework. The network architecture is defined as follows:

```
class BreastCancerClassifier(nn.Module):
    def __init__(self, input_dim):
        super(BreastCancerClassifier, self).__init__()
        self.layer1 = nn.Linear(input_dim, 64)
        self.layer2 = nn.Linear(64, 32)
        self.layer3 = nn.Linear(32, 1)
        self.relu = nn.ReLU()
        self.sigmoid = nn.Sigmoid()
```

Training is performed using the Adam optimizer with a learning rate of 0.001 and binary cross-entropy loss function. The model is trained for 100 epochs with a batch size of 16. Input features are normalized using standard scaling with zero mean and unit variance.

C. Quantization Methodology

Post-training uniform quantization is applied to the trained model using MATLAB HDL Coder. Three quantization schemes are evaluated: 14-bit, 16-bit, and 18-bit fixed-point representations. The quantization process involves:

1) **Weight and Bias Quantization**: All network parameters are converted to fixed-point representation with the specified bit-width.
2) **Activation Quantization**: Intermediate layer outputs are quantized to maintain consistent precision throughout the network.
3) **Scaling Factor Optimization**: Quantization scaling factors are optimized to minimize the quantization error while preventing overflow conditions.

The normalization operation is implemented as:

$$\text{input} = (\text{input} - \text{scaler\_mean}) \cdot \text{scaler\_std\_rec} \quad (1)$$

where `scaler_std_rec` represents the reciprocal of the standard deviation to avoid costly division operations in hardware.

D. LUT-Based Sigmoid Implementation

A 256-entry lookup table is generated for sigmoid function approximation covering the input range [-6, 6] with linear interpolation:

```
x_min = -6; % Min input value for LUT
x_max = 6; % Max input value for LUT
num_points = 256; % Number of LUT entries
x_values = linspace(x_min, x_max, num_points);
sigmoid_values = 1 ./ (1 + exp(-x_values));
```

The LUT is implemented as a persistent variable in MATLAB and mapped to RAM during synthesis. Input values outside the LUT range are clipped to the nearest boundary values to ensure robust operation.

E. MATLAB Hardware Description

The forward propagation algorithm is implemented in MATLAB using HDL-compatible syntax. Key implementation features include:

1) **Persistent Variable Management**: Model parameters and LUT data are loaded once and stored as persistent variables to minimize memory access overhead.
2) **Explicit Loop Implementation**: ReLU activation functions are implemented using explicit conditional loops to ensure proper HDL translation.

TABLE I
CLASSIFICATION ACCURACY COMPARISON

Implementation	Accuracy (%)	Accuracy Loss (%)
PyTorch (Baseline)	97.3	-
18-bit Quantized	95.6	1.7
16-bit Quantized	89.4	7.9
14-bit Quantized	64.9	32.4

TABLE II
POWER AND AREA COMPARISON

Bit-Width	Power (mW)	Area (GE)	Power Density (μW/GE)
14-bit	1.924	145,277	13.24
16-bit	1.819	162,379	11.20
18-bit	2.440	183,963	13.27

3) **Fixed-Point Arithmetic**: All computations are performed using single-precision fixed-point arithmetic compatible with hardware synthesis.

F. Hardware Synthesis and Implementation

The MATLAB function is synthesized using Cadence Stratus HLS 24.01 targeting 500 MHz operation frequency. The synthesis process employs:

1) **Technology Library**: GPDK 45nm standard cell library
2) **Synthesis Tool**: Cadence Genus 21 for logic synthesis
3) **Power Analysis**: Cadence Joules 21 for power estimation
4) **Interface Engine**: Full interface engine for complete I/O management

The design flow includes automatic FSM generation, resource scheduling, and register allocation optimized for the target frequency constraint.

IV. RESULTS AND ANALYSIS

A. Accuracy Analysis

Table I presents the classification accuracy results for different quantization bit-widths compared to the baseline PyTorch model.

The results demonstrate that 18-bit quantization maintains high accuracy with only 1.7% degradation compared to the floating-point baseline. The 16-bit implementation shows moderate accuracy loss of 7.9%, which may be acceptable for many applications. However, 14-bit quantization results in significant accuracy degradation of 32.4%, indicating insufficient precision for the complexity of the classification task.

B. Power and Area Analysis

Table II summarizes the power consumption and area utilization for each quantized implementation.

The power consumption shows a non-monotonic relationship with bit-width, with 16-bit implementation achieving the lowest power consumption of 1.819 mW. This counter-intuitive result can be attributed to the optimization algorithms used in the synthesis tool, which may find more efficient implementations for certain bit-width configurations.

Area utilization increases monotonically with bit-width, as expected, with the 18-bit implementation requiring 26.6% more area than the 14-bit version. The power density analysis reveals that 16-bit quantization achieves the most efficient power per unit area ratio.

C. Power-Accuracy Trade-off Analysis

The analysis reveals three distinct operating regions:

1) **Low Precision Region (14-bit)**: Characterized by low power consumption but unacceptable accuracy loss for medical applications.
2) **Balanced Region (16-bit)**: Offers reasonable accuracy with minimal power consumption, suitable for power-constrained applications where moderate accuracy degradation is acceptable.
3) **High Precision Region (18-bit)**: Maintains near-optimal accuracy at the cost of increased power consumption, appropriate for applications requiring high reliability.

D. Performance Metrics

The synthesized designs achieve the target operating frequency of 500 MHz across all quantization bit-widths. The critical path analysis indicates that the matrix multiplication operations in the fully connected layers constitute the primary timing bottleneck, while the LUT-based sigmoid implementation introduces minimal delay overhead.

Throughput analysis shows that each inference operation requires 3 clock cycles, resulting in a maximum inference rate of 166.7 million classifications per second. This performance exceeds the requirements for most real-time medical diagnosis applications.

V. DISCUSSION

A. Quantization Impact on Model Behavior

The significant accuracy degradation observed in 14-bit quantization can be attributed to insufficient precision for representing the small weight variations critical to the decision boundary in the feature space. Analysis of the quantization noise distribution reveals that the 14-bit representation introduces systematic bias in the intermediate layer outputs, leading to misclassification of borderline cases.

The 16-bit implementation maintains reasonable accuracy while providing substantial hardware savings compared to 18-bit quantization. This configuration represents a practical compromise for applications where moderate accuracy reduction is acceptable in exchange for improved power efficiency.

B. LUT Implementation Efficiency

The 256-entry LUT implementation for sigmoid activation proves highly effective, introducing negligible accuracy loss compared to direct mathematical computation. The LUT approach eliminates the need for expensive exponential function computation, resulting in significant area and power savings. The chosen LUT size provides sufficient resolution for the application while maintaining reasonable memory requirements.

C. Synthesis Tool Impact

The non-monotonic power consumption pattern across bit-widths highlights the importance of synthesis tool optimization in determining final implementation metrics. The Cadence Stratus HLS tool appears to achieve better optimization for 16-bit arithmetic, possibly due to alignment with native datapath widths in the target technology library.

D. Medical Application Considerations

For medical diagnosis applications, the 18-bit quantization scheme appears most appropriate due to its high accuracy preservation. The 2.44 mW power consumption remains within acceptable limits for battery-powered medical devices, while the area overhead can be justified by the reliability requirements of healthcare applications.

VI. Conclusion and Future Work

This work presents a comprehensive analysis of power-accuracy trade-offs in quantized neural network ASIC implementations for medical diagnosis applications. The study demonstrates that quantization bit-width selection significantly impacts both accuracy and hardware implementation metrics, requiring careful consideration of application requirements.

The key findings include: (1) 18-bit quantization provides the optimal balance of accuracy and hardware efficiency for high-reliability applications, (2) 16-bit quantization offers a practical compromise for power-constrained scenarios, and (3) 14-bit quantization results in unacceptable accuracy degradation for medical diagnosis tasks.

The LUT-based sigmoid implementation proves highly effective, providing hardware-efficient activation function computation with minimal accuracy impact. The complete design flow from PyTorch to ASIC demonstrates the feasibility of deploying quantized neural networks in practical hardware implementations.

Future work will investigate adaptive quantization schemes that employ different bit-widths for different network layers, potentially achieving better power-accuracy trade-offs. Additionally, the integration of quantization-aware training methods may further improve the accuracy of low-precision implementations. The extension of this methodology to larger networks and different application domains represents another promising research direction.

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