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A Power and Area Efficient CMOS Bandgap Reference Circuit with an Integrated Voltage-Reference Branch

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Abstract

This work presents a compact and low power bandgap voltage reference design using self-biased current mirror circuit. This design eliminates the standard complementary-to-absolute-temperature (CTAT) bipolar device in the voltage-reference branch, reducing the bipolar area by 20 percent. Instead, the design shares the same bipolar device in the main CTAT branch for generating the reference voltage. An additional benefit of eliminating the voltage-reference branch is the reduction of total power consumption by approximately 30 percent. This novel topology reduces power and area of the core bandgap reference circuit without compromising temperature drift performance. Designed, fabricated and functionally tested in a $0.6\mu m$ CMOS process. The simulation result shows the temperature coefficient of this design is $6.3\,ppm/^{\circ}C$ for a temperature range of $-40\,^{\circ}C$ to $125\,^{\circ}C$. This bandgap reference design occupies a silicon area of $0.018\ mm^2$ and draws an average quiescent current of $2\ \mu A$ from a supply voltage of $3.3 - 5V$. The simulated flicker voltage noise is $4.34\ \mu V/\sqrt{Hz}$ at $10\ Hz$.

1 Introduction

Voltage reference circuits are an essential block in most applications from a simple integrated circuit (IC) to a large System-on-Chip (SoC) ranging from purely digital circuits to mixed-signal applications such as Analog to Digital converters (ADCs), Digital to Analog converters (DACs), phase locked loops (PLLs), low noise amplifiers (LNAs), digital multimeters, battery chargers, low-power IoT sensor nodes, portable data acquisition systems and so on. Since the first bandgap reference (BGR) circuit introduced by Robert Widlar Widlar (1970), BGR has been widely used since it provides a well-defined voltage reference with a very weak dependence on process, voltage and temperature. Most analog and mixed-signal circuits also require a current reference that sets the internal bias current for the circuits. The BGR can also provide a reference current directly which has positive temperature co-efficient (PTC). For most bias currents, a PTC reference current is sufficient. For circuits demanding more stable current reference can achieve so with some additional circuits Ji et al. (2017).

Figure 1, shows two type of traditional BGR circuit: (a) one using operational amplifier (Op-Amp) and (b) using self-biased current mirror circuit Wu et al. (2007). The principle of operations is the same in both cases where the nodes A and B are forced to be the same by (a) the Op-Amp or (b) the self-biased current mirror. Forcing same node voltages makes the voltage drop across R_1 be exactly difference between the base-to-emitter voltage V_{BE} of the two bi-polar transistor provided that, the size of the transistor $Q_1 = N \cdot Q_2$. The voltage across the resistor R_1 produces a proportional-to-absolute-temperature (PTAT) voltage, which is multiplied with a suitable constant and added to V_{BE} of Q_3 to generate a stable voltage Allen and Holberg (2012) as follows:

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} \cdot V_T \cdot \ln(N) \tag{1}$$

Where, V_{REF} is the output reference voltage and V_T is the thermal voltage of the semiconductor.

Typically, Op-Amp based BGR is preferred over self-biased for better power supply rejection (PSR) performance and lower supply requirement. Although the self-biased BGR may have a lower performance in those two metrics, it is a simpler design consuming less area and power while achieving almost similar

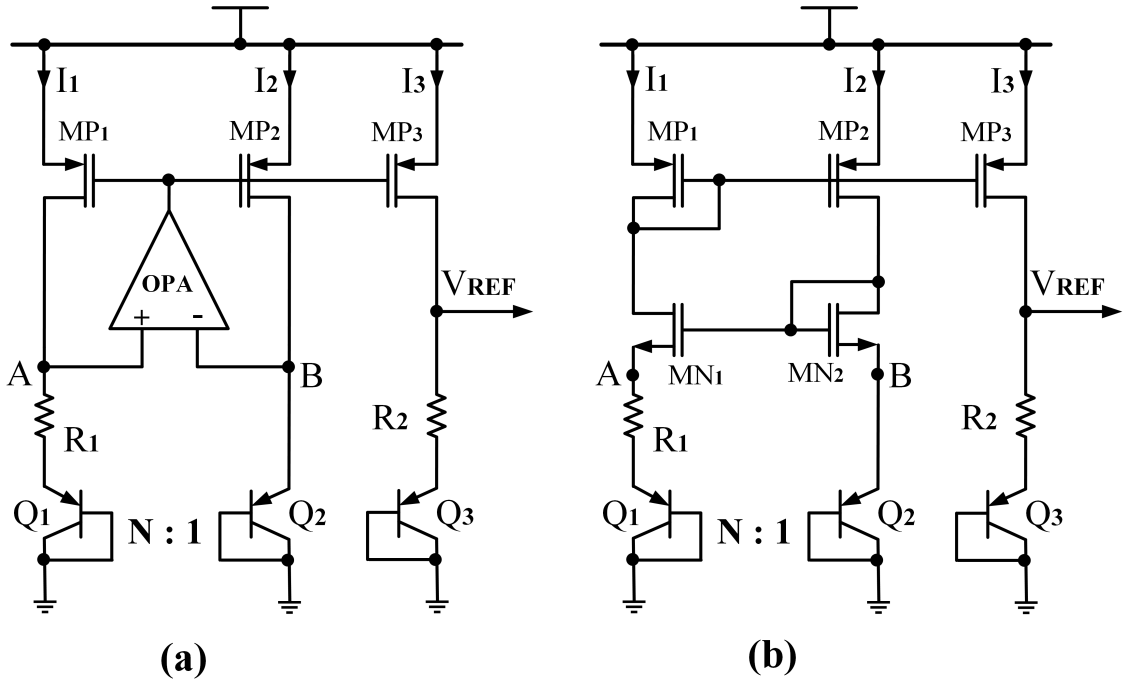

Figure 1: Traditional BGR circuits; (a) using Op-Amp, (b) using self-biased current mirror

temperature drift performance. In most IC or SoC designs the self-biased BGR performance may suffice allowing less design time, lower risk, lower area and power which is always desirable for any SoC design. Moreover, the PSR in a self-biased BGR can be improved by using cascode current mirrors Wu et al. (2007) or symmetric biasing of both the branches Lam and Ki (2010). In this paper an improved self-biased based bandgap reference circuit has been proposed which further lowers the area and power of the reference circuit while preserving the temperature coefficient performance. The improved circuit generates the reference voltage without using the separate reference-voltage branch as in the traditional self-biased BGR. This paper is organized as follows: Section II describes the proposed architecture of the BGR along with its design procedure and circuit implementation. Simulation and measurement results are presented in Section III, followed by a conclusion in Section IV.

2 Proposed bandgap reference

Figure 2 shows the core part of the proposed bandgap reference circuit. As evident from the figure, this modified circuit avoids a bi-polar device in the reference branch. Here the BJT Q_2 used for dual purpose; firstly, it helps for generating a PTAT voltage across resistor R_1 and secondly, voltage across this adds with voltage across R_2 for generating reference voltage V_{REF} at the output node. This elegant modification in the traditional self-biased current mirror based BGR provides some great advantages particularly in power consumption and silicon area of the core circuit. These advantages are;

- Since we eliminate the standard voltage-reference branch, the bi-polar device area reduces by approximately 20 percent and the PMOS current-mirror area reduces by approximately 30 percent. Note that, bi-polar devices and the current mirrors are a significant portion of the core BGR area.,
- One-third of the total current is reduced in the core BGR and therefore one-third reduction in power consumption in the core BGR circuit as well.

The self-biased current mirror uses two P-MOS transistor MP_1, MP_2 and two N-MOS transistor MN_1, MN_2. These four transistor forms the self-biased feedback loop which makes the node voltages at A and B equal.The second branch of the circuit uses a single bi-polar device Q_2, which produces a CTAT voltage V_{BE2} across the BJT Q_2, whereas, in the first branch, four parallel BJTs are connected with a resistor R_1 in series. As both the node voltages at A and B are same and current flowing through both the BJTs are

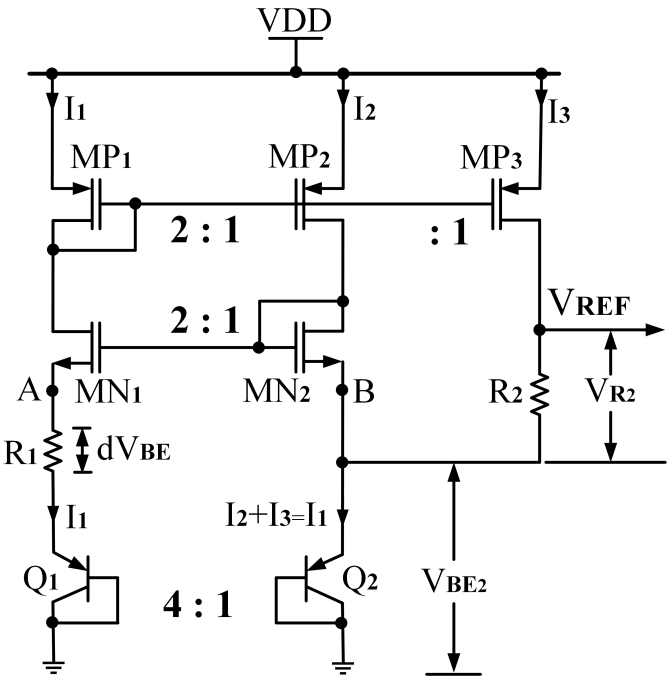

Figure 2: Core part of the proposed self-biased current mirror based BGR

same, a PTAT voltage $dV_{BE} = V_{BE2} - V_{BE1}$ produced across resistor R_1, where V_{BE1} is voltage across the four parallel BJTs Q_1.

As V_{BE2} is a CTAT voltage and dV_{BE} is a PTAT voltage, so addition of CTAT voltage with some appropriate constant multiplication of the PTAT voltage will generate a reference voltage which will be zero temperature coefficients at a reference temperature.

The power-supply rejection (PSR) performance does not change significantly from the traditional self-biased BGR. The PSR can be improved by using cascode current mirrors Wu et al. (2007) or symmetric biasing of both the branches Lam and Ki (2010). Our proposed integration of reference branch will also work with symmetric biasing as shown in Lam and Ki (2010).

2.1 Design Procedure of improved BGR

In this section, the expressions to calculate the resistance values of the core BGR circuit for a current value will be shown. For a low power BGR, Q_1 and Q_2 were each biased with $1\mu A$. Given the bias current, R_1 can be expressed as:

$$R_1 = \frac{V_T \cdot \ln(4)}{I_1} \tag{2}$$

Where V_T is the thermal voltage of the semiconductor and its value at room temperature is approximately $25.8\ mV$. Applying the values of V_T and I_1 in Equation 2, R_1 evaluates to $35.76\ k\Omega$.

The reference voltage can be calculated by combining the voltage across the BJT Q_2 (CTAT in nature) and voltage across the resistor R_2 (PTAT in nature) as;

$$V_{REF} = V_{BE2} + V_{R2} \tag{3}$$

Where, V_{R2} is the PTAT voltage across resistor R_2 and can be expressed as:

$$V_{R2} = \frac{R_2}{R_1} \cdot V_T \cdot \ln(4) \tag{4}$$

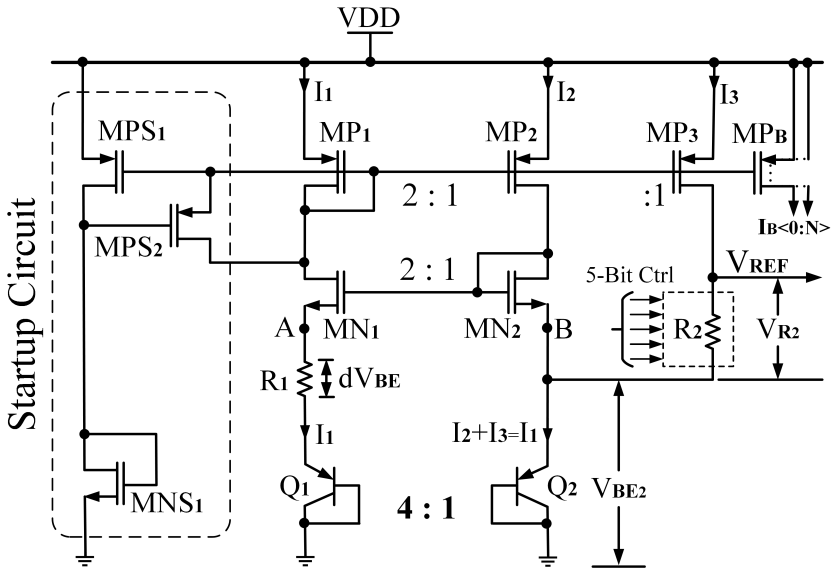

Figure 3: Complete schematic diagram of the proposed BGR circuit

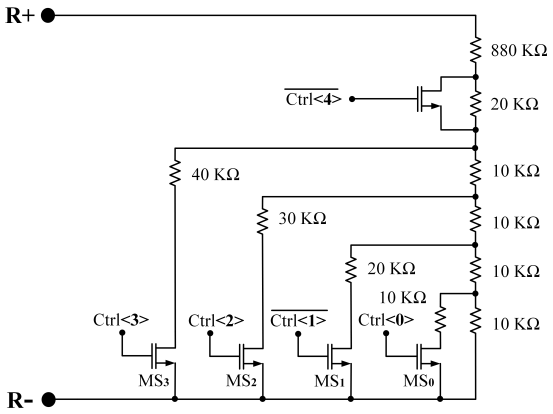

Figure 4: Implementation of the 5-bit trimmable resistor R_2

Equation 3 can be rewritten as;

$$V_{REF} = V_{BE2} + \alpha \cdot V_T \tag{5}$$

Where, $\alpha = (R_2/R_1) \cdot \ln(4)$ is a constant.

For calculating zero temperature coefficient reference voltage at the reference temperature, the derivative of V_{REF} should be zero.

$$\frac{dV_{REF}}{dT} = \frac{d(V_{BE2} + \alpha.V_T)}{dT} = 0 \tag{6}$$

Using $\partial V_{BE2}/\partial T = -1.6mV/°C$ and $\partial V_T/\partial T = 85\ \mu V/°C$ Allen and Holberg (2012) in Equation 6, α evaluates to 18.82 and using Equation 5, V_{REF} evaluats to $1.155\ V$

For this modified architecture the current flowing through resistor R_2 is half of that current flowing in resistor R_1. So the constant α for this circuit will be;

$$\alpha = \frac{R_2}{2R_1} \cdot \ln(4) \tag{7}$$

Applying α and R_1 values in Equation 7, R_2 evaluates to $971\ k\Omega$.

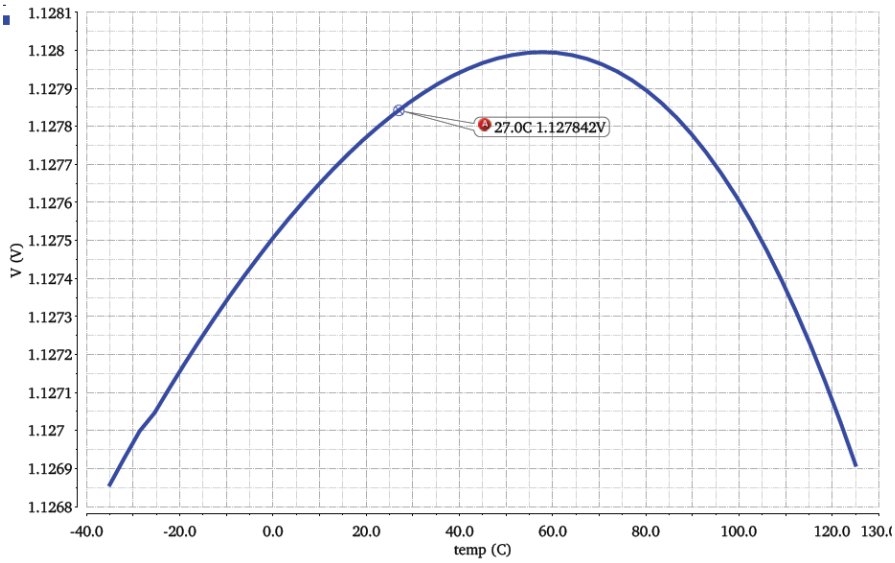

Figure 5: Simulation result: VREF-vs-Temperature (Tempco).

2.2 Implementation of complete BGR

Figure 3 shows the complete implementation of the proposed BGR. MP_{1-3}, MN_{1-2}, R_{1-2}, and Q_{1-2} forms the core part of the bandgap and the value of the resistors are calculated in the previous sub-section. MPS_{1-2} and MNS_1 form the start up circuitry since there are two stable states. MP_B transistors are the PTAT current sources for biasing internal circuits. MN_{1-2} are biased in the deep-sub-threshold (weak inversion) region to provide the maximum g_m/I_D for given bias current Harrison and Charles (2003), which ensures the voltages of node A and B are only offset by the V_T mismatch of the MN_{1-2} and the systematic offset of I_1 and I_2. Typically, $g_m/I_D > 20$ ensures deep-sub-threshold operation. Please note that, this offset is similar to a offset in a Op-Amp based BGR where the input referred offset of the Op-Amp is dominated by the V_T mismatch of the input pair of the differential amplifier which also biased in deep-subthreshold region for low-power application.

PMOS current mirrors MP_{1-3} and MP_B are biased in saturation region where g_m/I_D is typically less than 10 Harrison and Charles (2003), to ensure the minimum systematic offset in I_1 and I_2. As mentioned before, this systematic offset can be minimized by using cascode current mirrors Wu et al. (2007) or symmetric biasing of both the branches Lam and Ki (2010). The unit sizes of Q_1 and Q_2 are chosen to be the minimum allowable in the implemented technology and the ratio between them is chosen such that the area of Q_{1-2} and R_{1-2} is minimized. For the implemented technology, the BJT ratio $4:1$ was found to be optimum.

A high-sheet-rho poly resistor ($R_{sheet} = 3.76\,k\Omega/sq$) was chosen to minimize the resistor area. In order to trim the output temperature coefficient (TC) of the BGR after fabrication, R_2 is a 5-bit programmable resistor is used as shown in Figure 4, which is programmed through an Inter-IC Communication (I2C) protocol with a range of $890 - 940\,k\Omega$. Each of the programmable resistor in R_2 is made of series-parallel combination of unit resistors of $20\,k\Omega$. R_1 is also constructed from combination of same unit resistors so they can be matched in layout with R_2. During startup, MPS_2 ensures that the current mirror is pulled out of the zero-V_{gs} state and once the circuit is operating normally ($V_{REF} \approx 1.155$), the voltage drop across MNS_1 should be high enough that it shuts OFF MPS_2. MNS_1 needs to be sized such that there is no leakage current during normal operation. MPS_1 provides a trickle current for MNS_1 and MNS_1 is sized with a very long length transistor to provide a large voltage drop for the minimum amount of current. For layout, special care is taken to match MP_{1-3}, MN_{1-2}, R_{1-2}, and Q_{1-2} which affects the TC directly.

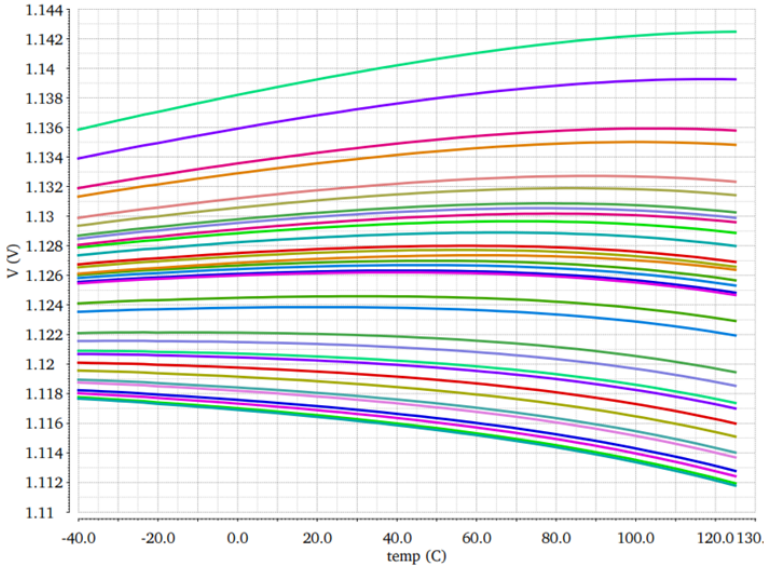

Figure 6: Simulation result: VREF versus Temperature for different R_2 trims.

Parameters	Value
Technology	0.06 μm CMOS
Power Supply Voltage	$3.3 - 5V$
Temperature range	$-40\ ^{\circ}C$ to $125\ ^{\circ}C$
Reference voltage V_{REF})	$1.15V$
Temperature coefficient	$6.3\ ppm/^{\circ}C$
Line regulation	$16mV/V$
Flicker noise @ 10Hz	4.34 $\mu V/\sqrt{Hz}$
PSR @ DC/1Hz	40dB/35dB

Table 1: Summary of the Simulation Results.

3 Simulation and measurement results

3.1 Simulation results

The improved self-biased bandgap reference has been simulated with a commercially available Spectre simulator using the Process Design Kit (PDK) from the foundry. The first order temperature drift performance is simulated over the entire temperature range of $-40^{\circ}C$ to $125^{\circ}C$. A simulated reference voltage (V_{REF}) versus temperature curve is shown in Figure 5.

The calculated temperature coefficient (TC) from the figure is $6.3\ ppm/\ ^{\circ}C$. Figure 6, shows the parametric plot of VREF versus temperature at all 32 (5-bit) trimming resistance values. The simulated PSR performance at room temperature for the improved BGR circuit is about 40 dB at DC and 35 dB at 1 kHz. The noise performance at room temperature is $4.34\ \mu V/\sqrt{Hz}$ at 10 Hz and $1.47\ \mu V/\sqrt{Hz}$ at 100Hz which is dominated by the flicker noise of current-mirrors, MN_{1-2} (46 percentage) and MP_{1-3} (52 percentage). The simulated average quiescent current is about $2\ \mu A$ over the temperature range of $-40\ ^{\circ}C$ to $125\ ^{\circ}C$. Table 1 summarizes the simulation parameters in and its corresponding simulated values.

3.2 Test setup and measurement results

This work has been fabricated in a commercially available $0.6\ \mu$m CMOS technology. The proposed work has been integrated to provide bias voltage to other blocks inside the chip. Figure 7 shows the chip micrograph with highlighting the proposed BGR and its corresponding layout view. The whole BGR consumes $0.018\ mm^2$ of silicon area inside the chip.

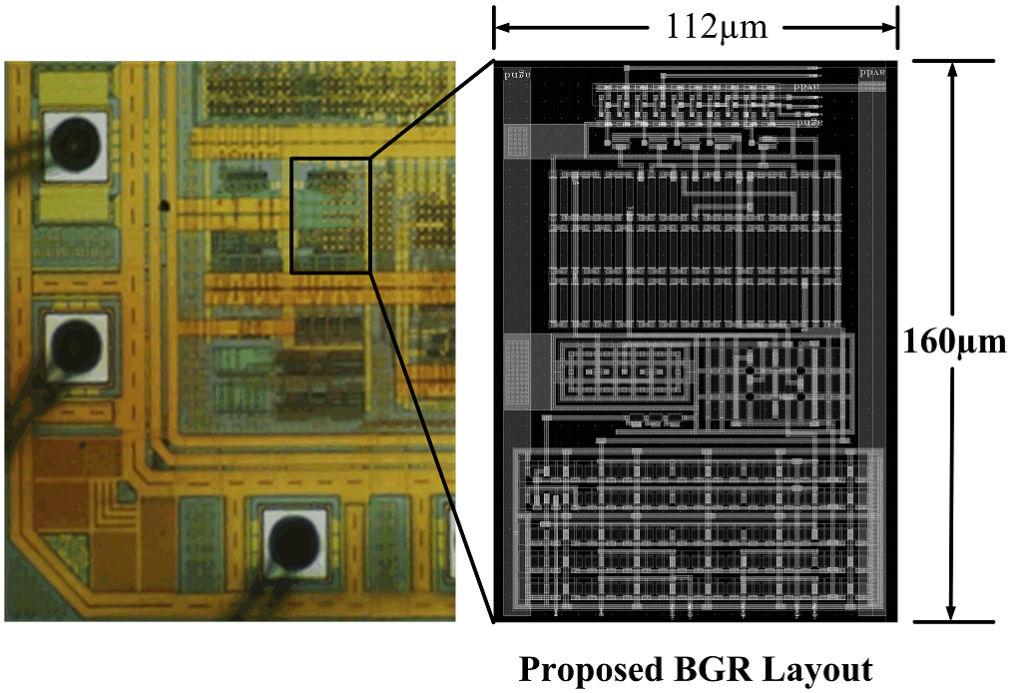

Figure 7: Chip micrograph and Layout of proposed BGR.

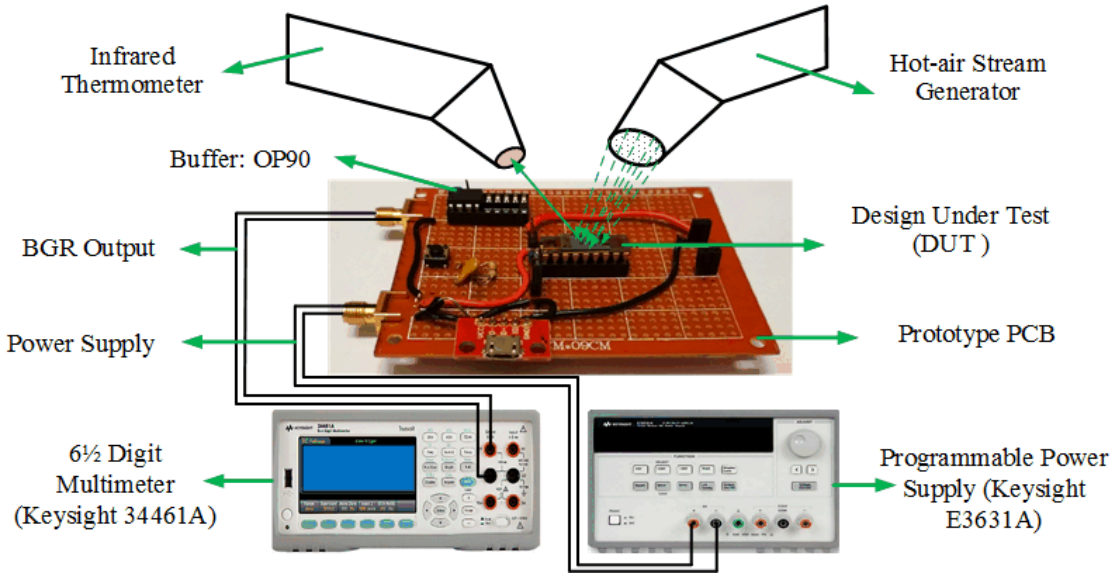

Figure 8: Test Setup for the functional verification of the fabricated BGR.

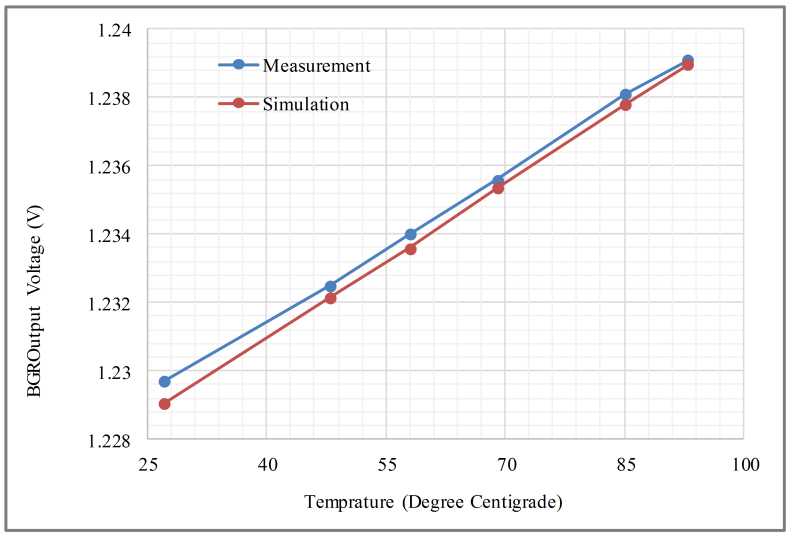

Figure 9: Tempco Plot: Measurement and Simulation.

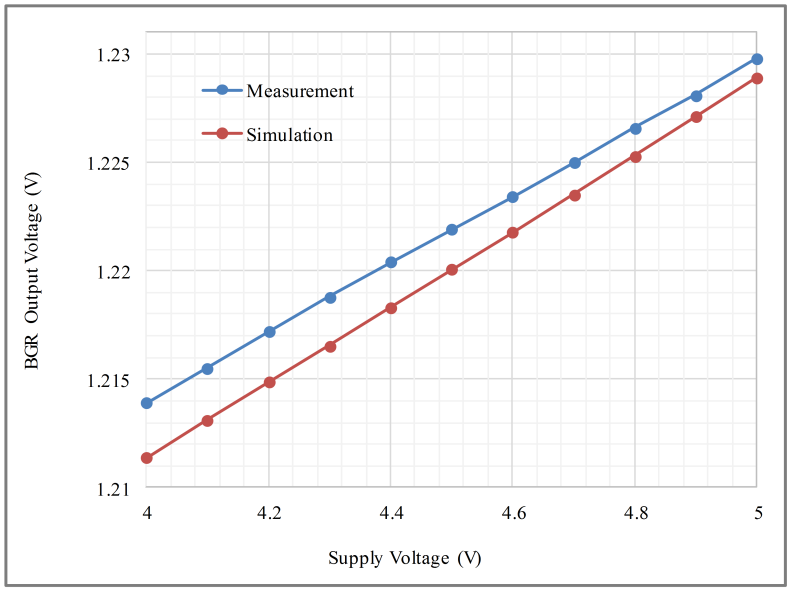

Figure 10: Line Regulation: Measurement and Simulation.

At the time of this writing, ability to do a full temperature characterization using an environmental chamber along with R_2 trimming through I^2C was unavailable. A functional test of the fabricated BGR was done using the test setup as shown in Figure 8 with the R_2 set to the default value. For the functional test, the packaged silicon chip is mounted on a temporary prototype board to test the functionality. We used a buffer (OP-90) at the output of chip to avoid loading from the low-impedance measurement device. A hot air stream was used to heat the device to temperatures between $25°C$ to $100°C$ from the top side of the chip. The temperature was changed by changing the distance between the source of the hot air stream and the device. The output of the BGR was measured using high precision (6-1/2 digit) voltage meter (Keysight 34461A). After each temperature value settled, the temperature of the device was measured using a mounted laser-guided infrared thermometer. The device was powered using a programmable power supply (Keysight E3631A)

Figure 9 shows the measurement result of output voltage versus temperature. As seen from the result, the untrimmed temperature coefficient is strongly PTAT in nature ($115\ ppm/°C$). Some of the random mismatch pairs that could contribute to this are MP_{2-3}, R_1 and R_2 ratio, Q_{1-2} and MN_{1-2} as well. In simulation, when R_2 is increased by 6.5 percentage and V_T offset value of $\sigma V_T/\sqrt{A}$ is applied between MP_{2-3} and MN_{1-2} the simulation results match the test result as shown in Figure 9

For the same offsets added as for the tempco simulation, the line regulation in both simulations and measurements match closely showing a line regulation of $16mV/V$ as shown in Figure 10. On availability of an environment chamber, we will be able to get to the root of the tempco response by doing accurate temperature characterization for different R_2 trim values.

4 Conclusion

In this paper, a self-biased based BGR was improved for area and power by eliminating the reference-voltage branch and integrating it in the main core without compromising temperature drift performance. By using the CTAT voltage in the core of the BGR to generate the reference voltage (V_{REF}), the power consumption of the core and area of the BJTs reduces by 33 percent and 20 percent respectively. The BGR is implemented in a 0.6-μ m CMOS process with an area of $0.018\ mm^2$ that includes the core bandgap and bias currents. This architecture greatly simplifies the design complexity with a temperature coefficient of $6.3\ ppm/^{\circ}C$ for a temperature range of $-40\ ^{\circ}C$ to $125\ ^{\circ}C$ from simulation. The simulated PSR is 35 dB at 1kHz which can be improved by using the cascode self-biased current mirror. This architecture gives a spot noise of $4.34\mu V/\sqrt{Hz}$ dominated by the flicker noise of NMOS and PMOS current-mirrors. The flicker noise can be reduced by increasing the area of those devices or chopping the current mirror.

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