Dual-Step Laser Ablation and Polishing for High-Quality Microgrooves in Low-k Wafer Dicing

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Abstract

High-quality microgrooves are essential for wafer dicing of low-*k* dielectric stacks, where back-end-of-line layers are prone to thermal and mechanical damage. This work introduces a dual-step laser approach that combines UV nanosecond ablation with a low-fluence polishing pass to improve groove integrity. The ablation step defines the microgroove geometry, while the polishing step induces localized remelting to remove recast and microcracks and reduce roughness. Experiments on silicon wafers show that a polishing fluence of 10.6 J/cm² significantly lowers surface roughness by up to 70% without additional ablation. Profilometry and SEM confirm smoother groove bottoms and cleaner sidewalls. The method offers a scalable solution for producing high-quality microgrooves in low-*k* wafer dicing.

Keywords

Wafer dicing; Low-*k* dielectric stacks; Laser grooving; Laser polishing

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1. Introduction

Chips today are becoming increasingly complex, with many heterogeneous layers and materials integrated into the active device region of modern integrated circuits. This complexity makes semiconductor manufacturing far more sensitive to mechanical and thermal damage during downstream processing [1]. After fabrication of the active device layer, the wafer must be separated into individual dies. The general process of cutting the wafer is referred to as wafer dicing, and the final step that physically separates the dies, whether by blade dicing, laser stealth dicing, or controlled breaking after laser grooving, is known as die singulation. As device dimensions continue to shrink and packaging density increases, even minor defects introduced during dicing can reduce yield or render an entire die unusable. Therefore, the precision and quality of wafer dicing are critical determinants of die strength, device yield, and overall reliability [2,3].

Current wafer dicing practices commonly employ laser dicing, laser stealth dicing, and mechanical blade dicing. In recent years, high-precision laser-based dicing technologies have become increasingly dominant due to their ability to process thin and fragile wafers with minimal mechanical loading [4,5]. For laser dicing using the full ablation method, a focused ultraviolet (UV) or visible laser beam scans along the dicing lanes to remove material through the entire wafer thickness [4]. This approach avoids mechanical stresses, but it is relatively slow and may cause thermal damage. It also tends to create debris deposition and microcracks, which ultimately reduce die strength and yield [6]. Laser stealth dicing uses a near infrared (IR) laser that penetrates the wafer surface and focuses approximately 100–150 μm below it. The high energy density at the focal plane generates localized internal modifications composed of microcracks and voids and forms a weakened subsurface layer. The wafer is then separated along this layer through film expansion or controlled mechanical stress [6]. Because no surface ablation occurs, stealth dicing produces clean cuts with minimal thermal impact and makes it highly attractive for ultra-thin and high value wafers used in advanced 3D packaging. However, this technique becomes ineffective for opaque or heavily doped wafers and cannot be applied to devices that contain low-k dielectric layers, creating a major limitation for modern integrated circuits.

Low-k dielectric stacks are porous back-end-of-line (BEOL) insulating layers with a lower dielectric constant ($k \approx 2$–3) than silicon dioxide ($k \approx 4$) [7]. They help reduce capacitance between metal lines which enables faster signal transmission and lower power consumption in integrated circuits. However, their porous and mechanically fragile structure makes them sensitive to stress and heat. This mechanical fragility means that stealth dicing cracks do not propagate uniformly through low-k stacks, leading to unpredictable fracture behavior and die-edge defects. As a result of that, these materials create challenges for stealth dicing, since the propagation of dicing cracks is hindered by the toughness mismatch between the low-k layer and the adjacent silicon or interconnect layers [8].

For these reasons, laser grooving, a shallow-trenching step performed prior to final separation, is often preferred. Grooving removes the fragile low-k dielectric stack in the BEOL prior to singulation, thereby reducing damage and improving overall reliability. As illustrated in Fig. 1, after back grinding, the wafer becomes significantly thinner and mechanically fragile, supported

only by a temporary adhesive layer. At this stage, a narrow laser-ablated trench typically about 50 µm in width and ~30 µm in depth is introduced along the dicing lanes to define the separation path for individual dies. This microchannel removes the low-k dielectric layers and part of the silicon substrate. Following grooving, die singulation methods such as blade dicing, stealth dicing, or hybrid approaches that combine laser-based and mechanical steps, ultimately separating the thinned wafer into individual functional chips.

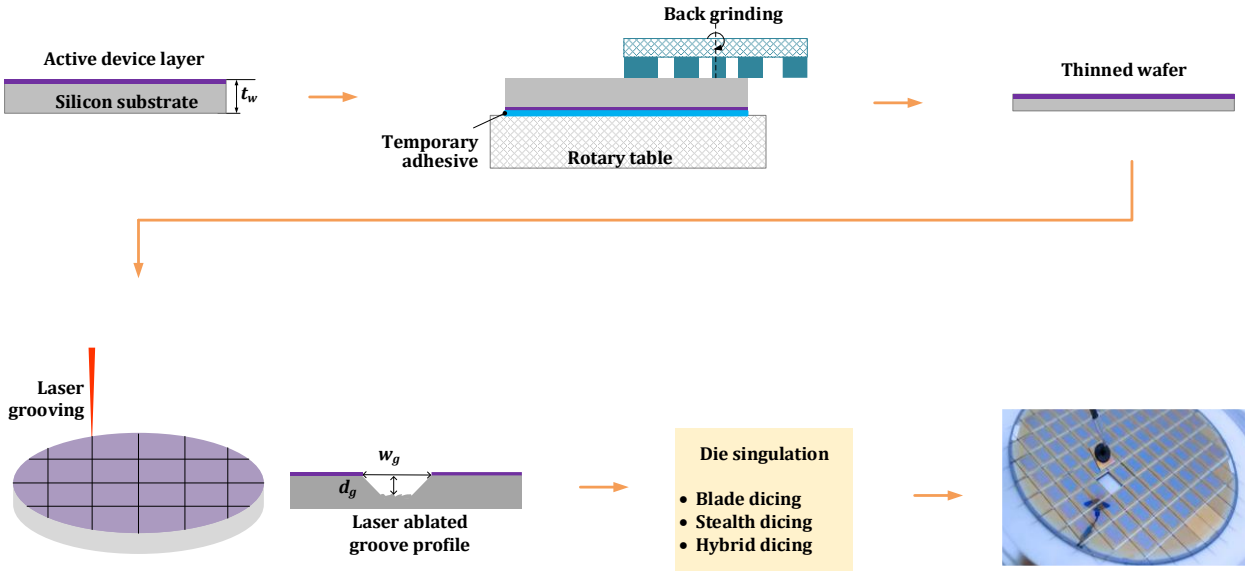

Fig. 1: Dicing workflow for low-*k* dielectric wafer using laser grooving and subsequent die singulation. Note the exact sequence of these operations may differ for different lines of products.

The quality of laser grooving depends strongly on the laser wavelength (λ) and associated process parameters. Shorter wavelengths (UV and visible) and longer wavelengths (near-IR) play distinctly different roles in silicon laser ablation, which in turn affects the cutting mechanism, cutting kerf (width), and achievable dicing speeds. The most widely used UV wavelengths for wafer dicing, i.e., 355 nm (nanosecond and picosecond lasers) and 266 nm (fourth-harmonic diode-pumped solid-state (DPSS) lasers), are absorbed within the first few hundred nanometers of silicon. The strong absorption arises from the high absorption coefficient of silicon (α within the order of 10^3-10^4 cm^{-1}) at UV wavelength region [9–13]. This leads to fine grooves or cuts with less peripheral damage, which is ideal for processes like laser dicing and grooving [14–16]. Near-IR lasers, e.g., 1,064 nm wavelength, have lower absorption in silicon and therefore require higher fluence for ablation; they are primarily used for subsurface modification in stealth dicing rather than surface ablation [17,18]. The range of spot diameter (d, µm) varies from ~10 µm for shorter wavelengths to ~30 µm for longer wavelengths, for a single scan [14,19–21].

These λ-dependent effects also influence achievable groove depth (g_d) and groove width (g_w), sidewall surface roughness (S_a), and the extent of thermally induced damage. For silicon wafer dicing, selecting the appropriate wavelength requires balancing precision and depth: UV lasers produce clean, shallow surface ablation, whereas near-IR lasers support deep modification or separation. Groove depth increases with laser fluence, F (J/cm^2), laser power, P (W), and the number of passes (N_p). To achieve a uniform groove width, the pulse overlapping ratio should be kept at about 70% or above [22]. At higher repetition rates (f, kHz), thermal accumulation occurs due to insufficient cooling time between pulses, increasing the effective heat-affected zone (HAZ) and potentially widening the groove. Lower repetition rate gives more cooling time and tends to confine heating, leading to less heat buildup[23,24]. For a fixed average power, increasing the pulse duration (τ) decreases the peak intensity (Ip), which reduces the ablation efficiency and results in shallower grooves [25].

Even with optimized wavelength and parameters, laser grooving can still produce rough surfaces, recast layers, and microcracks due to the thermal nature of ablation. These defects within the groove can create challenges during the subsequent die-singulation processes and may promote crack propagation into the chips.

In this work, we introduce a novel two-step laser process that combines UV nanosecond laser grooving with a subsequent low-power polishing step to refine the groove. To the best of our knowledge, this is the first approach that integrates laser polishing directly into a dicing workflow to reduce thermally induced groove defects. The two step-laser configuration decouples material removal from surface refinement: the grooving step defines the channel geometry, while the low-power polishing step selectively remelts only the groove surface, allowing smoother and more consistent groove profiles.

2. Method

In this study, we implemented the proposed two-step laser processing workflow to fabricate microgrooves on semiconductor substrates. Fig. 2a outlines the procedure, which consists of laser grooving followed by a low-power polishing scan. In the grooving step, a UV nanosecond laser ablates material along the dicing path to form the initial microchannel geometry. The subsequent polishing step applies a reduced laser fluence to thermally reflow only the surface layer, improving smoothness without additional ablation.

We used a Han's Laser Draco-31D40-15 UV nanosecond pulsed laser system equipped with a high precision galvanometric scanner for surface processing (Fig. 2b). The laser operates on a diode-pumped solid-state (DPSS) principle with a wavelength of 355 nm. It can deliver up to 15 W of average power, with a maximum pulse energy E_p of 500 µJ with a spot size of 40 µm. The output repetition rate is tunable from 10 kHz to 200 kHz, and the pulse duration ranges between 10 ns and 100 ns, allowing flexible control of energy deposition. The silicon wafer materials we tested with were 4-inch, single-side polished silicon wafers with a thickness of 1 mm.

The experimental conditions used for both the ablation and polishing steps are summarized in Table 1. In the ablation experiments, the laser power was maintained at 7.5 W with a repetition rate of 30 kHz and a scanning speed of 500 mm/s. These parameters correspond to a pulse

energy of approximately 250 µJ and a single pulse fluence of 19.9 J/cm², which is well above the ablation threshold of silicon. Under these conditions, three sets of experiments were conducted with 5, 10, and 20 passes, respectively, to investigate the effect of accumulated energy input on groove geometry. As expected, increasing the number of laser passes resulted in a proportional increase in groove depth and, in some cases, a slight variation in groove width due to localized heat accumulation and material re-deposition.

For the polishing step, the same scanning speed and repetition rate were maintained, and the fluence threshold for surface melting was identified for removing the recast layer by inducing localized melting of the surface. For polishing, the average laser power was reduced to 4 W, corresponding to a pulse energy of 133 µJ and a fluence of 10.6 J/cm². The photograph of the silicon wafer with unpolished and polished microgrooves is shown in Fig. 2c.

Table 1. Experimental conditions for ablation and polishing steps

STEP	N_P	***V* (MM/S)**	E_P **(µJ)**	***F* (J/CM²)**	***P* (W)**
STEP 1: ABLATION	5	500	250	19.9	7.5
	10	500	250	19.9	7.5
	20	500	250	19.9	7.5
STEP 2: **POLISHING**	1	500	133.3	10.6	4

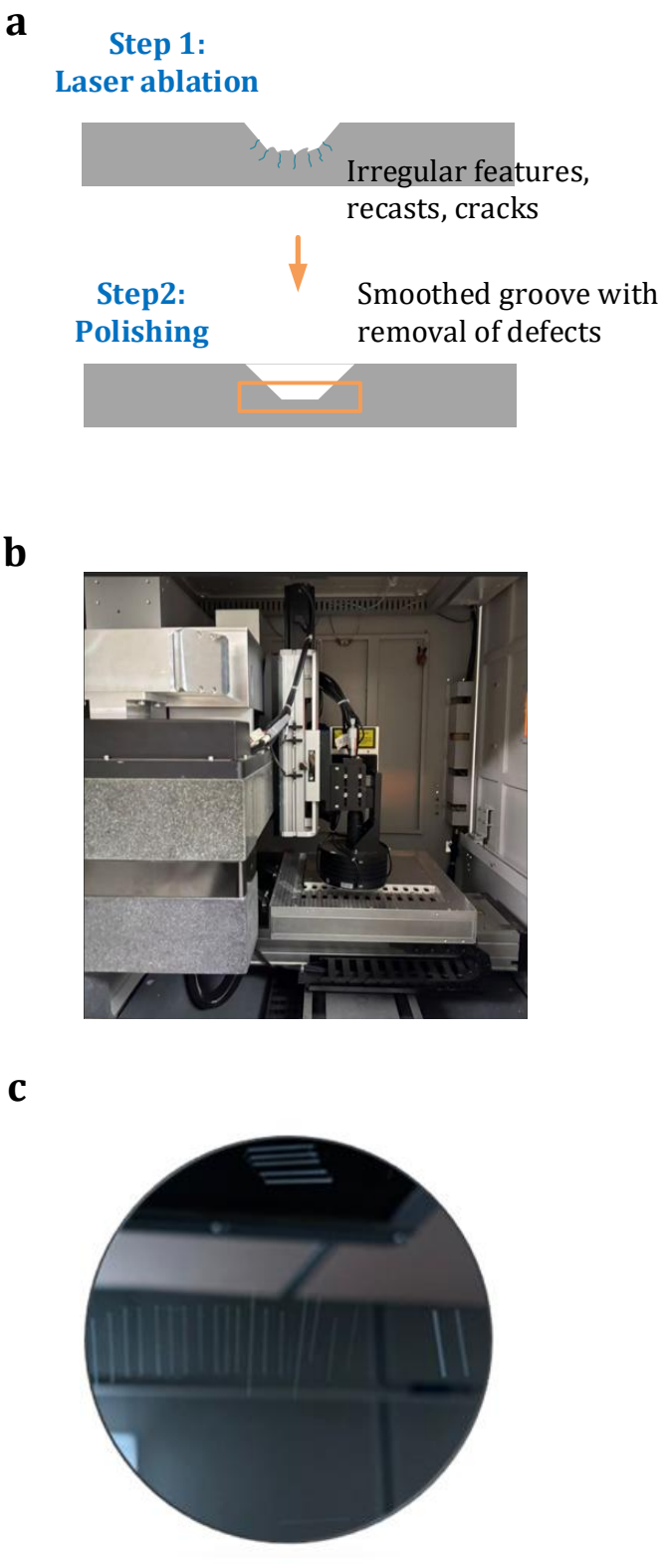

Fig. 2: Experimental approach in this work: (a) Proposed two-step laser ablation and polishing process; (b) Experimental setup using the UV nanosecond pulsed laser system; (c) A photograph of a silicon wafer with microgrooves

3. Results & Discussions

The microgroove profile measurements of the silicon wafer are illustrated in Fig.3. Fig. 3a illustrates the relationship between laser passes and groove depth at a constant laser pulse fluence of 19.9 J/cm². The results clearly show a linear increase in depth with the number of laser passes, confirming a stable and repeatable ablation process. The groove depth increased from approximately 3 µm after one pass to nearly 94 µm after 25 passes. This linear trend confirms that the laser delivers consistent energy per pass and the material removal rate remains stable without saturation or thermal shielding effects. The repeatability of the depth increment also confirms that heat accumulation is minimal, which prevents unintended thermal damage to the surrounding surface.

Fig. 3b shows the optimized laser pulse fluence with no measurable material removal or visible surface modification below a pulse fluence of 10.6 J/cm². Above 10.6 J/cm² pulse fluence, a clear groove began to form and deepen proportionally with increasing power. This behavior suggests that scanning with a 10.6 J/cm² pulse fluence for only one pass is the minimum requirement to induce local melting and trigger surface reflow, which helps remove recast debris and refine the microchannel surface. Consequently, 10.6 J/cm² was selected as the optimal polishing pulse fluence with one pass for subsequent experiments. Selecting an optimal laser power is important to ensure a high-precision surface finish without introducing thermal defects, cracks, or roughness.

Fig. 3c and Fig. 3d show the height profile of polished silicon wafers fabricated with 19.9 J/cm² laser pulse fluence and 10 passes. It can be seen from the height profile Fig.3d that the width of the microchannels is within 15~20 µm and the depth of the microchannels is around 35~40 µm. These values indicate stable material interaction with laser energy and controlled ablation, which is essential for producing uniform microstructures. A narrow range of the microgroove width also suggests that there is minimal lateral heat diffusion, as laser energy is primarily confined to the intended ablation path.

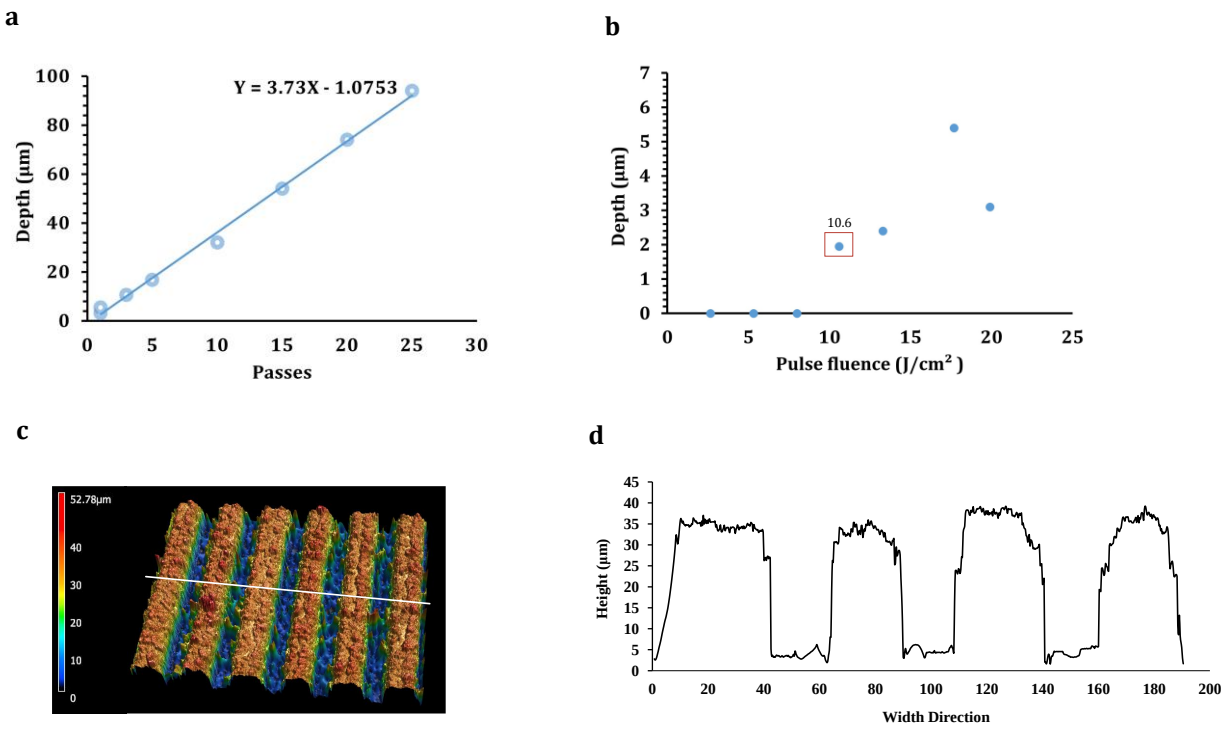

Fig. 3: Groove profile measurement: (a) Relationship of laser ablation passes with groove depth; (b) Relationship of laser pulse fluence with groove depth; (c) Groove morphology of polished silicon wafer for 19.9 J/cm² pulse fluence and 10 passes; (d) Groove profile of polished silicon wafer for 19.9 J/cm² pulse fluence and 10 passes.

Fig. 4 illustrates roughness and scanning electron microscopy (SEM) analysis investigating the surface morphology of unpolished and polished silicon wafers that were laser fabricated with 19.9 J/cm² pulse fluence for different numbers of passes. From Fig. 4a, the values of surface roughness S_a of polished silicon wafers are less than those of unpolished silicon wafers. For 5 passes of laser ablation, the surface roughness value decreased from 7.9 µm to 2.38 µm in polished samples. With increased laser ablation passes, the surface roughness in unpolished samples decreases compared to unpolished samples with five ablation passes. In the case of samples with 20 passes of laser ablation, polishing reduces the surface roughness value from 4.15 µm to 1.05 µm. For the roughness measurement, we kept the measurement window focused on the bottom surface of the microchannels, demonstrating the improvement in surface finishes for the polished surfaces. Reduced roughness after polishing indicates that the laser polishing step effectively removed the recast layer and smoothed the bottom surface of microgrooves.

In Fig. 4b and Fig. 4c, we compared the SEM images of unpolished and polished wafers fabricated with 10 and 20 passes of laser ablation, respectively. All images were taken at 1000× magnification using a 5 kV accelerating voltage to clearly show surface features. For the 10-pass condition in Fig. 4b, the unpolished sample showed surface defects such as recast layers, resolidified melt, and periodic ripples along the laser path. This indicates irregular energy absorption and incomplete ablation along the microgrooves. These defects occur because the melted silicon re-solidifies in an uneven way. This means the laser energy did not remove

material evenly, and some heat spread beyond the ablation path. As a result, the grooves were rough and not uniform. In contrast, the polished sample in Fig. 4b displayed much smoother and more continuous microchannels with cleaner edges. After 10 passes of laser ablation, 10.6 J/cm² pulse fluence was used for one pass to polish the sample. It is evident that polishing removes leftover melted material and flattens small bumps. As a result, the surface interacts with laser energy in a more controlled way, which reduces heat damage and improves groove shape. From Fig. 4c, for the 20-pass condition, the unpolished sample exhibited significant rippling and melt buildup due to excessive localized heating. The polished counterpart in Fig. 4c maintained consistent smooth groove depth and shape with minimal residue. It proves that surface polishing after laser texturing promotes uniform energy interaction and reduces thermal distortion.

The SEM images show that polishing after laser texturing greatly improves the surface quality. It helps prevent recast formation, lowers ripple intensity, and produces uniform microchannels. Polished samples have smoother grooves, cleaner edges, and fewer defects. These results show the importance of surface post-processing for getting a smooth surface finish in laser-textured microchannels.

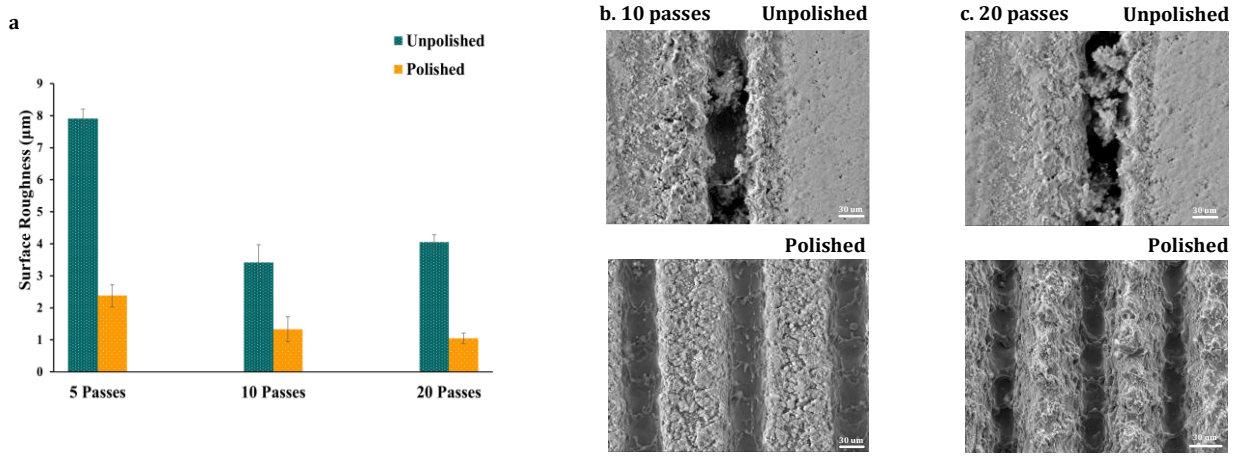

Fig. 4: Effect of laser ablation and polishing: (a) Roughness of unpolished and polished samples for different numbers of laser passes; (b) Unpolished and polished silicon wafer for 10 passes of ablation; (c) Unpolished and polished silicon wafer for 20 passes of ablation.

4. Conclusion

This study demonstrated a two-step laser-based surface modification approach to improve the quality of microgrooves produced on silicon wafers. By combining UV nanosecond laser ablation with a subsequent low-power polishing step, the process effectively reduced surface roughness, recast layers, and microcracks commonly observed in conventional laser grooving. Profilometry and SEM analyses confirmed that controlled thermal remelting during the polishing phase smooths the groove surface while maintaining dimensional accuracy. The results show that the polishing step requires a fluence of 10.6 J/cm² to achieve optimal surface refinement without

additional material removal, which ensures both efficiency and process stability. Following the polishing step, the average roughness of the microgroove bottom surface was reduced to approximately 1–2 μm, representing a substantial decrease compared to the unpolished samples. The proposed dual-step strategy provides a clean, controllable, and scalable route to achieve enhanced surface integrity in semiconductor dicing operations.

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