ON-CHIP SCALABLE HIGH-SPEED ACTIVE BATTERY BALANCERS

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ABSTRACT

Fast active battery balancing circuits often suffer from high implementation cost and limited performance due to the large number of required power switches, gate drivers, and sensing circuitry. Moreover, their balancing speed and efficiency are constrained by parasitic resistances and inductances, resulting in bulky designs and poor scalability. This paper presents a high-speed on-chip active battery balancing module based on flexible stacked half-bridge submodules capable of interfacing with multiple off-chip capacitor networks. The proposed architecture is driven by a single control signal and operates autonomously, eliminating the need for voltage or current sensor-based balancing algorithms. The chip natively supports balancing among four battery cells and can be readily extended to larger battery strings. All control functions, including dead-time generation, voltage level shifting, and gate driving of the balancing switches, are fully integrated on a 3.4 mm^2 die fabricated in a 130-nm Bipolar-CMOS-DMOS (BCD) process using 5-V lateral power switches. To validate the balancing capability, the chip is connected to four external balancing capacitors arranged in a star configuration, and a full-bridge configuration is realized using an additional chip to enhance performance. Experimental results demonstrate robust operation over a wide range of conditions, with switching frequencies from 1 kHz to 5 MHz and cell voltages from 2.4 V to 4.3 V. The proposed circuit achieves effective battery balancing with an average balancing current of up to 2.5 A.

Keywords Integrated battery balancer · Active battery balancing · Battery management systems (BMS) · Switched-capacitor converters · On-chip gate drivers · BCD technology

1 Introduction

Battery cells in drivetrain battery packs are connected in series to achieve high voltages (e.g., 400–800 V) required by the inverter and motor. Due to variations in electrical characteristics such as capacitance, internal resistance, and self-discharge rates, cells experience imbalance, which leads to inefficient utilization of the pack capacity and can trigger premature shutdowns during charging [1, 2]. To address this issue, the Battery Management System (BMS) incorporates a battery balancer to ensure safety and optimal performance by equalizing the state of charge (SOC) across cells [1, 3].

Passive balancing is widely adopted in commercial BMSs due to its circuit simplicity, relying on resistors and/or switches to dissipate excess cell energy as heat. However, this approach results in zero energy efficiency and slow balancing performance [4]. Because passive balancers handle low currents, their switches are relatively simple to drive and can be readily integrated into BMS integrated circuits (ICs), as demonstrated in [5].

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In contrast, active balancing redistributes energy among cells, enabling higher efficiency and faster balancing. This improvement typically comes at the cost of increased circuit complexity, requiring multiple switches and intermediary components to shuttle energy between cells [6, 7].

State-of-the-art capacitor-based active balancers implemented in discrete forms include the single-tiered switched-capacitor (STSC) [8], double-tiered switched-capacitor (DTSC) [9], single switched-capacitor (SSC) [10], chain-structured switched-capacitor (Chain-SC) [11], series-parallel switched-capacitor (SP-SC) [12], star switched-capacitor (Star-SC) [13], delta-structured [14], mesh-structured [15], and complementary star switched-capacitor (CS-SC) [16] topologies. Table 1 summarizes the required numbers of switches, gate drivers, and capacitors, along with their maximum voltage ratings, as functions of the number of battery cells n and the cell voltage V_{cell}. These scaling relationships clearly indicate the rapid growth in hardware complexity for large battery strings. For instance, balancing a 100-cell stack using the CS-SC topology would require 400 switches (and associated gate drivers), resulting in considerable implementation cost, driving complexity and reduced practical scalability.

By avoiding bulky inductors, transformers, and converters, capacitor-based balancers are still attractive candidates for compact and high-speed BMS implementations [6, 17]. Nevertheless, several challenges limit their practical deployment in high-performance systems. High-speed balancing demands extremely low routing resistance, as parasitics directly constrain balancing current, especially at high switching frequencies where resistive impedance dominates. Moreover, parasitic inductances associated with long printed circuit board (PCB) traces restrict the maximum achievable switching frequency. As a result, practical implementations are typically limited to tens of kilohertz, necessitating large, high-voltage capacitors to maintain acceptable balancing speed, which increases cost and volume. In addition, topologies that enable any-cell-to-any-cell energy transfer, such as Star-SC, Delta, Mesh, and CS-SC, require a large number of switches that are often over-rated in discrete implementations and demand costly gate drivers, isolation, and power supplies, further increasing system complexity. In discrete capacitor-based balancers, these parasitic effects fundamentally limit balancing current and switching frequency, forcing large capacitors and over-rated switches that prevent compact, high-speed integration.

In discrete realizations [13, 15, 14, 16], simplicity is achieved through sensor-less automatic balancing based on instantaneous cell-voltage differences and open-loop pulse-width modulation (PWM) control. While attractive, the achievable balancing performance is fundamentally limited by package- and PCB-level parasitics, including routing resistance, parasitic inductance, switch on-resistance, and capacitor equivalent series resistance (ESR). Consequently, a trade-off arises between preserving open-loop control simplicity and achieving high balancing speed and current capability.

Closed-loop approaches mitigate parasitic sensitivity by employing voltage- or SOC-based feedback and are often realized using converter-based topologies [18]. Although effective, these methods increase sensing, control, and power-stage complexity, leading to higher cost and reduced scalability in large cell strings. Therefore, preserving open-loop simplicity while overcoming parasitic and size limitations through tighter integration is critical for advancing capacitor-based balancers.

Monolithic integration of active battery balancers has received limited attention, with most integrated BMS efforts focusing on monitoring and protection. Only a few works incorporate basic balancing functionality. In [5], a battery management IC (BMIC) integrating balancing, protection, and sensing for an eighteen-cell Li-ion stack was demonstrated in a 180-nm Bipolar–CMOS–DMOS (BCD) process. However, the design employs passive resistive balancing, dissipating excess energy as heat. The balancing switches exhibit an on-state resistance of 25 Ω, limiting the balancing current to approximately 5 mA, while the use of high-voltage P-channel devices increases silicon area and cost.

Similarly, [19] proposed a seven-cell Li-ion monitoring and balancing IC in which stacked cells are compared against a reference voltage. The balancing current is limited to 100 mA, and the design relies on bulky 50 V P-channel switches and an external transformer with isolated gate drivers. The IC was fabricated in a 0.35-μm high-voltage triple-well CMOS process using gate-extended devices.

Commercial BMS solutions typically integrate passive balancing alongside monitoring and protection. For example, the TLE9012DQU battery cell management IC supports twelve Li-ion cells with up to 200 mA balancing current capability. Moreover, the Texas Instruments BQ76PL455A-Q1 supports up to sixteen series cells using 60 V switches and shunt resistors. Active balancing is not natively supported and instead requires external devices such as the EMB1428Q switch-matrix gate-driver IC and the EMB1499Q DC–DC controller [20]. These components implement a switch-matrix–based active balancing architecture but rely on discrete, bidirectional high-voltage devices, resulting in increased cost and system complexity.

This paper addresses these gaps by presenting a high-speed on-chip active balancing architecture implemented in 130 nm BCD technology, enabling high-frequency operation through on-chip parasitic minimization and switch-size and

Table 1: Components and Ratings of Capacitor-Based Battery Balancing Circuits

Ref.	Topology	C	SW/GD	$V_{C,max}$	$V_{sw,max}$
[8]	STSC	$n-1$	$2n$	V_{cell}	V_{cell}
[9]	DTSC	$3(n-1)/2$	$2n$	$2V_{cell}$	V_{cell}
[10]	SSC	1	$n+5$	V_{cell}	nV_{cell}
[11]	Chain-SC	n	$2n+4$	V_{cell}	$(n-1)V_{cell}$
[12]	SP-SC	n	$4n$	V_{cell}	$\frac{(n-1)V_{cell}}{2}$
[13]	Star-SC	n	$2n$	$\frac{(n-1)V_{cell}}{2}$	V_{cell}
[14]	Delta	$n(n-1)/2$	$2n$	$(n-1)V_{cell}$	V_{cell}
[15]	Mesh	$2n$	$2n$	$(n-1)V_{cell}$	V_{cell}
[16]	CS-SC	$2n$	$4n$	$\frac{(n-1)V_{cell}}{2}$	V_{cell}

rating customization. The proposed design is scalable on-chip up to the process breakdown limit and can be extended at the board level through its modular architecture, making it suitable for large battery strings. The contributions of this work include monolithic integration and circuit-level techniques that enable a compact, high-current, and high-switching-frequency active balancer through parasitic-aware monolithic integration. For the first time, the design also addresses the optimal sizing and driving of high-current balancing switches based on conduction and dynamic loss optimization.

This paper presents the following contributions:

1. A flexible on-chip stacked half-bridge architecture compatible with multiple capacitor-network topologies, including single-tier, double-tier, mesh, delta, and star configurations. The proposed IC integrates lateral N-channel power switches and gate drivers optimized for the Li-ion voltage range. Integrated level shifting and dead-time generation eliminate the need for external boosted supplies and bulky isolation structures.
2. An optimized layout and wire-bonding strategy that minimizes parasitic resistance and inductance by placing bond pads directly above the power switches. This approach improves high-frequency performance, reduces conduction losses, and significantly lowers the required balancing-capacitor size and cost.
3. Experimental validation of complementary operation using two chip modules, demonstrating enhanced balancing current, faster equalization speed, and improved efficiency.
4. Development of a generalized analytical model linking cell-level imbalance dynamics to transistor-level design parameters, enabling systematic prediction of balancing current and associated power losses.

2 Proposed On-Chip Battery Balancing Architecture and Compatible Capacitive Networks

The proposed topology for on-chip integration is shown in Fig. 1(a) and a complementary circuit architecture composed of two identical circuits of Fig. 1(a) is shown in Fig. 1(b). The on-chip active part composed of lateral switches M_1 to M_{2n} is flexible and supports a broad range of external balancing capacitor configurations presented in the area of active battery balancing literature, including single-tier and double-tier structures, as well as more complex networks such as star, mesh, and delta configurations, as summarized in Fig. 1(c)-(h). Each topology introduces trade-offs in terms of balancing speed, implementation cost, assembly complexity, and the voltage rating requirements of capacitors and switches.

To highlight the key features of the on-chip stacked half-bridge architecture, the star configuration in Fig. 1(e) has been used. Compared to mesh and delta networks, the star topology requires a smaller number of capacitor while providing faster balancing performance than traditional double-tier switched capacitor and single-tier switched capacitor configurations. This benefit arises from the availability of direct charge transfer paths between all cells, enabling an any-cell-to-any-cell energy transfer mode [13].

The circuit shown in Fig. 1(a) operates in two distinct phases and requires only a single open-loop PWM signal. When the control signal is high, the high-side switches (M_1, M_3,...,M_{2n-1}) are turned on during the first half of the switching period (State 1). During the second half of the period (State 2), the low-side switches (M_2, M_4,...,M_{2n}) are activated. This complementary switching scheme enables efficient and rapid energy redistribution among all cells in the stack.

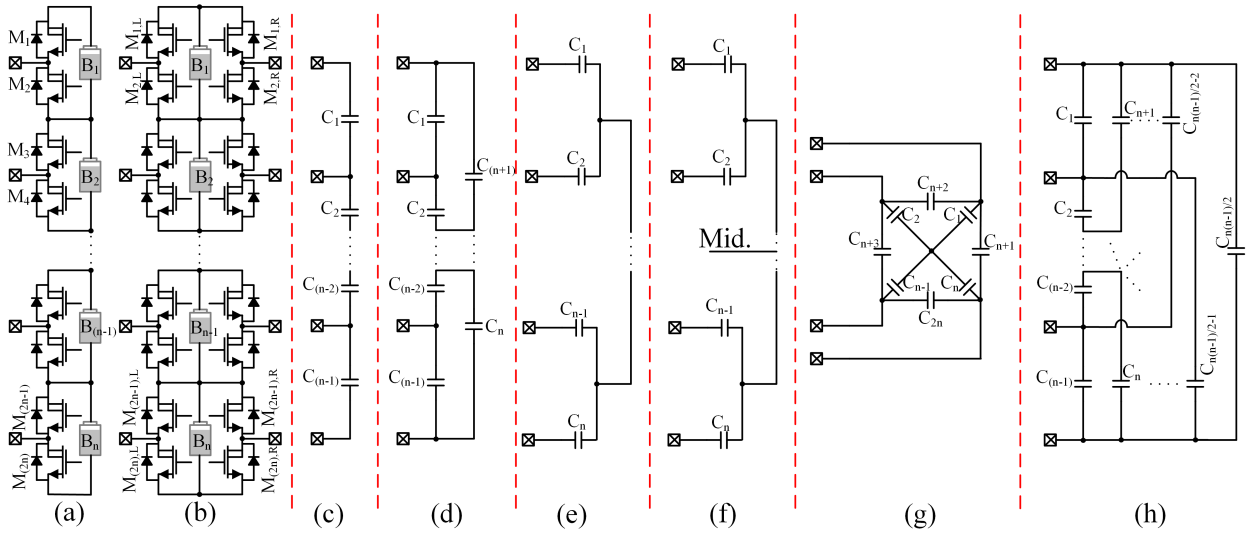

Figure 1: (a) Proposed cell-level stacked half-bridge submodules and (b) its complementary circuit architecture. Options for off-chip balancing networks that can be connected to the circuits in (a) and (b) including: (c) STSC [8], (d) DTSC [9], (e) star-SC [13], (f) modified star-SC [21], (g) mesh-structured SC [15], and (h) delta-structured SC [14].

Furthermore, the circuit can be complemented, as illustrated in Fig. 1(b), to further increase the balancing current by exploiting the full switching cycle for energy transfer, particularly for the top-most and bottom-most cells in the battery stack.

2.1 Generalized Dynamic Analysis of Balancing Currents

To obtain a quantitative characterization of the circuit behaviour under arbitrary cell-imbalance conditions and to relate key design parameters, namely the switching frequency, balancing capacitance, and balancing-path resistance, to the average and RMS values of the balancing currents, this section analyses the half-bridge stacked balancer with a star-configured balancing network.

Prior work, such as [21], employs switching-limit impedance analysis, in which the slow- and fast-switching limit (SSL and FSL) impedances are derived to estimate balancing impedances at low and high switching frequencies, respectively. While effective for single-input single-output topologies such as switched-capacitor DC–DC converters, this approach cannot be readily generalized to systems with an arbitrary number of cells. Consequently, the balancing currents under general imbalance conditions cannot be predicted based on switching-limit impedance analysis. The transient analysis presented in [16] considers electrically isolated cell configurations, such as cascaded H-bridge balancers, in which the cells are not connected in series. For the series-connected capacitive balancer circuit, only a static DC analysis is provided. Building on that approach, generic analytical expressions are derived for the balancing currents, capacitor voltages, and capacitor currents under arbitrary imbalance conditions for the series-connected circuit shown in Fig. 1(a), when combined with the capacitor-based balancing network in Fig. 1(e). These expressions are subsequently used to evaluate power losses and to determine the optimal switch sizing of the balancer IC.

In this analysis, the switching frequency is assumed to be well below the self-resonant frequency of the balancing capacitors, which is determined by their equivalent series inductance and the parasitic inductance associated with the circuit interconnections and PCB routings, as demonstrated in the lumped circuit model in Fig. 2. Under this condition, the balancer operates in the capacitive regime and the impedance is dominated by the capacitive reactance. The impact of operating at frequencies near and beyond the self-resonant frequency is examined and compared with the analytical results through circuit simulations and experimental measurements in the next sections of this paper.

The equivalent circuits for the two operating states are shown in Fig. 3. All balancing capacitors $C_1 - C_n$ are assumed identical, and the internal battery resistance R_b is neglected in the analytical development for simplicity. Its impact on the balancing currents is evaluated separately through simulations.

For State 1 ($t \in [0, T/2]$, $k \in \{1, \ldots, n-1\}$), Kirchhoff's voltage law (KVL) gives

$$\left(1 + R_e C_e \tfrac{d}{dt}\right)\left(V_{Ck,1} - V_{C(k+1),1}\right) = -V_k u(t), \tag{1}$$

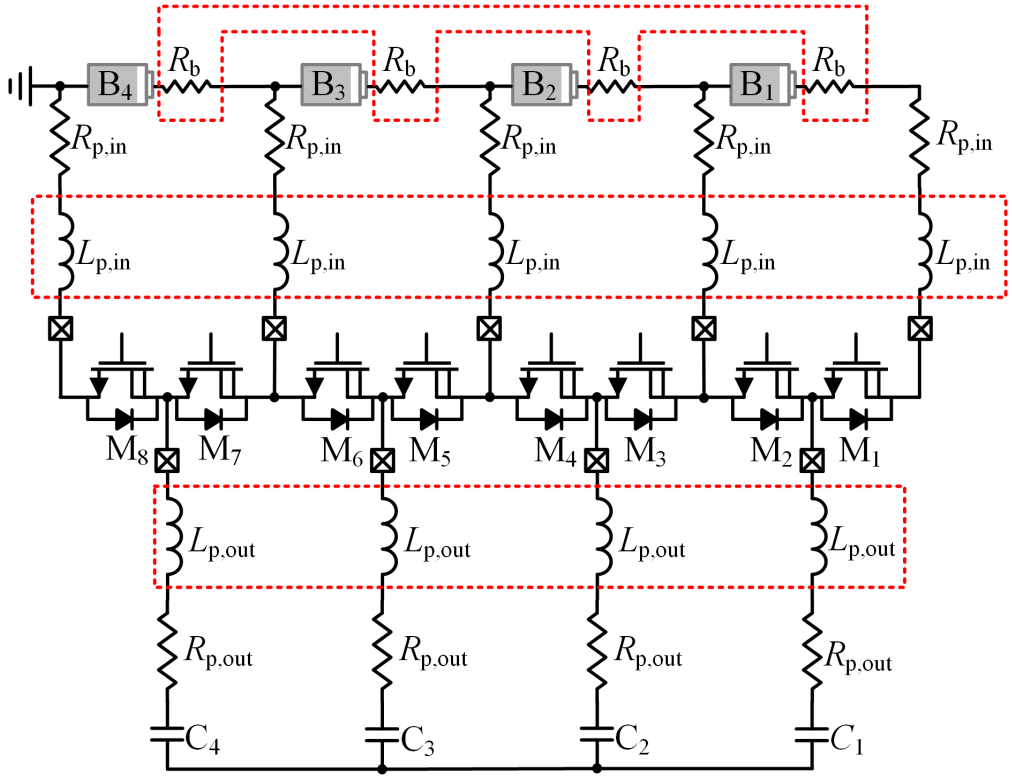

Figure 2: Half-bridge balancer architecture incorporating parasitic effects, including the internal battery resistance R_{b} and inductances at the input and output ports ($L_{\mathrm{p,in}}$ and $L_{\mathrm{p,out}}$).

where R_{e} includes the input and output parasitic resistances ($R_{\mathrm{p,in}}$ and $R_{\mathrm{p,out}}$ in Fig. 2) as well as the switch on-state resistance. Because the capacitor bottom plates share a floating node, and the node is assumed initially uncharged, the charge conservation gives:

$$\sum_{k=1}^{n} Q_k(t) = 0 \implies \sum_{k=1}^{n} V_{Ck,1}(t) = 0. \tag{2}$$

Moreover, applying Kirchhoff's current law (KCL) at the floating node gives

$$\sum_{k=1}^{n} i_{Ck}(t) = C_e \sum_{k=1}^{n} \frac{dV_{Ck}(t)}{dt} = 0 \tag{3}$$

Solving (1) subject to (2) and (3) yields a first-order response with $\tau = R_e C_e$:

$$V_{Ck,1}(t) = V_{Ck,1}^{\infty}\left(1 - e^{-t/\tau}\right) + V_{Ck,1}^{0} e^{-t/\tau}, \qquad t \in [0, T/2], \tag{4}$$

where the State-1 forced (steady) value is

$$V_{Ck,1}^{\infty} = \frac{1}{n}\left(\sum_{i=1}^{n-1} iV_i - n\sum_{i=k}^{n-1} V_i\right). \tag{5}$$

In State 2 ($t \in [T/2, T]$), the same development applies with the index shift $V_i \mapsto V_{i+1}$, giving

$$V_{Ck,2}^{\infty} = \frac{1}{n}\left(\sum_{i=1}^{n-1} iV_{i+1} - n\sum_{i=k}^{n-1} V_{i+1}\right). \tag{6}$$

The fast-switching-limit (FSL) voltage, illustrated in Fig. 4, is thus expressed as

$$V_{\mathrm{FSL}} = \frac{V_{Ck,1}^{\infty} + V_{Ck,2}^{\infty}}{2}. \tag{7}$$

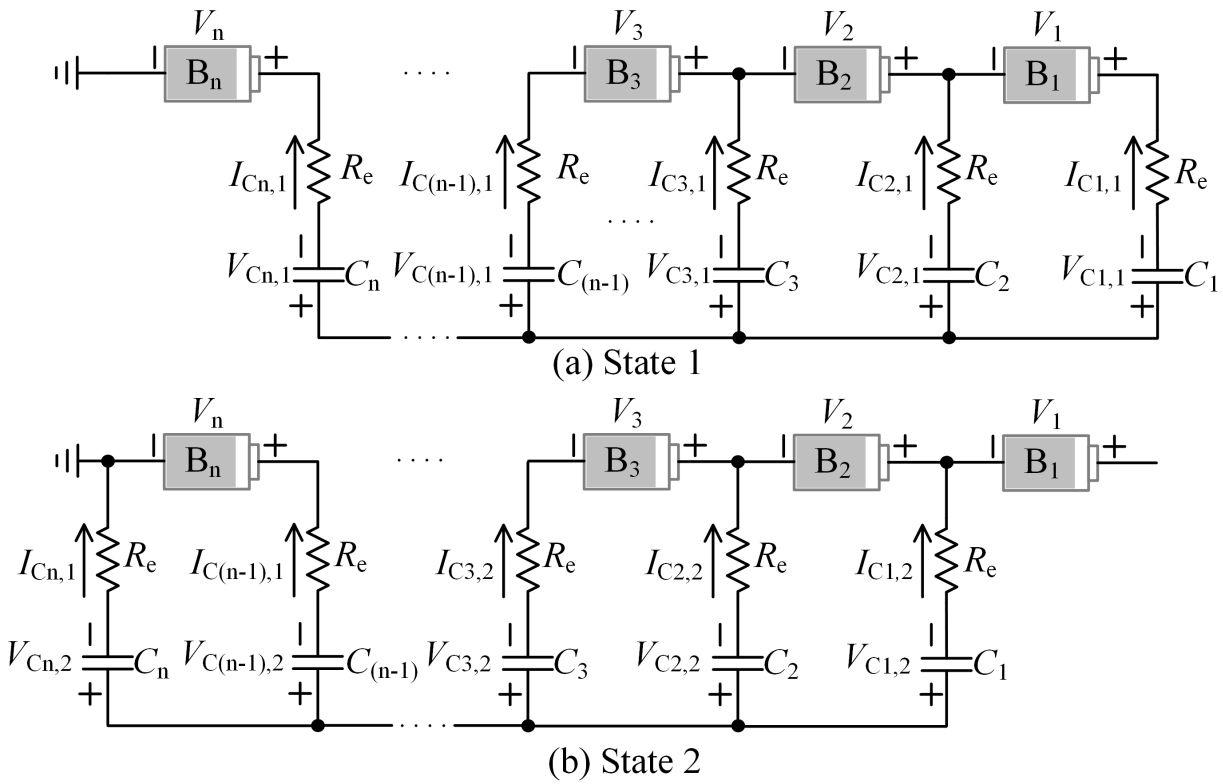

Figure 3: Equivalent circuits of the proposed architecture in Fig. 1(a) when interfaced with the capacitive network in Fig. 1(e) for switching States I and II.

Hence, the half-cycle boundary condition is written as

$$V_{Ck,1}\left(\tfrac{T}{2}\right) = 2V_{\mathrm{FSL}} - V^{0}_{Ck,1}. \tag{8}$$

For compactness, define

$$\alpha(t) = e^{-t/\tau}, \qquad \beta = e^{-T/(2\tau)} = e^{-1/(2fR_eC_e)}, \tag{9}$$

and

$$A = nV^{\infty}_{Ck,1}, \qquad B = nV^{\infty}_{Ck,2}. \tag{10}$$

Then the periodic steady-state capacitor voltage over one period is

$$V_{Ck,1}(t) = \frac{1}{n}\left[A(1-\alpha(t)) + \alpha(t)\left(\frac{B+A\beta}{1+\beta}\right)\right], \tag{11}$$

$$V_{Ck,2}(t) = \frac{1}{n}\Bigg[B(1-\alpha(t-T/2)) + \alpha(t-T/2)\left(\frac{A+B\beta}{1+\beta}\right)\Bigg]. \tag{12}$$

Using $I_{Ck} = C_e\, dV_{Ck}/dt$, the capacitor current is

$$I_{Ck,1}(t) = -\frac{1}{nR_e}\left(\frac{B-A}{1+\beta}\right)\alpha(t), \tag{13}$$

$$I_{Ck,2}(t) = -\frac{1}{nR_e}\left(\frac{A-B}{1+\beta}\right)\alpha(t-T/2). \tag{14}$$

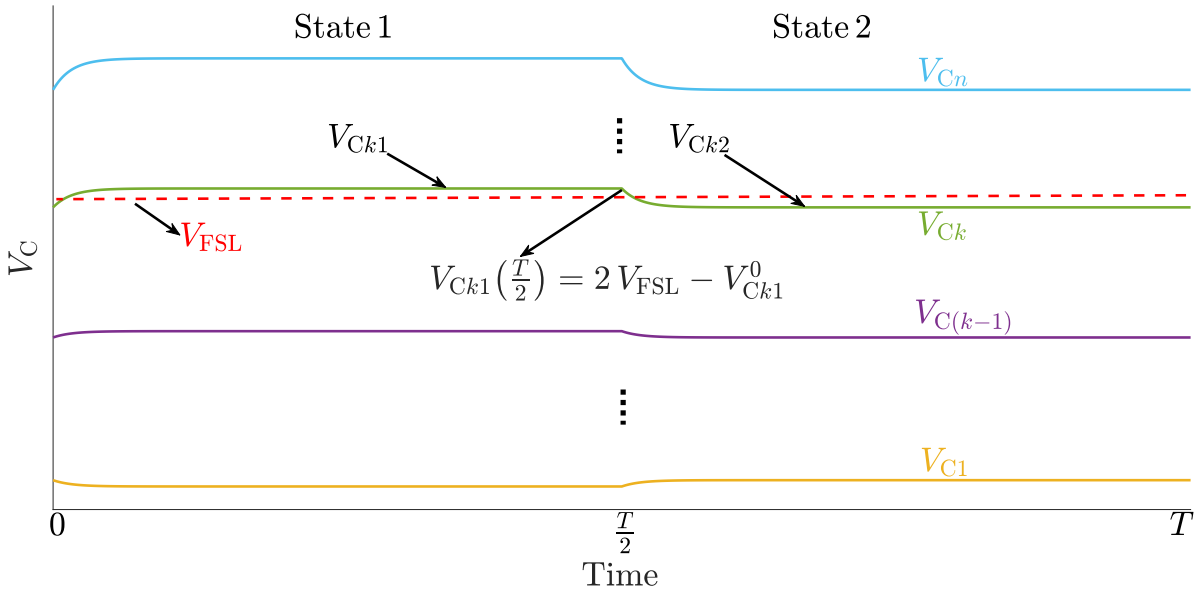

Figure 4: Illustration of the initial condition of the k^{th} capacitor voltage under an arbitrary imbalance condition.

The instantaneous battery current follows from KCL as

$$I_{Bk}(t) = \begin{cases} -\sum_{i=1}^{k} I_{Ci,1}(t), & t \in [0, T/2],\ 1 \le k \le n-1, \\ \sum_{i=k}^{n} I_{Ci,2}(t), & t \in [T/2, T],\ 2 \le k \le n-1, \\ 0, & \text{otherwise.} \end{cases} \tag{15}$$

Hence, the average and RMS battery currents are

$$\overline{I_{Bk}} = \frac{1}{T}\left[\int_0^{T/2}\left(-\sum_{i=1}^{k} I_{Ci,1}(t)\right)dt + \int_{T/2}^{T}\left(\sum_{i=k}^{n} I_{Ci,2}(t)\right)dt\right], \tag{16}$$

$$I_{Bk,\text{RMS}} = \left\{\frac{1}{T}\left[\int_0^{T/2}\left(\sum_{i=1}^{k} I_{Ci,1}(t)\right)^2 dt + \int_{T/2}^{T}\left(\sum_{i=k}^{n} I_{Ci,2}(t)\right)^2 dt\right]\right\}^{1/2}. \tag{17}$$

This analysis can be readily extended to the full-bridge circuit shown in Fig. 1(b), which incorporates a replica circuit operating in a complementary manner with respect to the primary one. Based on this symmetry, the battery currents during State I and State II can be derived using KCL:

$$I_{Bk,i} = \begin{cases} -I_{Ck1,i}, & i = 1, \\ I_{Ck1,i}, & i = 2, \end{cases} \qquad \text{for } k \in [1, n]. \tag{18}$$

Therefore, full-bridge operation enables continuous current flow through the battery cells, improving balancing performance and efficiency by increasing the average balancing current relative to its RMS value. Although this advantage was demonstrated in discrete implementations in [16], it requires double the hardware resources, limiting practicality and scalability for large battery strings and thereby motivating the need for an integrated on-chip solution.

These analytical predictions will be validated through circuit simulations and comprehensive experimental results.

2.2 Balancer Power Losses

The primary power loss components include switching losses and conduction losses. Switching power losses arise from the charging and discharging of the switches' parasitic capacitances, namely the gate-source ($C_{\rm gs}$), gate-drain ($C_{\rm gd}$), and drain-source ($C_{\rm ds}$) capacitances. The total switching power loss can be expressed as:

$$P_{\rm dyn} = 2nf\left(C_{\rm gs}\Delta V_{\rm gs}^2 + C_{\rm gd}\Delta V_{\rm gd}^2 + C_{\rm ds}\Delta V_{\rm ds}^2\right), \tag{19}$$

where f is the switching frequency, and $\Delta V_{\rm gs}$, $\Delta V_{\rm gd}$, and $\Delta V_{\rm ds}$ represent the voltage differences between the switch terminals during switching phases.

Conduction losses arise from the RMS current flowing through different resistances in the balancing path. The resulting conduction power loss over one switching period is given by

$$P_{\rm cond} = R_e \sum_{k=1}^{n} \overline{I_{Ck}^2}. \tag{20}$$

The capacitor currents in the two half-cycles are equal but opposite in direction, i.e.,

$$I_{Ck,2}(t) = -I_{Ck,1}(t - T/2), \qquad t \in [T/2,\, T]. \tag{21}$$

As a result, the mean-square capacitor current can be evaluated over either half-cycle as

$$\overline{I_{Ck}^2} = \frac{2}{T}\int_0^{T/2} I_{Ck,1}^2(t)\,dt = \frac{2}{T}\int_{T/2}^{T} I_{Ck,2}^2(t)\,dt. \tag{22}$$

Summing the two loss components, the total losses of the balancing circuit are:

$$P_{\rm tot} = P_{\rm dyn} + P_{\rm cond}. \tag{23}$$

The total capacitance and on-state resistance for a given switch width, $W_{\rm s}$, can be expressed by:

$$R_{\rm on} = \frac{r_{\rm on}}{W_s}, \tag{24}$$

$$C_{\rm gs} = c_{\rm gs}\cdot W_{\rm s}, \tag{25}$$

$$C_{\rm gd} = c_{\rm gd}\cdot W_{\rm s}, \tag{26}$$

$$C_{\rm ds} = c_{\rm ds}\cdot W_{\rm s}, \tag{27}$$

where $c_{\rm gs}$, $c_{\rm gd}$, $c_{\rm ds}$ are the per-unit gate-source, gate-drain, and drain-source capacitances of the switch, respectively, and $r_{\rm on}$ is the per-unit on-state resistance. Defining the following parameter for dynamic losses:

$$\zeta = c_{\rm gs}\Delta V_{\rm gs}^2 + c_{\rm gd}\Delta V_{\rm gd}^2 + c_{\rm ds}\Delta V_{\rm ds}^2, \tag{28}$$

The total losses per switch are then expressed as:

$$P_{\rm switch} = \frac{r_{\rm on}}{W_{\rm s}}\cdot 0.5 I_{\rm switch}^2 + f\cdot W_{\rm s}\cdot\zeta, \tag{29}$$

where $I_{\rm switch}$ is the RSM switch current which can be computed based on the mean-square capacitor currents in (22).

To determine the optimal switch size, $P_{\rm switch}$ is differentiated with respect to $W_{\rm s}$ and the result is set to zero to yield the optimal switch width:

$$W_{\rm s,opt} = \sqrt{\frac{0.5 I_{\rm switch}^2\cdot r_{\rm on}}{f\cdot\zeta}}. \tag{30}$$

Different design approaches can be adopted for sizing the circuit components. One approach starts from the desired balancing performance. In this case, the target balancing speed and current are first specified, from which suitable values of $C_{\rm e}$ and the switching frequency f are selected. The required on-resistance $R_{\rm on}$ is then obtained from the analytical model, and the switch width $W_{\rm s}$ is sized accordingly. Under this approach, the switch and capacitor currents are known a priori, and the corresponding switching and conduction losses can be directly evaluated to meet the targeted performance and efficiency. Alternatively, the sizing process can be driven by silicon area and cost constraints. In this case, the available switch width $W_{\rm s}$ (or equivalently, the maximum allowable switch area) is fixed in advance. The resulting switch $R_{\rm on}$ determines the allowable switch current for given values of $C_{\rm e}$ and f, which in turn sets the achievable balancing current, speed, and overall performance.

3 Integrated Circuit Technologies

A key advantage of on-chip integration for battery balancers is the flexibility in device sizing. Transistor dimensions, particularly channel width, can be optimised to achieve an appropriate trade-off between on-resistance and parasitic capacitances, thereby balancing conduction losses against switching performance.

BCD technologies incorporate high-voltage MOS devices specifically designed for power management applications. Unlike discrete vertical power transistors, these devices are realised in lateral configurations, enabling co-integration with analogue, digital, and mixed-signal circuitry on the same die. All device terminals are accessible from the chip surface, simplifying routing and fabrication whilst supporting high integration density.

The co-integration of high-voltage power devices with control and protection circuitry enables battery balancing systems to be implemented on a single chip. Functions such as monitoring, protection, regulation, and control can be embedded within the same IC, improving compactness, cost efficiency, and overall system reliability.

High-voltage operation of on-chip power switches above the global silicon substrate can be achieved either through junction-isolated structures or by employing silicon-on-insulator (SOI) substrates, as discussed in the following sections based on [22, 23, 24, 25, 26, 27].

3.1 DEMOS and LDMOS Switches

A drain extended MOS (DEMOS) transistor employs a lightly doped drain extension to increase breakdown voltage by reducing the electric field beneath the gate near the drain. This structure is achieved using an extended N-well region without adding process complexity. DEMOS transistors exhibit threshold voltages similar to standard CMOS devices. However, their relatively high on-resistance limits their use to medium-voltage applications rather than true power switching [24, 22].

The laterally diffused MOS (LDMOS) transistor is the standard power device in integrated power technologies. It achieves lower on-resistance through a more complex process involving double diffusion of the N+ source and P-type body. The separation between source and drain defines the drift region, which allows high drain–source voltages.

Figure 5(a) shows the LDMOS structure, where current flows laterally across the surface, enabling co-integration with other control functions. To support high-voltage operation, where the source–body terminal of the device is biased above the substrate potential, a buried N-layer (NBL) is employed as a junction-isolation technique. The NBL electrically separates the device from the substrate and thus enables high-side switch operation in BCD technologies. As the source terminal is isolated, it can swing below ground potential, whilst the drain must remain positive to maintain reverse bias with respect to the P-substrate. A few parasitic diodes are thus inherent to the LDMOS structure: a body diode between drain and source, an isolation diode between NBL and substrate, and a diode between the body-source of the device and the NBL.

Although the NBL approach offers a cost-effective isolation solution, it necessitates careful management of bipolar parasitic effects and increases the required layout area of the switch. Alternative isolation techniques developed to enhance performance and mitigate these limitations use deep-trench isolation (DTI) and SOI technologies.

To achieve lower on-resistance, multiple unit transistors, referred to as fingers, are connected in parallel. Each unit corresponds to a single LDMOS finger, similar to the cross section shown in Fig. 5(a). The symmetrical geometry of each finger allows adjacent drain regions to overlap, enabling a compact and highly regular transistor layout. The channel length, however, is predefined by the technology for a given breakdown voltage and cannot be altered through circuit design [22, 23, 24, 25, 26, 27].

3.2 SOI Technology

Instead of using an NBL or deep n-well isolation structures, BCD technologies can be implemented on an SOI substrate, as illustrated in Fig. 5(b) [26]. In this case, DTI structures are also employed to isolate the field regions between devices.

SOI technology offers substantial flexibility for series stacking of devices, since it improves breakdown capability and supports floating source/body operation. Additionally, the high-resistivity SOI substrate reduces substrate losses, and the overall switch area is smaller than in junction-isolated BCD processes because no bulky rings are required for isolation. SOI processes are inherently immune to latch-up due to the suppression of parasitic bipolar conduction paths, making them well suited for high-voltage and highly integrated circuits. Another key advantage is the ability to support negative (below-ground) supply voltages and to maintain robust immunity against negative transients [24].

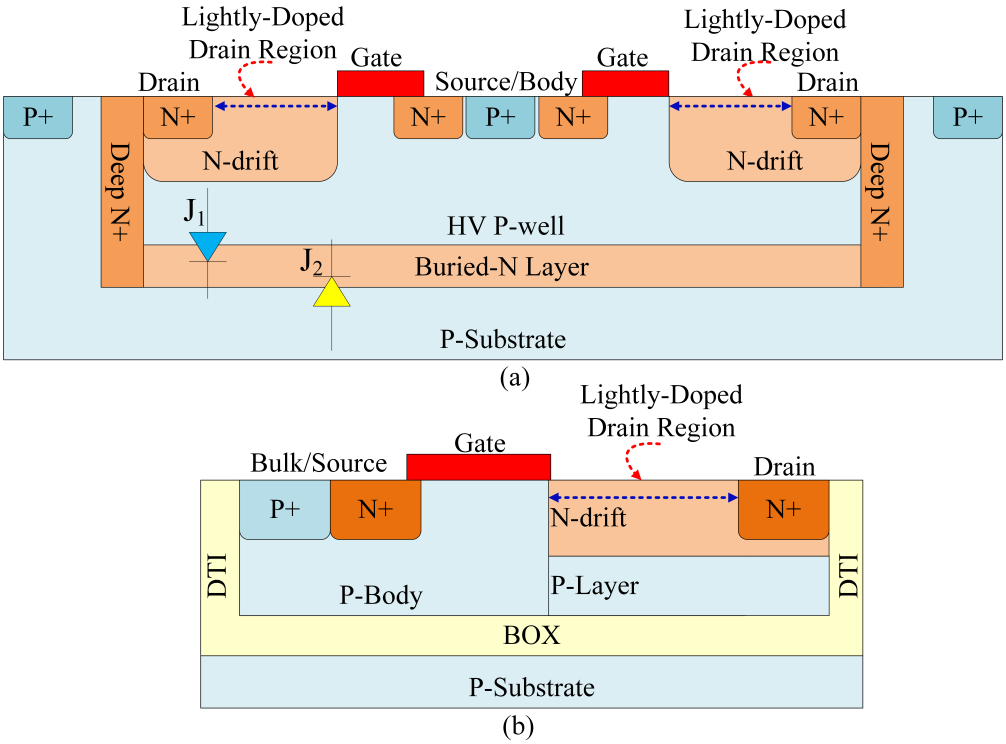

Figure 5: Cross-sectional views of (a) an LDMOS device with junction isolation and (b) a power transistor implemented in an SOI technology, isolated by DTI and a BOX layer.

However, the insulated substrate of SOI technologies leads to higher fabrication costs. Furthermore, the BOX layer exhibits a higher thermal resistance than silicon, which can degrade heat dissipation. As a result, SOI-based devices may experience increased junction temperatures during high-power operation due to both dynamic and static power losses [28, 29, 30].

In this work, the circuit was designed and implemented in a 130-nm BCD process using 5-V devices with substrate isolation, enabling operation with battery stacks of approximately eight to ten Li-ion cells. To reduce fabrication cost while validating the proposed on-chip balancing approach, a four-cell balancer prototype was fabricated. Owing to the modular and scalable architecture of the design, the solution can be extended in several ways. On-chip expansion is possible up to the breakdown limits of the isolation structure, or by adopting an SOI-based process to support higher stack voltages. Alternatively, multiple ICs can be stacked at the board level to accommodate longer battery strings.

4 Circuit Implementations

The complete schematic of the proposed balancer, including the off-chip balancing capacitors, is shown in Fig. 6. The circuit is composed of four stacked half-bridge converter sub-modules (termed HBC_1 to HBC_4) as detailed in (Fig. 6(b)). The details of the circuit design elements are explained next.

4.1 Dead-Time Generation and Level-Shifting

The circuit is driven by an input control signal IN with a duty cycle of 0.5. This signal is divided into two non-overlapping phases with an inserted dead-time interval and is subsequently fed into a voltage level shifter, which generates multiple differential output signals, as shown in Fig. 6(a) [31, 32].

The dead-time generation circuit comprises two devices, $\mathrm{M}_{\mathrm{dt1}}$ and $\mathrm{M}_{\mathrm{dt2}}$, along with resistors R_{dt1} and R_{dt2}, capacitors C_{dt1} and C_{dt2}, and CMOS inverters. The duration of dead-time is determined mainly by the $R_{\mathrm{dt1}}C_{\mathrm{dt1}}$ time constant, which delays the rising edge of the signals to achieve the desired dead-time. Various NAND- or NOR-based non-overlapping clock generation techniques may also be employed.

The output signals from the dead-time circuit are then level-shifted using a multiple-output voltage level shifter. This circuit consists of stacked NDMOS devices (M_1 to M_7 and M_2 to M_8).

The circuit operates by distributing the total voltage, V_{cell1}, equally across the NDMOS devices in both high and low states of the input signal, IN. When IN_1 transitions from V_{cell4} to V_{SS}, the gate-source voltage of M_1 increases while its drain-source voltage decreases from V_{cell3} to V_{cell4}. This causes M_1 to turn on, which in turn activates M_3 in a cascading sequence through the stack until the topmost device, M_7, is triggered. At this point, V_{cell1} is evenly divided across the drain-source terminals of all devices in the stack. Conversely, when IN_1 transitions from V_{SS} to V_{cell4}, M_1 enters a high-impedance state, causing its drain voltage to rise towards V_{cell3}. The remaining devices in the stack respond similarly, maintaining a constant drain-source voltage across each device equivalent to the supply voltage. A detailed delay-power trade-off analysis of the circuit is provided in [31].

4.2 Half-Bridge Architecture

The output signals of the level shifter, V_{LS_R1}...V_{LS_R4} and V_{LS_L1}...V_{LS_L4}, are subsequently used to control the operation of the half-bridge sub-modules gate driver circuits in Fig. 6(b).

To maintain waveform polarity and phase alignment, preserve the pre-set dead-time duration, and ensure proper circuit operation, the low-side and high-side control paths are designed to be identical. As a result, floating voltage level shifter

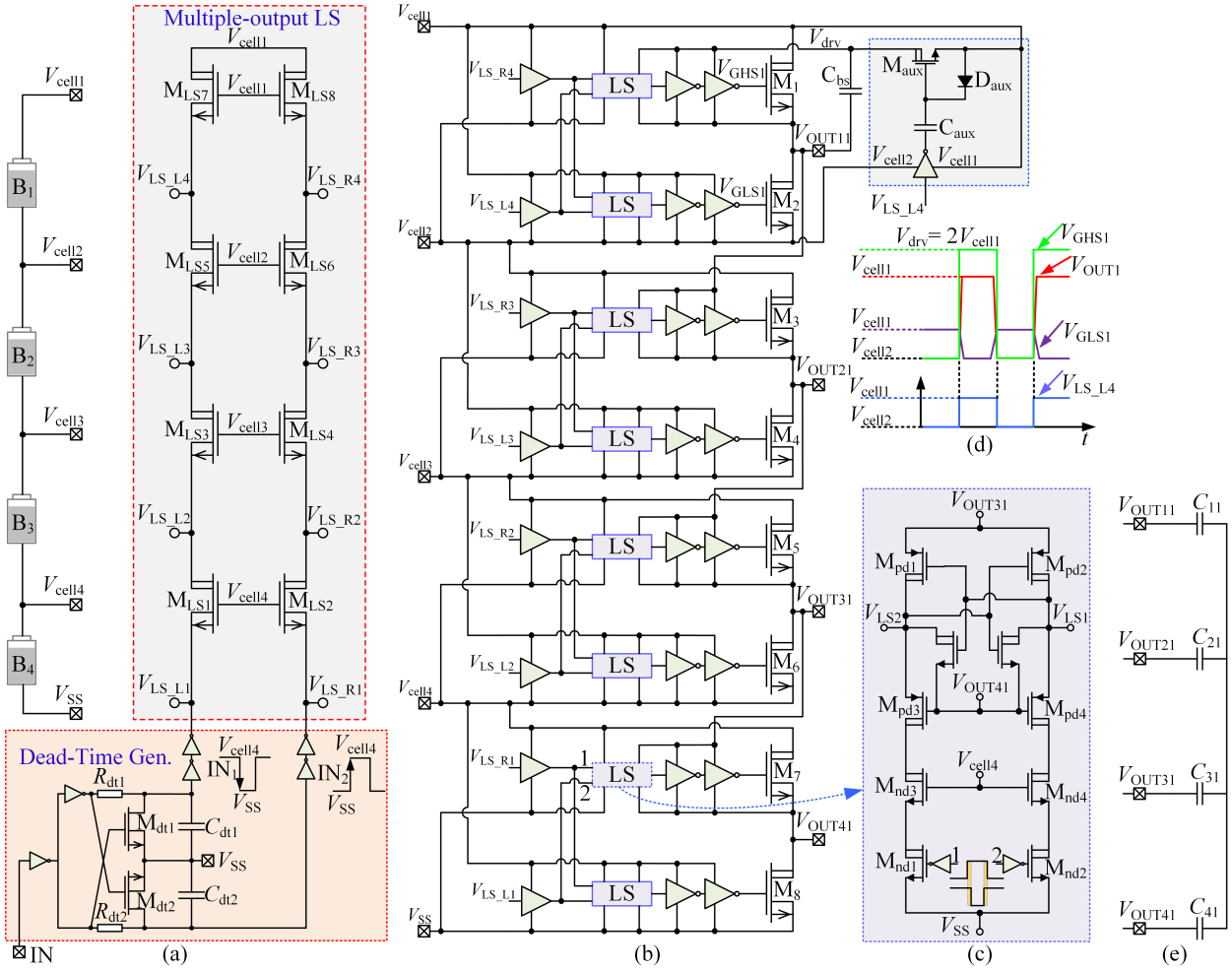

Figure 6: Detailed transistor-level implementation of the half-bridge balancing architecture, including: (a) dead-time generation and multiple-output level shifter [31, 32]; (b) stacked half-bridge balancing modules with drivers and level-shifter circuits; (c) floating voltage level shifter; (d) timing diagram for the top-most half-bridge operation with a bootstrapped high-side supply; and (e) off-chip balancing capacitors in a star configuration.

circuits (LS) are symmetrically employed for both control paths. For the low side, the LS blocks primarily serve to equalize delays. Each LS block utilizes a conventional cross-coupled architecture, as demonstrated in Fig. 6(c) [33].

The high-side switches receive their gate overdrive voltages from the outputs of the upper sub-modules. For instance, the output of HBC_1, denoted as V_{OUT11}, supplies the gate overdrive voltage for the high-side switch of HBC_2. In general, for all intermediate stacked sub-modules, the driver supply voltage is provided directly by the battery cell of the next higher sub-module, and no dedicated external driver supply is required as long as additional cells are stacked above.

For the high-side switch in the uppermost sub-module, where no higher cell is available, a floating gate overdrive voltage must be generated locally. In this case, the required drive voltage can be generated using the simple bootstrap capacitor circuit shown in Fig. 6(d) [22]. Owing to the low driver-voltage requirement (5 V) and the relatively high switching frequency of the proposed balancer, this approach requires only a small off-chip capacitor (around 1 nF) and introduces negligible additional cost.

The low-side switches, by contrast, are directly driven by gate voltages derived from the same battery domain they are regulating. This advantage is enabled by the use of low-voltage NDMOS devices, which, unlike discrete switches, can be effectively turned on by gate overdrive voltages within the typical Li-ion battery voltage range.

Finally, the circuit outputs V_{OUT11} through V_{OUT41} are connected to off-chip capacitors C_{11} through C_{41}, enabling charge redistribution for active battery cell balancing.

The proposed IC can be configured to operate as a full-bridge circuit, as previously introduced at the topology level in Fig. 1(b). As illustrated in Fig. 7, two identical ICs, denoted as IC1 and IC2, are interconnected to operate in a complementary manner. Each IC module is driven by a single PWM control signal and interfaces with four balancing capacitors arranged in a star configuration. This configuration enables full-bridge operation and is intended to achieve higher balancing speed and improved efficiency as validated in discrete form in [16].

5 Simulation Results

In this section, simulation results are presented to validate the derived expressions for the balancing current. The simulations also examine the impact of parasitic inductances and internal battery resistance on the balancing performance, and compare the results with the analytical model that neglects these parasitic effects. The analytical model is subsequently used to estimate the total power losses and to decompose them into conduction and switching losses, as well as additional contributions arising from parasitic elements such as capacitor ESR and wire-bond resistances. Furthermore, post-layout circuit simulations are performed to verify the operation of the level-shifting and dead-time

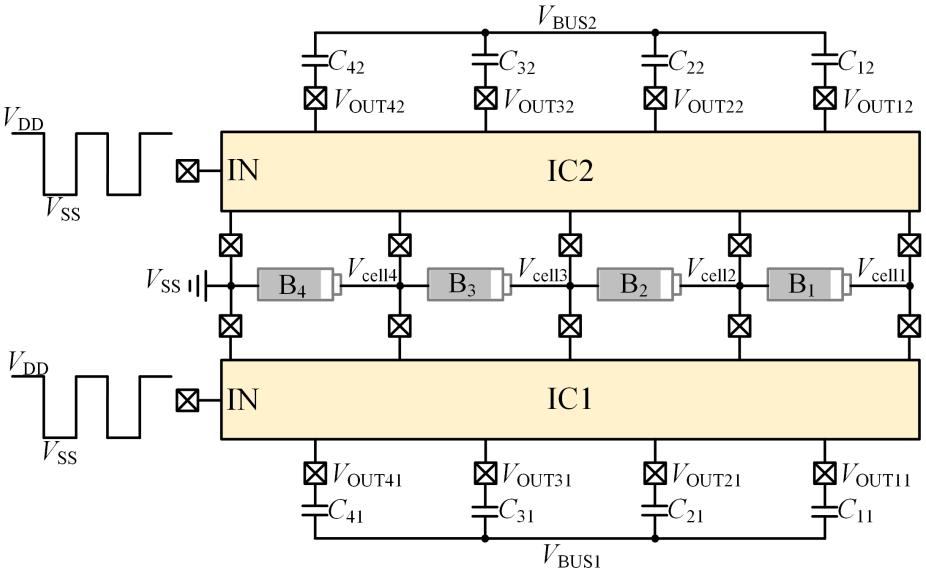

Figure 7: Full-bridge balancer realization formed by two complementary IC modules, enabling higher balancing current and improved balancing speed.

generation circuits under realistic non-ideal conditions, including parasitic effects, battery voltage mismatch, and process and temperature variations.

5.1 System-Level Simulations

The half-bridge and full-bridge balancing circuits were simulated for a string of four battery cells. Fig. 8 illustrates the capacitor voltages and currents, as well as the battery currents, at a switching frequency of $f = 4\,\text{kHz}$, with an equivalent resistance of $R_\text{e} = 0.2\,\Omega$ and a total balancing capacitance of $C_\text{e} = 200\,\mu\text{F}$. The cell voltages from top to bottom (V_1 to V_4) were set to 4.3 V, 4.0 V, 3.1 V, and 2.8 V, respectively.

As expected, the capacitor voltages in Fig. 8(a) sum to zero at any time, in accordance with (2). Furthermore, Fig. 8(b) shows that each capacitor current has a zero average value over one switching period, and that the sum of all capacitor currents leaving the floating bus node is also zero, which is consistent with (3).

The battery currents for the half-bridge circuit are shown in Fig. 8(c) and follow the relationship given in (15). The corresponding battery currents for the full-bridge circuit are reported in Fig. 8(d), and they satisfy (18).

It can be observed that the complementary operation of the full-bridge topology results in a continuous current flow through the battery cells during both halves of the switching cycle. This leads to a more symmetric balancing process among the cells and improved performance in terms of average balancing current.

The impact of the balancing capacitance and the switching frequency on the operation of both the half-bridge and full-bridge circuits is investigated in Fig. 9 under identical cell voltage imbalances and path resistance. Indices $k = 1, 4$ correspond to the top and bottom cell currents, while $k = 2, 3$ correspond to the middle-cell currents. It can be observed that increasing either the switching frequency or the balancing capacitance increases the average battery current, and therefore accelerates the balancing process. This relationship indicates that operating at higher switching frequencies is beneficial, provided that switching losses can be maintained at a low level. Since this trend requires high-performance switches and very compact layouts to minimize parasitic effects, on-chip integration becomes a natural and attractive solution for implementing high-speed balancer circuits.

Moreover, keeping the balancing capacitance as low as possible reduces the overall implementation cost and enables the use of compact packaging, thereby increasing the power density of the balancer. This aspect is particularly important for large battery strings, where the balancing capacitors must withstand high voltages. For the full-bridge topology, it is evident that the balancing current is almost doubled compared to the half-bridge configuration. This allows a further reduction in the required capacitance and/or switching frequency without compromising the balancing performance.

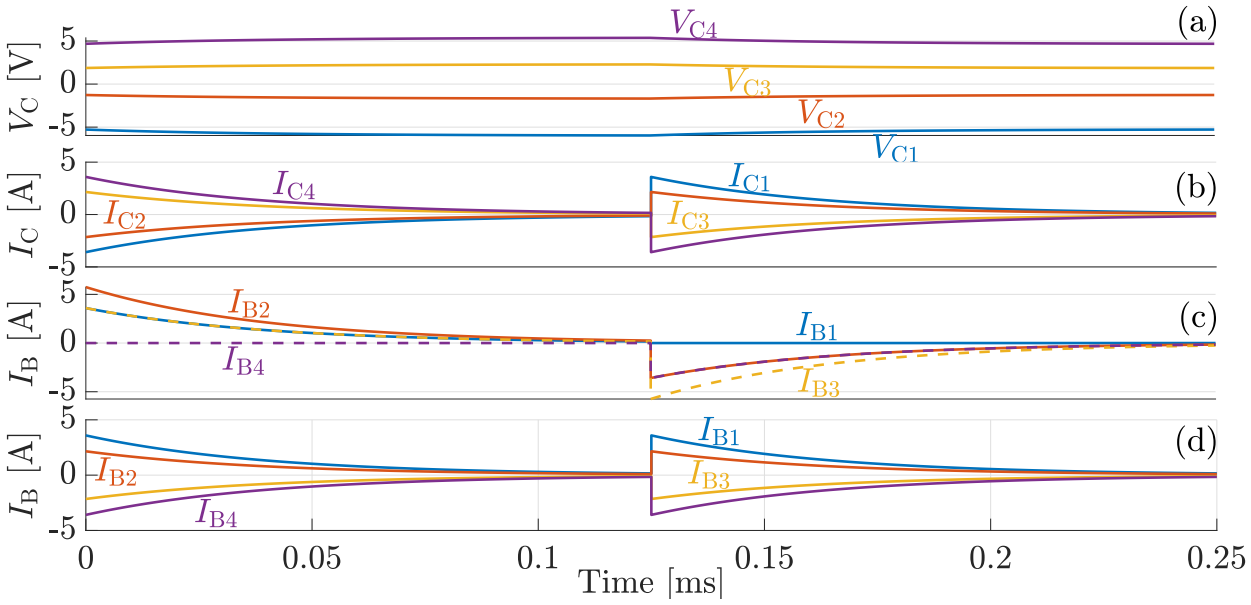

Figure 8: Analytically derived waveforms of (a) capacitor voltages, (b) capacitor currents, and (c) battery currents for the half-bridge architecture (Fig. 1(a)), and (d) battery currents for the full-bridge architecture (Fig. 1(b)). The cell voltage distribution from V_1 to V_4 is 4.3 V, 4.0 V, 3.1 V, and 2.8 V.

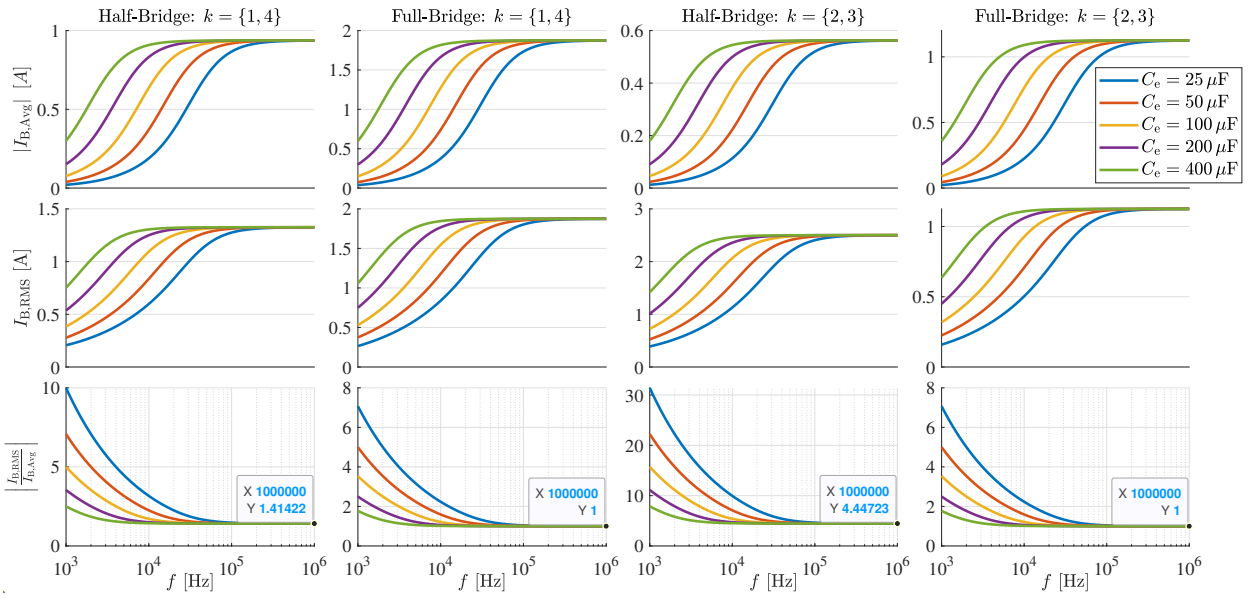

Figure 9: Comparison of half-bridge and full-bridge architectures based on analytically derived waveforms of the average battery current, RMS battery current, and the RMS-to-average ratio of the battery balancing current for a four-cell balancing circuit. The cell voltage distribution from V_1 to V_4 is 4.3 V, 4.0 V, 3.1 V, and 2.8 V.

The impact of these parameters on the balancing efficiency can be further assessed by examining the RMS battery currents. The RMS current determines the conduction losses and the self-heating of both the battery cells and the power switches. Therefore, it is desirable to maximize the average balancing current relative to the RMS current. To achieve this, the switching frequency and/or the balancing capacitance must be sufficiently high to minimize the RMS-to-average current ratio, as illustrated in Fig. 9. Once again, the full-bridge circuit exhibits superior performance according to this metric, as the current continuity enabled by the complementary operation leads to higher average balancing currents for a given RMS value.

The main drawback of the full-bridge configuration is the doubling of the required hardware with respect to the single-circuit balancer. However, with the proposed IC-based balancer approach, the overall balancer size remains compact, while the hardware complexity and cost are significantly reduced compared to fully discrete implementations [16, 13].

The impact of the parasitic inductances at both the input and output of the balancer circuit, as well as the internal battery resistance, illustrated in Fig. 2, is investigated in Fig. 10. The circuit was simulated considering 20 nH parasitic inductances at both the input and output terminals and an internal battery resistance of 10 mΩ, under the same cell voltage distribution discussed previously.

These parasitic elements have a negligible effect on the battery current waveforms at low switching frequencies, or in the SSL regime. This is due to the dominance of the capacitive reactance in the balancing path. In contrast, their influence becomes more pronounced at higher switching frequencies, corresponding to FSL regime, where the dominant impedances are the inductive reactance of balancing capacitors, resistive components of the switches, the capacitor ESR, and other parasitic resistances.

Since the full-bridge circuit achieves continuous current operation at significantly lower switching frequencies compared to the half-bridge topology, the effect of parasitic inductances on its balancing currents is considerably reduced, as confirmed by Fig. 10(ii). This characteristic makes the full-bridge configuration inherently more robust against parasitic effects in high-speed operation.

Overall, minimizing parasitic inductances and resistances is essential to achieve higher balancing currents, reduce power losses, and enable operation at higher switching frequencies for faster balancing. Such requirements are difficult to satisfy using bulky off-chip components and long PCB interconnections. Therefore, an on-chip implementation naturally mitigates these limitations by offering compact layouts with reduced parasitics, making it a highly suitable solution for high-performance balancing circuits.

To further demonstrate the effectiveness of the on-chip balancer design, the breakdown of the power loss components at a switching frequency of 1 MHz is presented in Fig. 11 for three different imbalance scenarios. These results

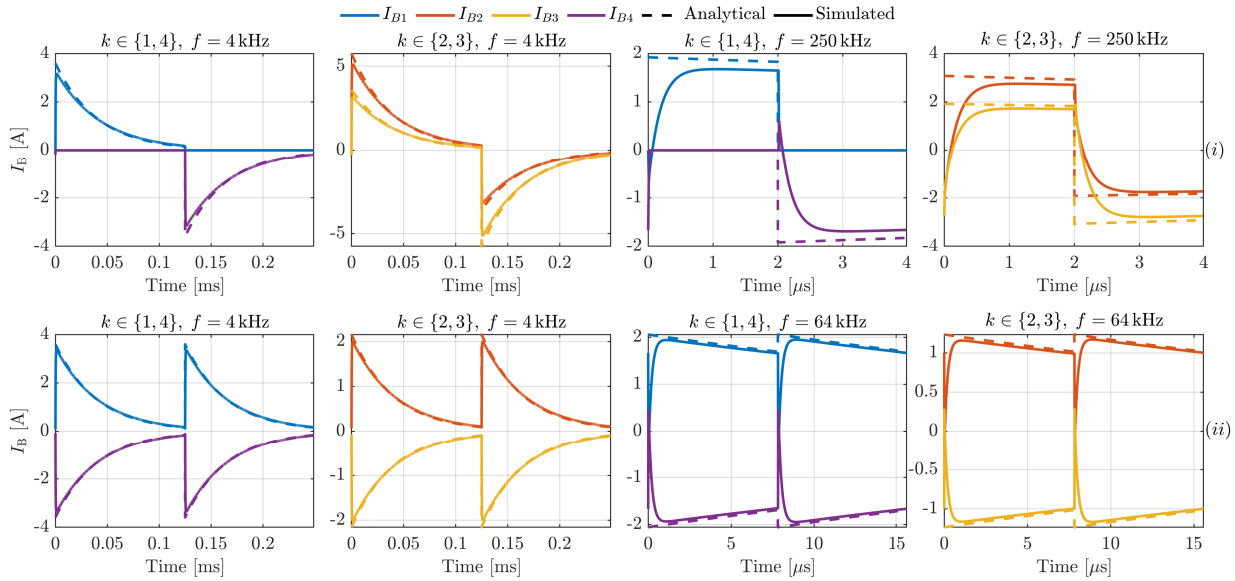

Figure 10: Analytical versus simulated waveforms of battery balancing currents under slow and fast-swtiching limits for (i) a four-cell half-bridge architecture and (ii) a four-cell full-bridge architecture. The analytical model includes $R_\text{e} = 0.2\,\Omega$ and $C_\text{e} = 200\,\mu\text{F}$. The simulated model includes an internal battery resistance of $R_\text{b} = 10\,\text{m}\Omega$ and input and output parasitic inductances of $L_\text{p,in} = L_\text{p,out} = 20\,\text{nH}$. The cell voltage distribution from V_1 to V_4 is 4.3 V, 4.0 V, 3.1 V, and 2.8 V.

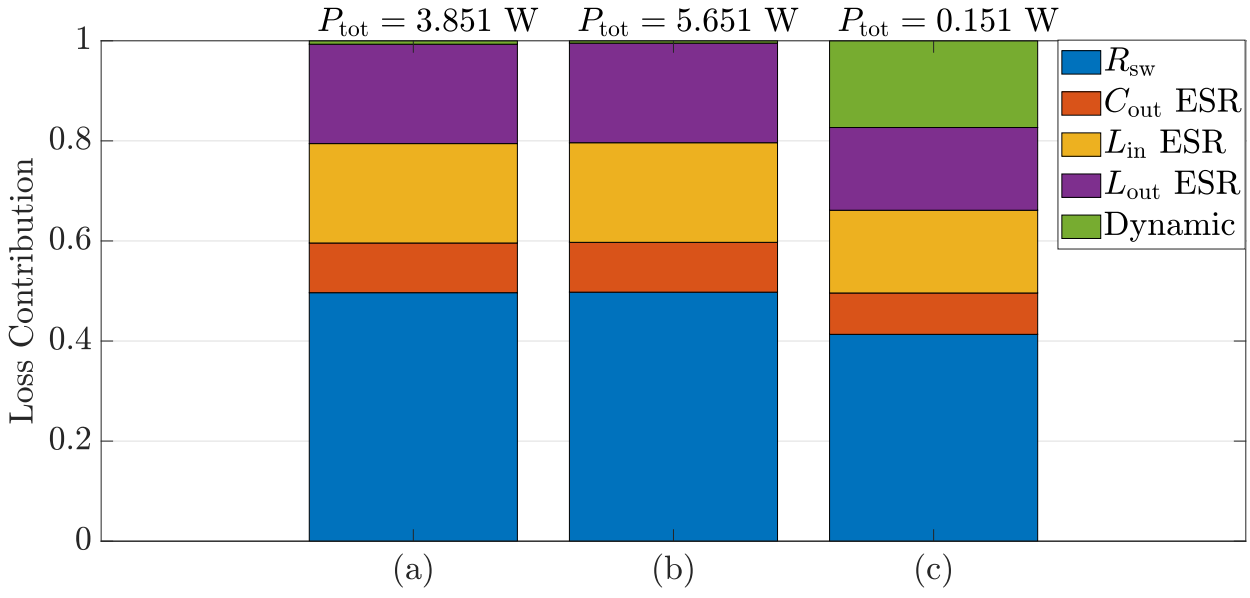

Figure 11: Breakdown of power loss components for a four-cell balancing circuit, at a switching frequency of 1 MHz a total balancing capacitance (C_e) of 200 μF. The cell voltage distribution from top to bottom is for (a) 4.3 V, 4.0 V, 3.1 V, 2.8 V, (b) 4.3 V, 2.8 V, 4.3 V, 2.8 V, and (c) 3.6 V, 3.5 V, 3.4 V, 3.3 V.

correspond to a switch width of approximately 64 mm. The total losses are decomposed into contributions from the switch on-resistance, R_sw, including metallization effects, the ESR of the balancing capacitors and the input and output wire-bond inductors, as well as the dynamic (switching) losses of the power devices.

It can be observed that, across all three scenarios, the dynamic power loss component remains relatively small. It becomes noticeable only under small voltage imbalance conditions, as shown in Fig. 11(c), and is negligible in the other cases.

These findings validate the high-speed operational capability of the on-chip balancer architecture and its potential to achieve fast battery balancing. Moreover, the low dynamic losses at 1 MHz indicate that the balancing capacitance can be reduced by operating at higher switching frequencies without compromising the overall efficiency or the switching performance of the circuit.

5.2 Post-layout Circuit Simulations

To validate the robustness of the proposed dead-time generator and level-shifter circuits in Fig. 6, a set of post-layout simulations was carried out under different operating conditions. The extracted parasitic resistances, capacitances, and coupling capacitances (RCC) were included and compared against schematic-level simulations, as shown in Fig. 12. The simulations were performed with all battery cell voltages set to 3.7 V and at a nominal temperature of $27\,^{\circ}\mathrm{C}$. The results demonstrate a very low propagation delay of the level-shifter, which increases from 290 ps at schematic level to 365 ps after including parasitic resistive and capacitive effects. The level-shifter draws approximately 18 mA during signal transitions, while the dead-time generator provides a fixed dead-time duration of about 20 ns. The current consumption can be significantly reduced by increasing the device dimensions in the level-shifter stage.

To investigate the impact of battery voltage imbalance on the circuit operation, Fig. 13(a) and (b) show the output waveforms of the level-shifter pre-buffer stages for two extreme imbalance scenarios. In Fig. 13(a), the cell voltages (V_1 to V_4) are 3.01 V, 3.44 V, 3.87 V, and 4.3 V, respectively, whereas in Fig. 13(b) they are reversed to 4.3 V, 3.87 V, 3.44 V, and 3.01 V. The results confirm reliable operation even under severe imbalance conditions, while maintaining a propagation delay between 240 ps to 300 ps.

The robustness of the proposed circuits under extreme operating conditions is further evaluated through process, voltage, and temperature (PVT) corner simulations, as reported in Fig. 14. Simulations were performed at temperatures of $-20\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ for each process corner. The cell voltages were set to $V_1 = 3.44\,\mathrm{V}$, $V_2 = 4.3\,\mathrm{V}$, $V_3 = 3.44\,\mathrm{V}$, and $V_4 = 4.3\,\mathrm{V}$. It can be observed that process variations mainly affect the dead-time duration: it increases under the slow–slow (SS) corner and decreases under the fast–fast (FF) corner. However, the propagation delay remains almost unchanged, since both the rising and falling edges shift consistently. The current drawn by the first inverter stack is also shown, indicating that under extreme PVT conditions some inverters exhibit a small static or cross-conduction current on the order of 1 mA, mainly due to large voltage differences between adjacent cells.

Finally, the impact of device mismatch on timing accuracy was evaluated through Monte Carlo simulations performed at the worst-case minimum cell voltage of 2.5 V, which corresponds to the slowest operating condition. The dead-time durations for the bottom-most and top-most submodules were extracted and are shown in Fig. 15, together with the relative time shift between their dead-time windows. The results show that the dead-time varies by approximately 2.4 ns, with negligible 3σ dispersion, further confirming the robustness of the proposed dead-time generator and level-shifter circuits against mismatch effects.

In principle, non-simultaneous switching of adjacent high-side and low-side devices could introduce transient voltage differences between neighbouring V_{OUT} nodes in Fig. 6(b). In the proposed architecture, such transients could only arise during falling transitions, if one V_{OUT} node were to be pulled down faster than an adjacent upper V_{OUT} node. However, the symmetric high-side and low-side signal paths of the HBC architecture, combined with the extremely low propagation delays (sub-0.5 ns) and the demonstrated robustness against mismatch and process variations, effectively prevent the occurrence of harmful transient voltages at the HBC outputs. This simulation-based prediction is experimentally validated in the following section.

6 Experimental Results

The proposed IC was fabricated using a 130-nm BCD technology featuring 5 V N-channel and P-channel LDMOS devices. The die layout, micrographs of two wire-bonded dies, and the corresponding test board are shown in Fig. 16. The total chip area is $3.4\,\mathrm{mm}^2$. To improve area efficiency and minimize routing resistance, the power pads are implemented both adjacent to the devices using circuit-under-pad (CUP) structures and directly above the active regions using bond-on-active-circuit (BOAC) pad structures.

The wire-bonded die was mounted on a two-layer printed circuit board (daughterboard) that includes one 0.1 μF and two 22 μF decoupling capacitors connected across the four battery terminals. For rapid characterization, a 50-contact card-edge connector was used to interface the daughterboard containing the wire-bonded chip. Each power pad was routed to four connector contacts to reduce contact resistance, while the input logic signals were routed to two contacts.

A separate test board (motherboard) was employed to evaluate the balancer functionality. It includes four 22 μF decoupling capacitors for each battery or supply input. Circuit control is provided by an FPGA, driven by a B-Box

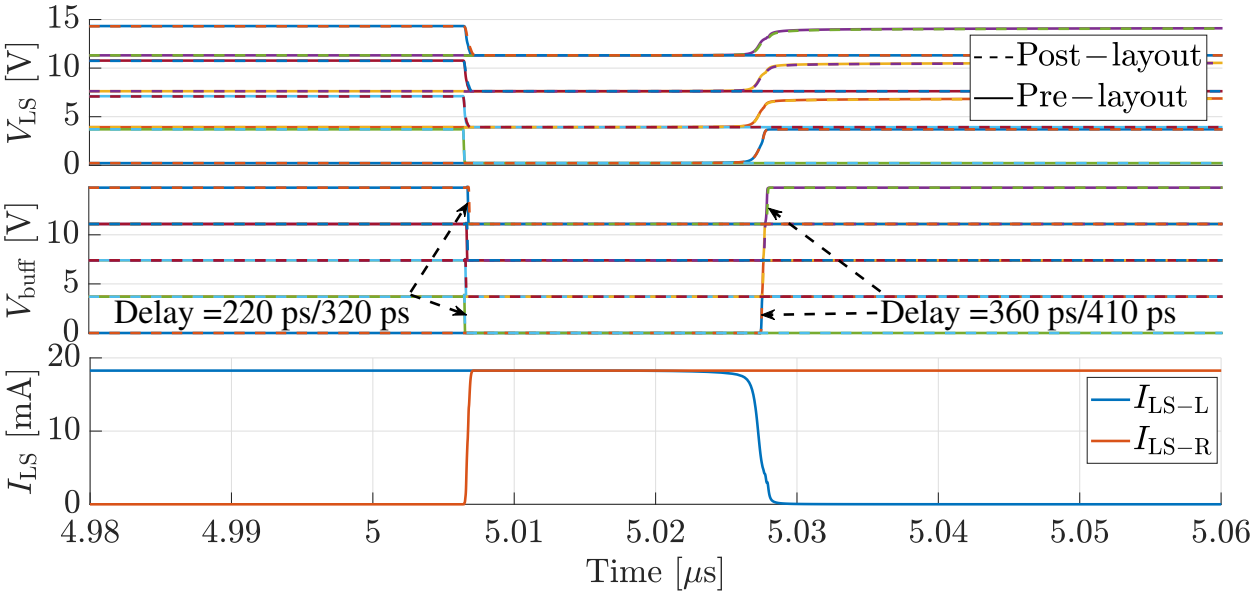

Figure 12: Multiple-output level-shifter voltage and current waveforms obtained from pre-layout schematic simulations and post-layout RCC parasitic simulations. V_{LS} denotes the direct output waveform (pre-buffer stage), V_{buff} is the post-buffer output waveform, and I_{LS} represents the current waveform in either branch of the level shifter.

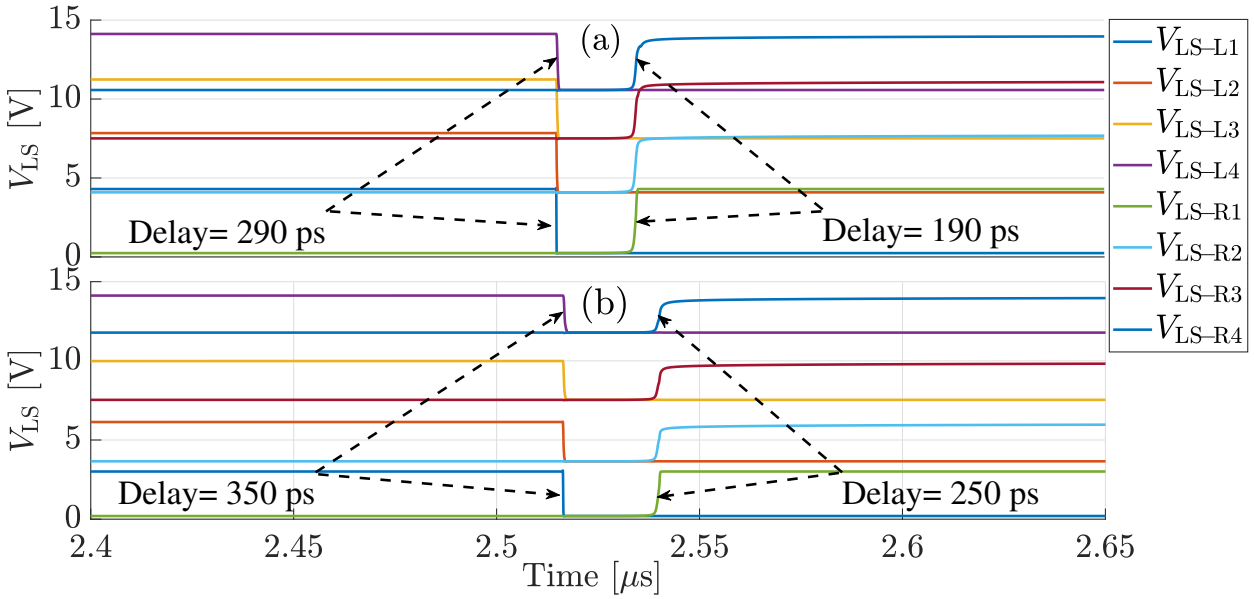

Figure 13: Post-layout RCC simulations of the level shifter under two different battery voltage distributions (V_1 to V_4): (a) 3.01 V, 3.44 V, 3.87 V, and 4.3 V; and (b) 4.3 V, 3.87 V, 3.44 V, and 3.01 V.

microcontroller, and allows operation over a switching frequency range from 1 kHz to 5 MHz. To validate the chip functionality as a battery voltage balancer, the test setup shown in Fig. 17 was implemented as in Fig. 18. The test board was connected to four Keithley 2281S-20-6 units, which can operate either as battery emulators or as programmable voltage supplies connected in series. These devices provide voltages in the range of 2.4 V to 4.3 V and emulate a 3.7 V Li-ion battery model.

A summary of the experimental parameters is provided in Table 2. Two 16 V, 100 μF ceramic capacitors connected in parallel were used at the output of each half-bridge in a star configuration. These capacitors exhibit a self-resonant frequency in the range of 200–250 kHz and an equivalent series resistance of approximately 10 mΩ.

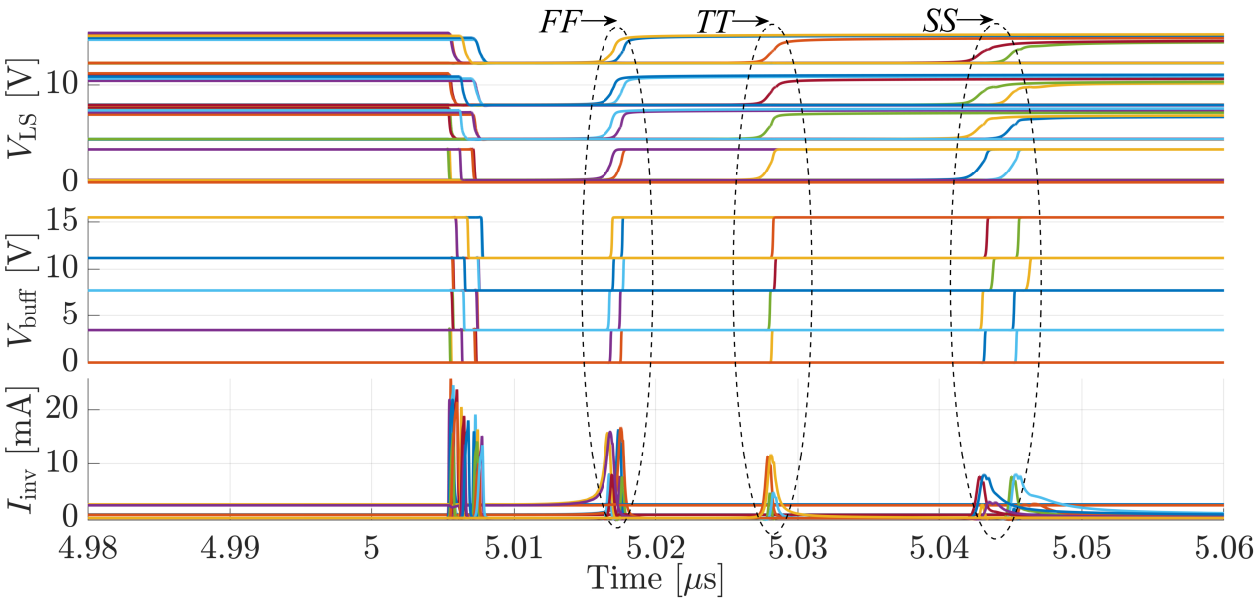

Figure 14: PVT simulations of the level shifter with RCC post-layout parasitics, including fast–fast (FF), typical–typical (TT), and slow–slow (SS) process corners. Simulations are performed at temperatures of $-20\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ for each corner. The cell voltages from V_1 to V_4 are 3.44 V, 4.3 V, 3.44 V, and 4.3 V, respectively.

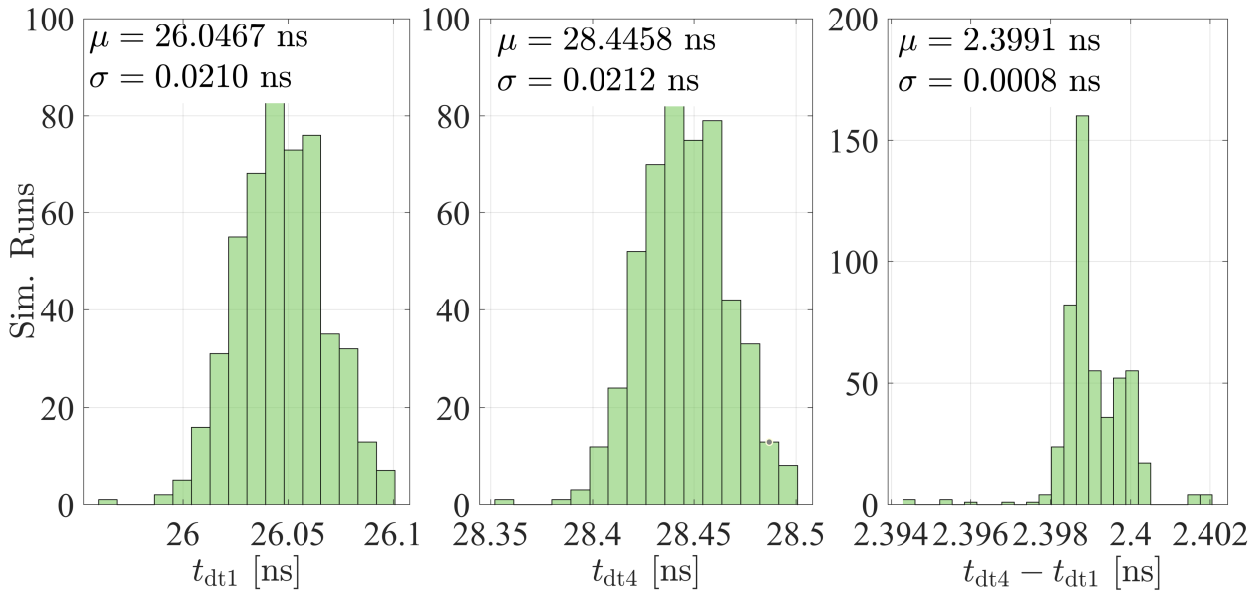

Figure 15: Mismatch Monte Carlo simulations of the level shifter with RCC post-layout parasitics. The cell voltages are all set to 2.5 V to illustrate the worst-case condition.

To fully characterize the proposed battery balancer IC, a comprehensive set of tests was conducted under both balanced and imbalanced conditions.

6.1 IC Characterization Under Balanced Condition

In the absence of voltage mismatches or imbalances among the input DC sources, both the balancing currents through the DC sources and the capacitor currents are ideally zero. Consequently, the only current flowing through the cells corresponds to the chip bias current under the presence of the PWM control signals, where the IC draws approximately

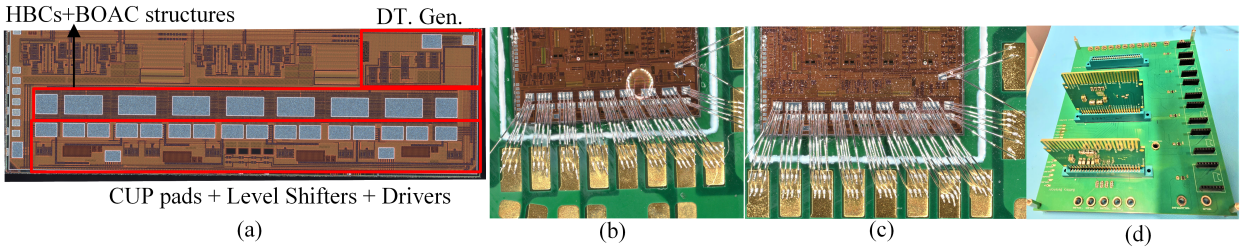

Figure 16: (a) Chip layout including stacked half bridges (HBCs), dead-time generation circuit (DT Gen.), voltage level shifters, bond-on-active-circuit (BOAC) pads, and circuit-under-pad (CUP) structures, with a total layout area of 3.4 mm^2. (b)–(c) Balancer dies bonded using 33 μm aluminum wire bonds and mounted on two-layer daughterboards. (d) Test board with the daughterboards inserted into edge-connector sockets.

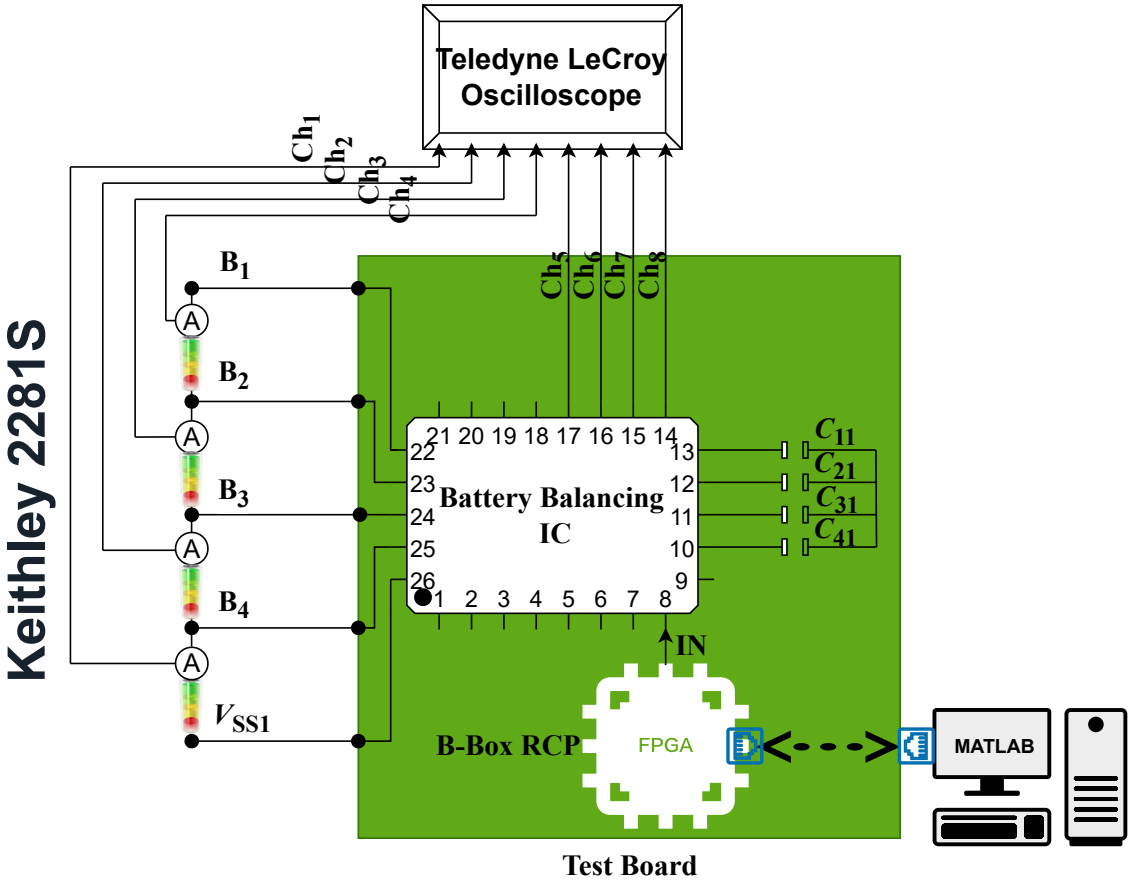

Figure 17: Testbench schematic of the IC balancer

18 mA. To experimentally validate the fabricated balancer ICs under this operating condition, all inputs were set to the extreme voltage levels of 2.5 V and 4.3 V, and the ICs were operated at switching frequencies of 1 kHz and 1 MHz.

Two ICs were operated in complementary mode, as discussed in Fig. 7. The measured complementary switching node voltages, (V_{OUT11}, V_{OUT12}, …, V_{OUT41}, V_{OUT42}), of all half-bridge submodules are shown in Fig. 19. Furthermore, the corresponding voltages across the four balancing capacitors on the IC1 side of Fig. 7, namely V_{C11}, V_{C12}, V_{C31}, and V_{C41}, are presented in Fig. 20. The measured bus voltages at the common plates of the balancing capacitors, denoted as V_{BUS1} and V_{BUS2} in Fig. 7, are presented in Fig. 21 under identical voltage and switching-frequency conditions. In

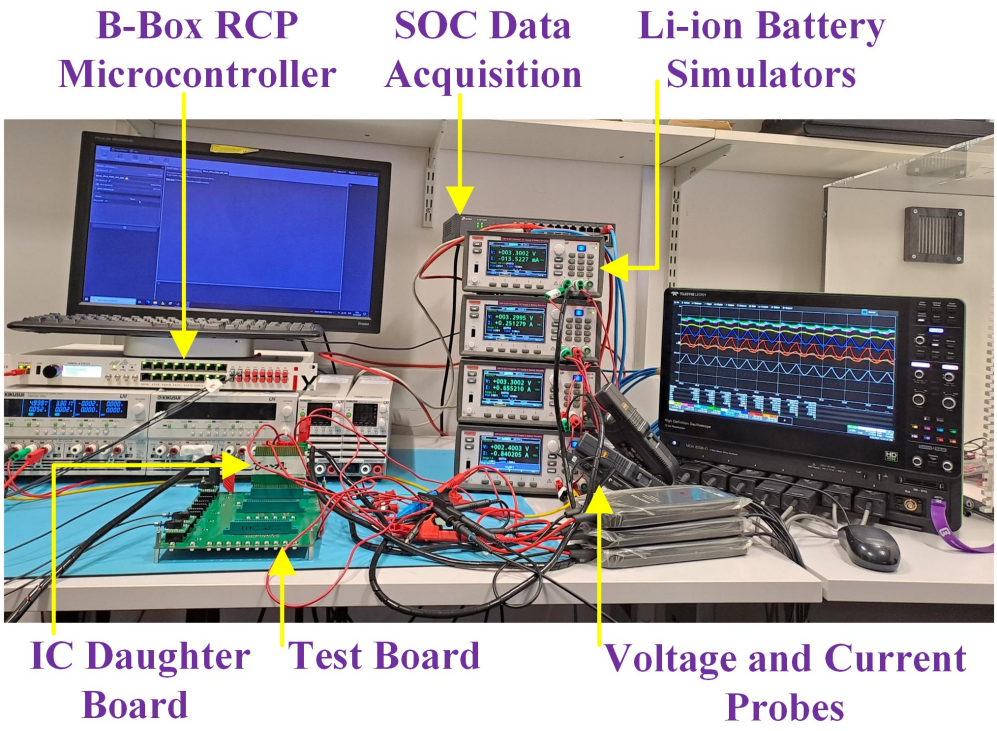

Figure 18: Testbench setup including the test board, chip daughterboard, power supplies and battery simulators, FPGA-based B-box microcontroller, SOC data acquisition system, current and voltage probes, and an oscilloscope.

Table 2: Experimental Parameters

Parameter	**Value**
Balancing capacitors	2 x 100 μF MLCC, 16 V, 20%
Daughterboard Decoupling	0.1 μF+2 × 22 μF
Motherboard Decoupling	4 × 22 μF
Input voltage range	2.4-4.3 V
Frequency range	1 kHz-5 MHz
Wire-bonds per pad	6-8 AL 33 μm wires
Supplies and Battery Emulators	Keithley 2281S-20-6

addition, the voltages between adjacent switching nodes of IC1 side, i.e., $(V_{\mathrm{OUT11}} - V_{\mathrm{OUT21}})$, $(V_{\mathrm{OUT21}} - V_{\mathrm{OUT31}})$, and $(V_{\mathrm{OUT31}} - V_{\mathrm{OUT41}})$, are shown in Fig. 22. These results confirm the absence of voltage spikes or over-voltage transients around the switching instants.

The measurements are in close agreement with both analytical predictions and simulation results. The complementary outputs exhibit fast rising and falling edges, thereby validating the correct operation of the multiple-output level shifter and its capability for low-delay level shifting.

Moreover, the algebraic sum of the capacitor voltages is equal to zero, in accordance with (2). During each switching phase, the bus voltages V_{BUS1} and V_{BUS2} can be expressed as weighted averages of the battery cell voltages, which is also consistent with (2).

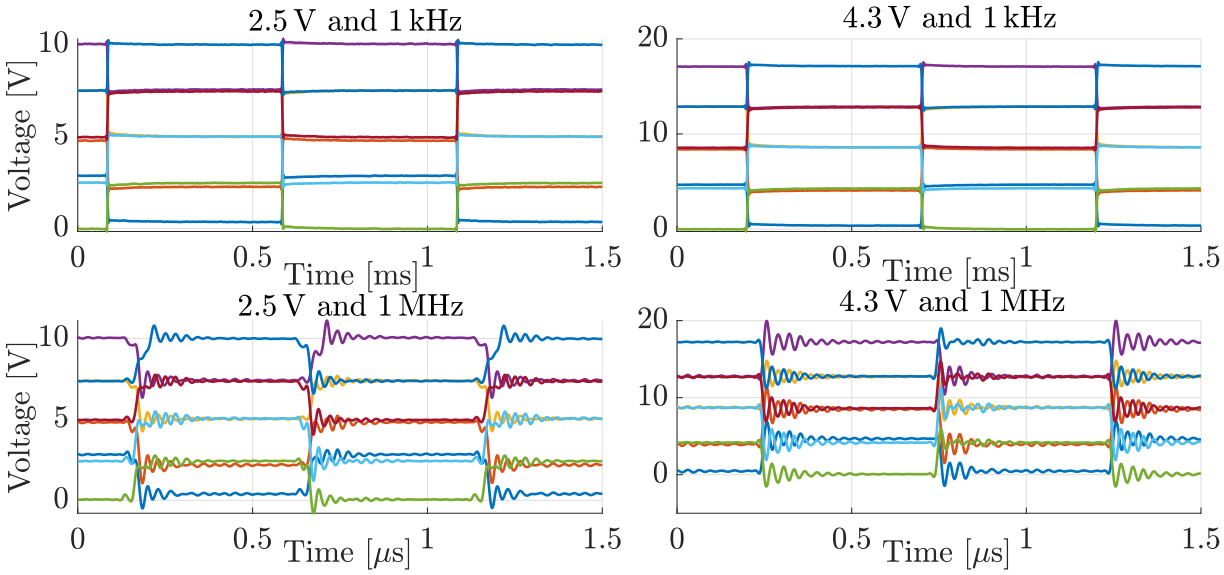

Figure 19: Output voltage waveforms of complementary half-bridge submodules (V_{OUT11}, V_{OUT12}, …, V_{OUT41}, V_{OUT42} as denoted in Fig. 7) at input cell voltages of 2.5 V and 4.3 V, and switching frequencies of 1 kHz and 1 MHz under balanced operating conditions.

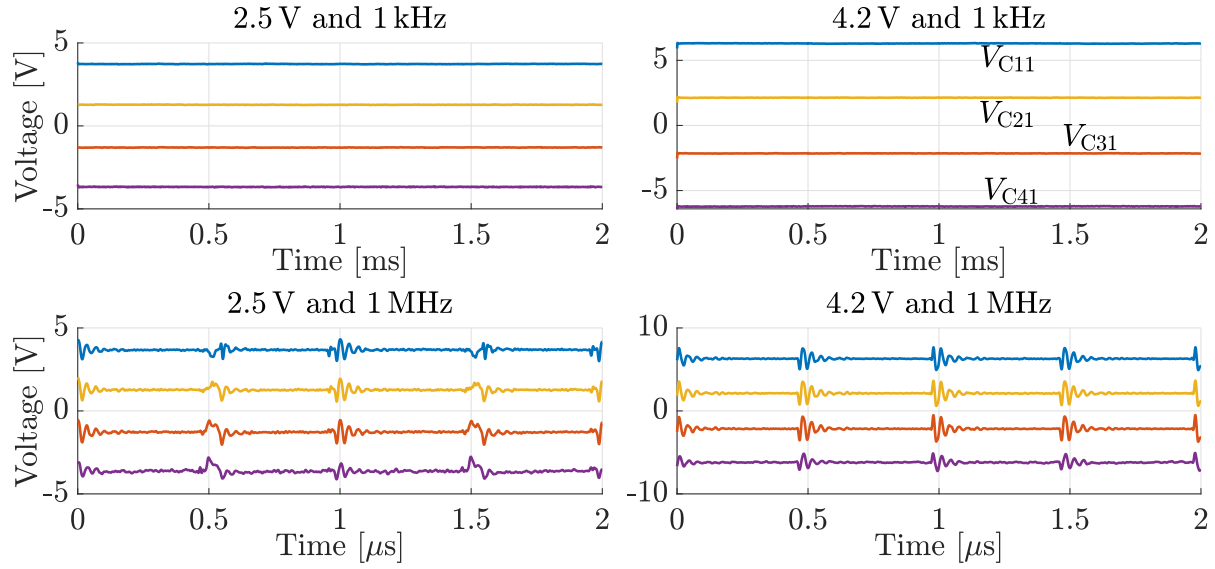

Figure 20: Balancing capacitor voltage waveforms (V_{C11}, V_{C12}, V_{C31}, and V_{C41}, as shown in Fig. 7) at input cell voltages of 2.5 V and 4.2 V, and switching frequencies of 1 kHz and 1 MHz under balanced operating conditions.

These fundamental results validate several critical design aspects. First, the functionality of the BOAC pads, CUP structures, and the adopted switch layout and termination strategy are verified, demonstrating reliable operation with wedge–wedge Al wire bonding. Second, the results confirm the capability of high-frequency switching up to 1 MHz over a wide input-voltage range that fully covers the Li-ion battery cell operating window. This further demonstrates the proper functionality of the LDMOS switches and their excellent dynamic performance. In addition, the successful operation of the IC experimentally validates the proposed driver-rail generation method based on internal switching nodes, as discussed in the circuit implementation.

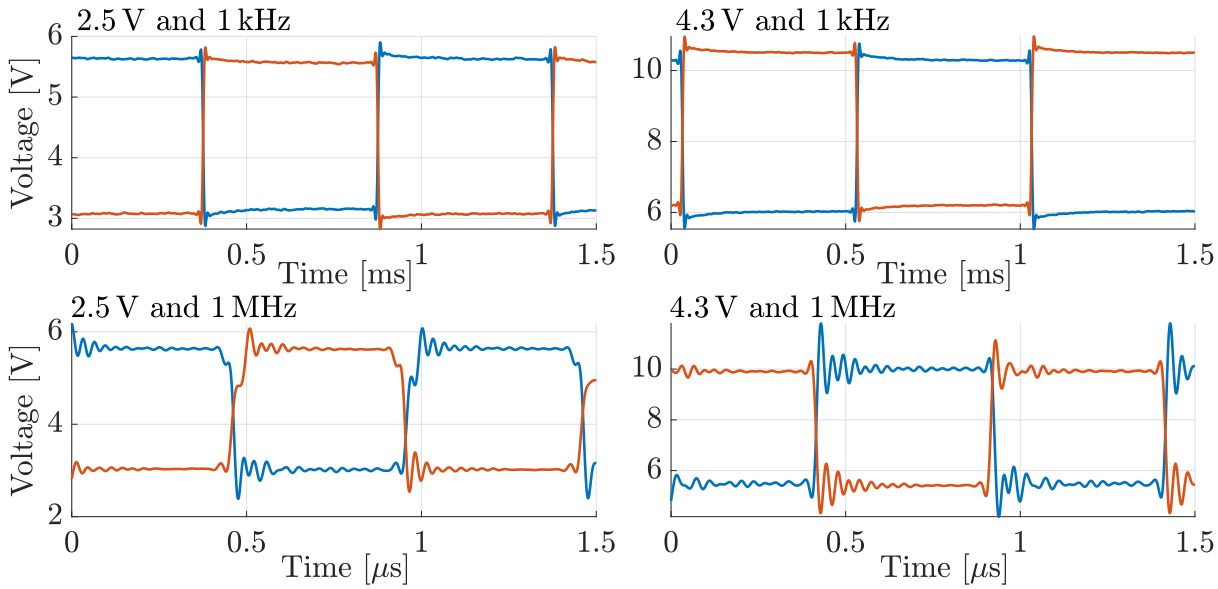

Figure 21: Bus voltage waveforms (V_{BUS1} and V_{BUS2}, as shown in Fig. 7) at input cell voltages of 2.5 V and 4.3 V, and switching frequencies of 1 kHz and 1 MHz under balanced operating conditions.

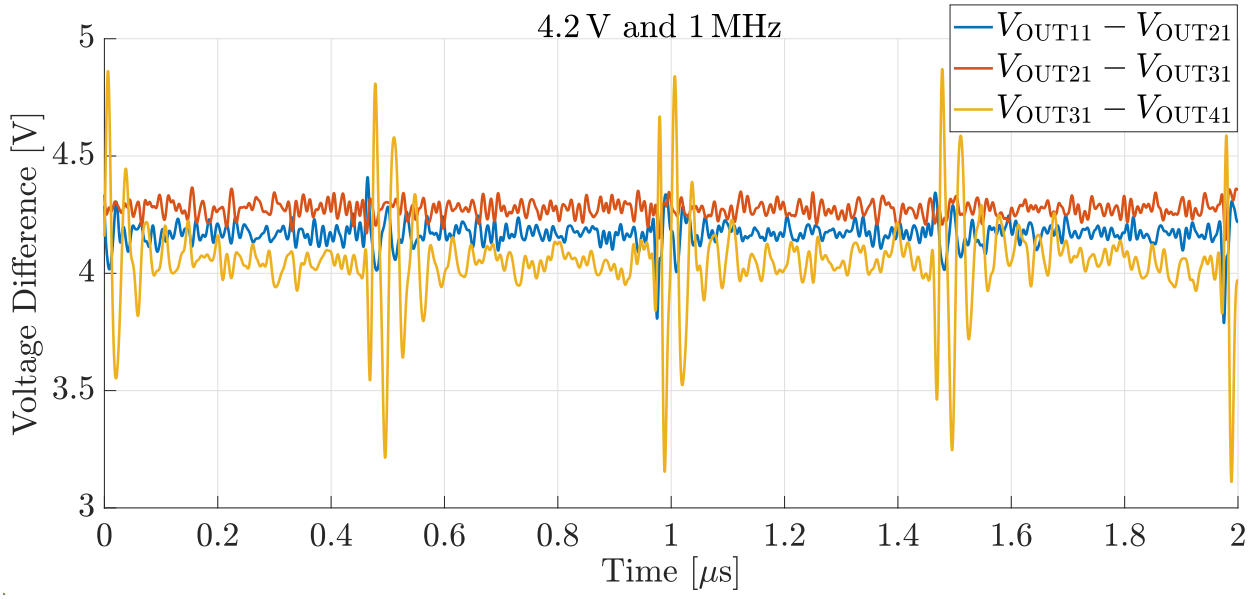

Figure 22: Differential output voltage waveforms at input cell voltages of 4.2 V and a switching frequency of 1 MHz under balanced operating conditions.

6.2 Operation Under Imbalance Conditions

To evaluate the balancing current capability of a single IC, the average balancing current sourced or sunk was measured over a switching frequency range from 8 kHz to 500 kHz while the voltages of the topmost cell and the third cell were varied from 2.4 V to 4.2 V, with all other cells fixed at 3.3 V, as shown in Fig. 23. As expected, the average current increases approximately linearly with the voltage imbalance at each switching frequency, validating the automatic energy-transfer characteristic of the balancing IC. In addition, the balancing current increases with the switching frequency. For example, when the topmost cell voltage is 4.2 V and all other cells are at 3.3 V, the average balancing current rises from approximately 0.5 A at 8 kHz to about 1.25 A at both 250 kHz and 500 kHz. Beyond the

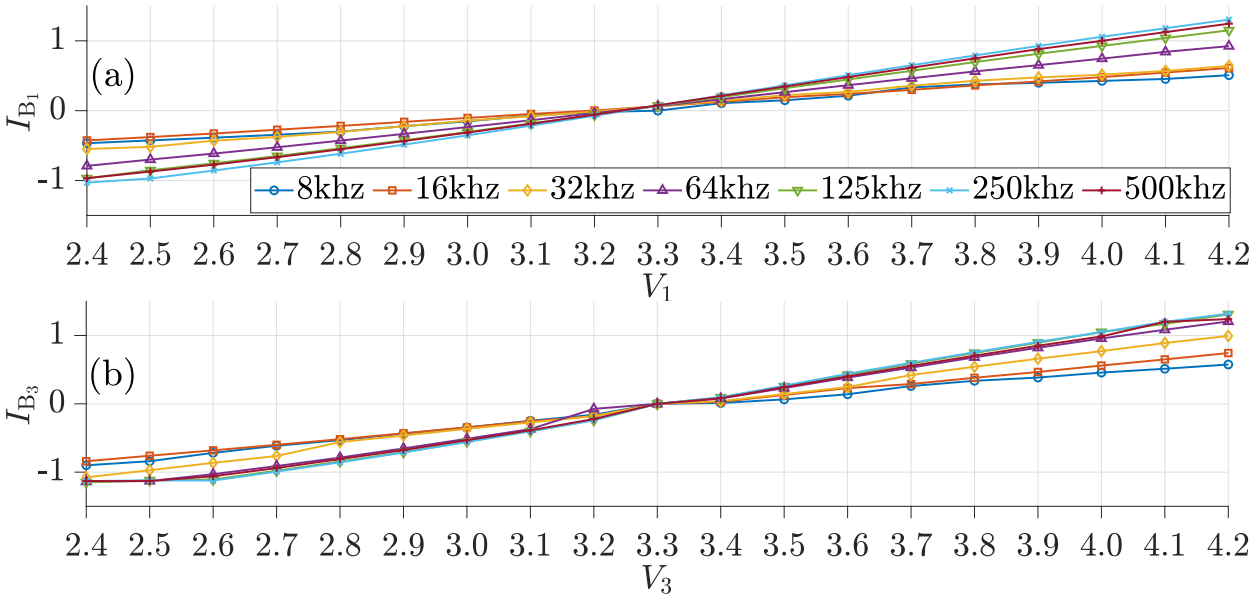

Figure 23: Average battery balancing current variation with voltage imbalance at switching frequencies from 8 kHz to 500 kHz: (a) sweeping the top-most cell voltage (V_1) from 2.4 V to 4.2 V with all other cells fixed at 3.3 V, and (b) sweeping the third cell voltage (V_3) from 2.4 V to 4.2 V with all other cells fixed at 3.3 V.

125 kHz–250 kHz range, the balancing current starts to slightly decrease due to the effects of parasitic inductances; this phenomenon is examined in more detail later.

A similar behavior is observed when the third cell voltage is imbalanced with respect to the remaining cells: it sinks current when its voltage is below 3.3 V and sources current when it exceeds 3.3 V. Furthermore, when all cells are at 3.3 V, corresponding to the balanced condition, the measured current reduces to the IC bias current. The slight variations in the current characteristics with respect to frequency and voltage imbalance observed in the two scenarios of Fig. 23 are primarily attributed to mismatches in the PCB routing paths of the balancing capacitors and wire bonding, as well as to minor inconsistencies introduced by the measurement cables and current probes.

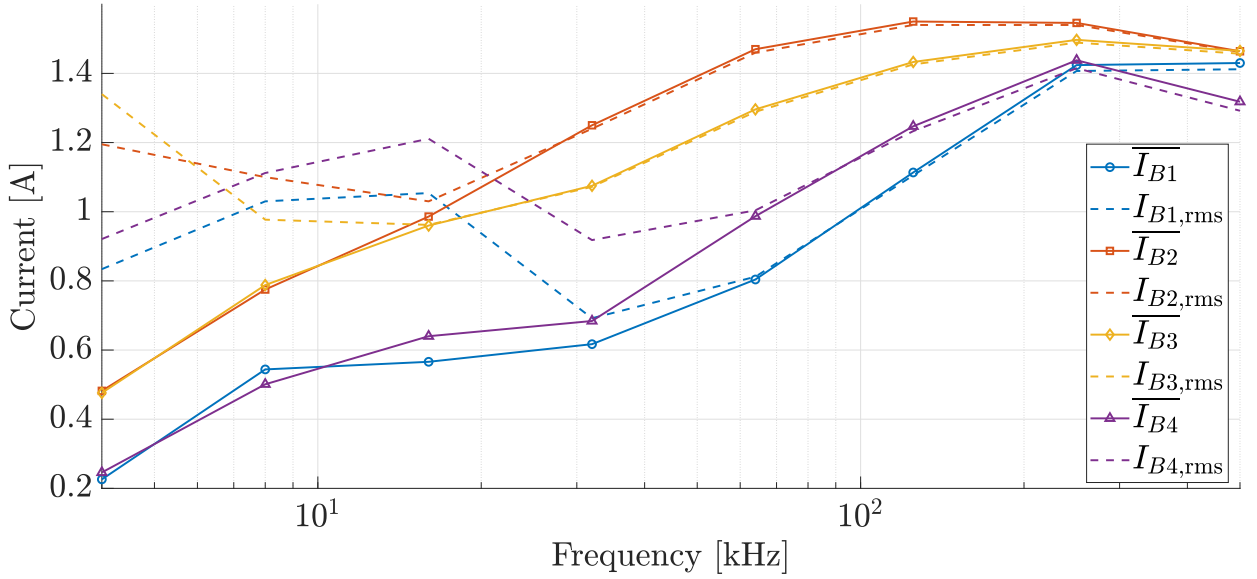

Figure 24: Effect of switching frequency on the average and RMS battery balancing currents of all cells for a fixed imbalance condition.

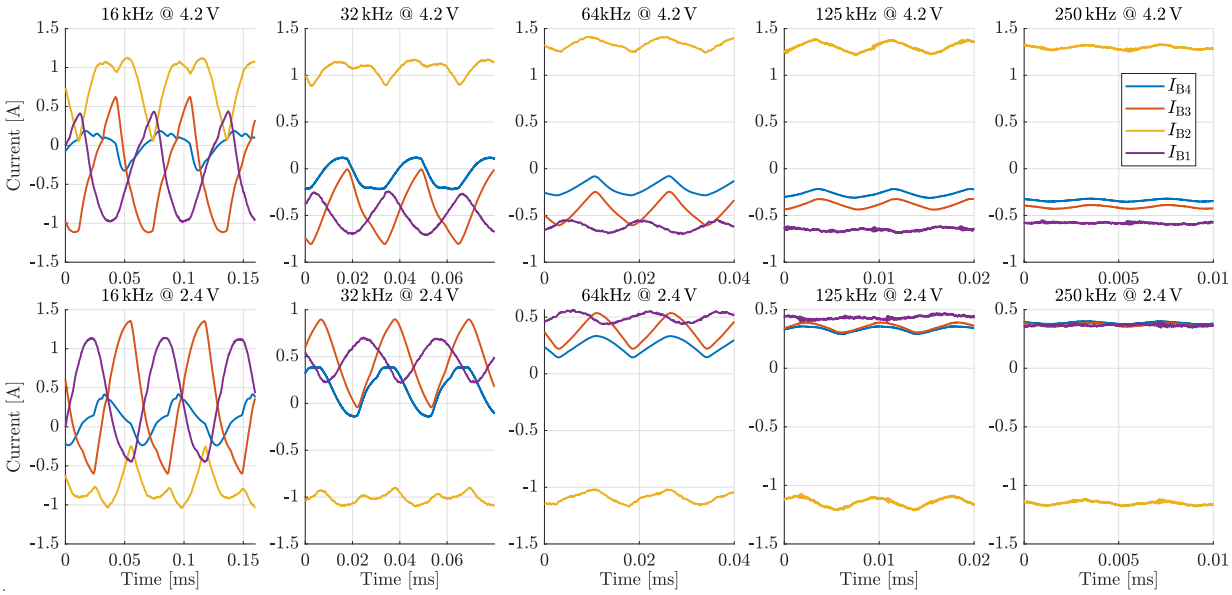

Figure 25: Battery balancing current waveforms of the four cells with the second cell voltage (V_2) set to 4.2 V and 2.4 V, while the remaining cells are fixed at 3.3 V, across different switching frequencies.

The average and RMS balancing currents were measured over a switching-frequency range from 4 kHz to 500 kHz, where each cell was individually set to the maximum voltage of 4.2 V while the remaining cells were fixed at 3.3 V, as shown in Fig. 24. The results validate the convergence of the average and RMS balancing currents for each cell beyond certain switching frequencies. For the terminal cells (topmost and bottom-most), this convergence occurs at approximately 60 kHz, while for the middle cells it occurs at roughly half this frequency. This difference arises because the current in the middle cells is continuous, whereas the current in the terminal cells is discontinuous, as they are disconnected for half of the switching cycle. It is also observed that the balancing currents start to decrease beyond approximately 250 kHz due to the parasitic effects.

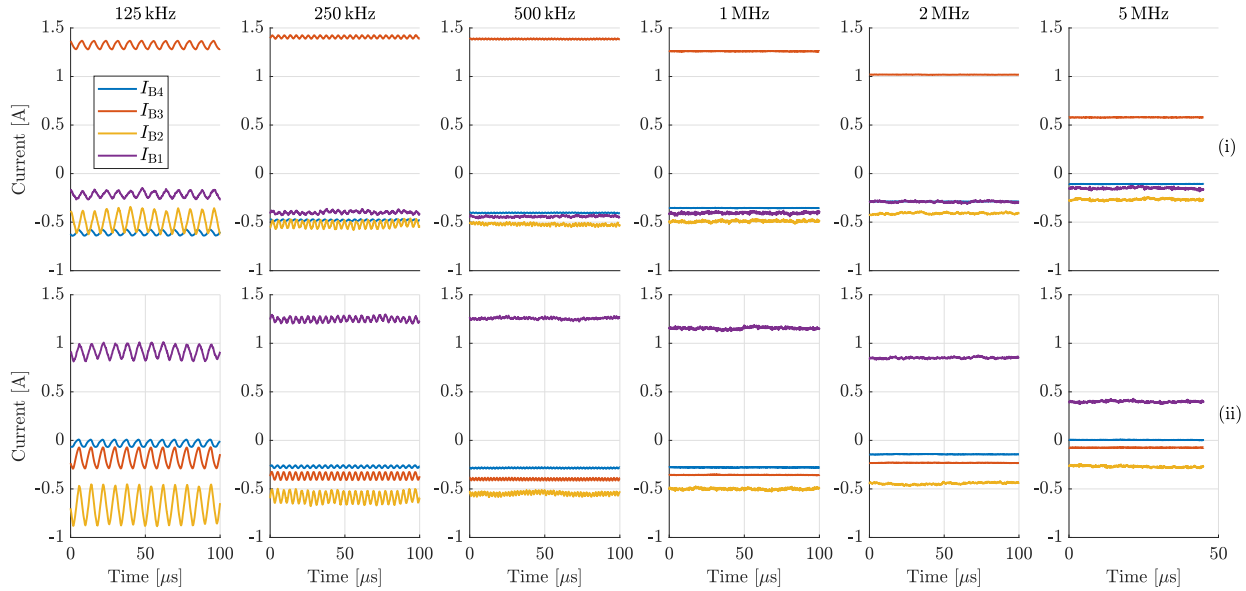

Figure 26: Effects of parasitic inductances in the balancing path on the battery balancing currents at high switching frequencies, with currents measured from 125 kHz to 5 MHz under two imbalance scenarios: (i) V_3 set to 4.2 V with the remaining cells fixed at 3.3 V, and (ii) V_1 set to 4.2 V with the remaining cells fixed at 3.3 V.

Therefore, operating at frequencies above the point where the average and RMS currents become nearly equal (i.e., their ratio approaches unity) is recommended, as it reduces self-heating in both the battery cells and the IC while still ensuring fast balancing performance. Overall, the observed convergence behavior between the RMS and average currents is consistent with the simulation and analytical results presented in Fig. 9. However, the presence of a low-pass filter at the IC input terminals, formed by the decoupling capacitors (approximately $140\,\mu$F) and the cable inductance (approximately $1\,\mu$H), causes the measured balancing current to become continuous at higher switching frequencies and hence to converge toward the RMS current. This behavior differs from the ideal case examined in Fig. 9, where the ratio of RMS to average current remains high (around 1.4 and 4.4) even at high switching frequencies.

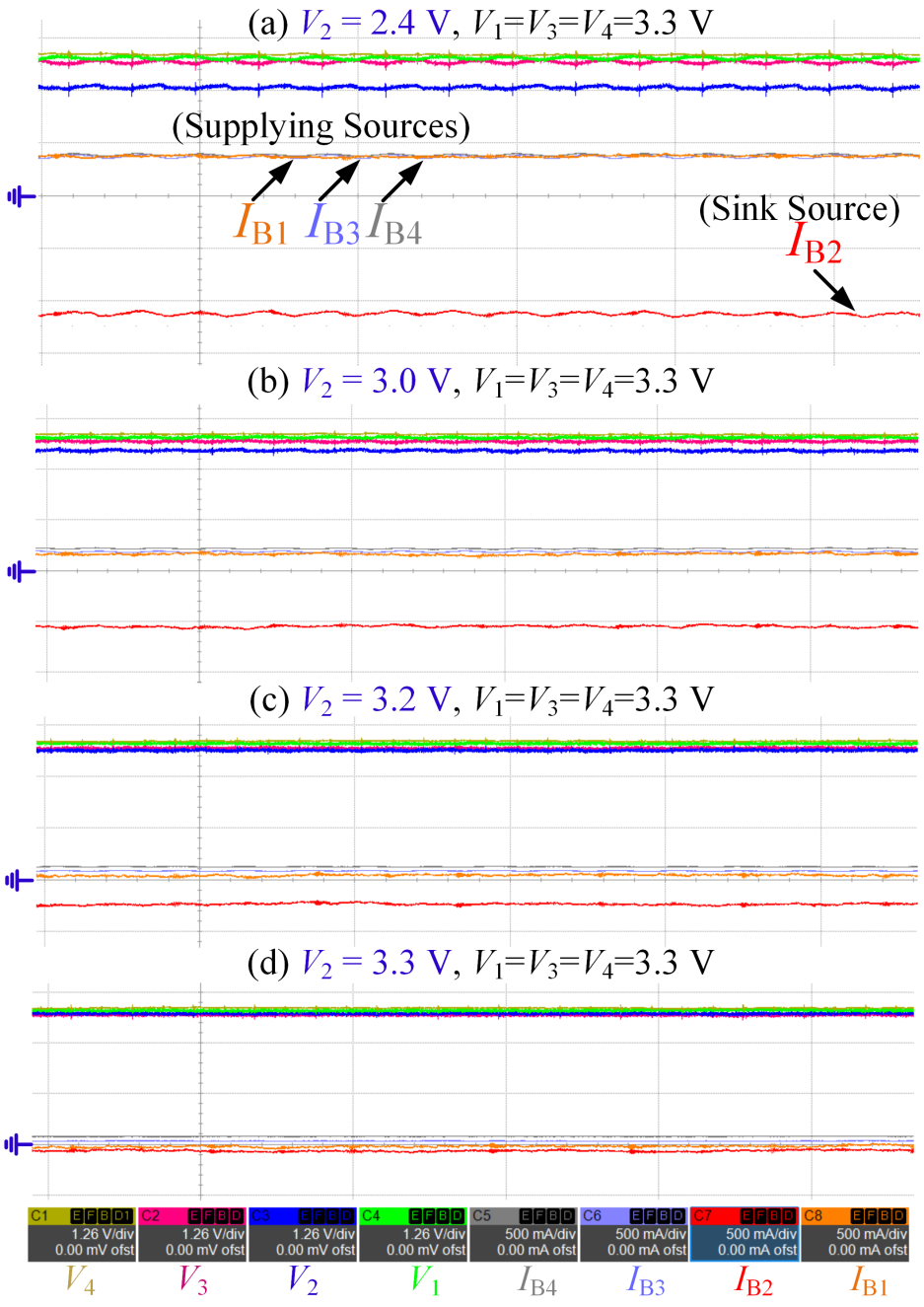

Figure 27: The convergence of balancing currents toward the chip bias current as balanced conditions are reached.

Measured balancing current waveforms are shown in Fig. 25 for switching frequencies ranging from 16 kHz to 250 kHz, where the second cell voltage (V_2) is set to 4.2 V and 2.4 V, respectively, while the remaining cells are fixed at 3.3 V.

It can be observed that when the second cell voltage is 4.2 V, it exhibits a positive balancing current waveform I_{B2}, whereas the other cells at 3.3 V exhibit negative current waveforms I_{B1}, I_{B3}, and I_{B4}, indicating that they are receiving energy. The opposite behavior is observed when the second cell voltage is set to 2.4 V, where I_{B2} becomes negative and the remaining cells source current.

The current waveforms increase gradually with the switching frequency and evolve into predominantly unidirectional waveforms beyond approximately 32 kHz. This behavior indicates a transition from the slow-switching regime to the fast-switching regime, in which the current is mainly limited by the equivalent switch resistances, PCB routing resistances, and other parasitic resistive elements in the current paths. This trend continues as the effective path resistance decreases, until the resonance frequency is approached. Beyond this point, the parasitic inductances of the interconnections and components begin to dominate and impede further increases in the balancing current. The impact of the parasitic inductances on balancing currents is further illustrated in Fig. 26, where the switching frequency is increased up to 5 MHz. Overall, operation near 500 kHz achieves the maximum balancing capability of the IC for the selected balancing capacitance.

To validate the convergence of the balancing currents toward the chip bias current, Fig. 27 expands upon the case shown in Fig. 25 by illustrating the cell voltages and corresponding balancing currents at a switching frequency of 250 kHz, when V_2 is set to 2.4 V, 3.0 V, 3.2 V, and 3.3 V.

To characterize the IC capability in balancing cells with initially different SOCs, three scenarios with distinct SOC distributions were evaluated, all measured at a switching frequency of 250 kHz, as shown in Fig. 28. The results show that the IC is able to balance the battery cells to within a maximum SOC difference of 1%. The differences in balancing time among the scenarios are attributed to the inherent asymmetry of the circuit, in which the middle cells experience higher balancing currents than the terminal cells. This asymmetry is addressed in the complementary IC operation, where the balancing speeds become less dependent on the location of the cells within the string.

The thermal performance of the IC is shown in Fig. 29 for the case of maximum imbalance applied to the top-most cell at a switching frequency of 250 kHz. The chip temperature rises to approximately 65 °C without any additional external cooling.

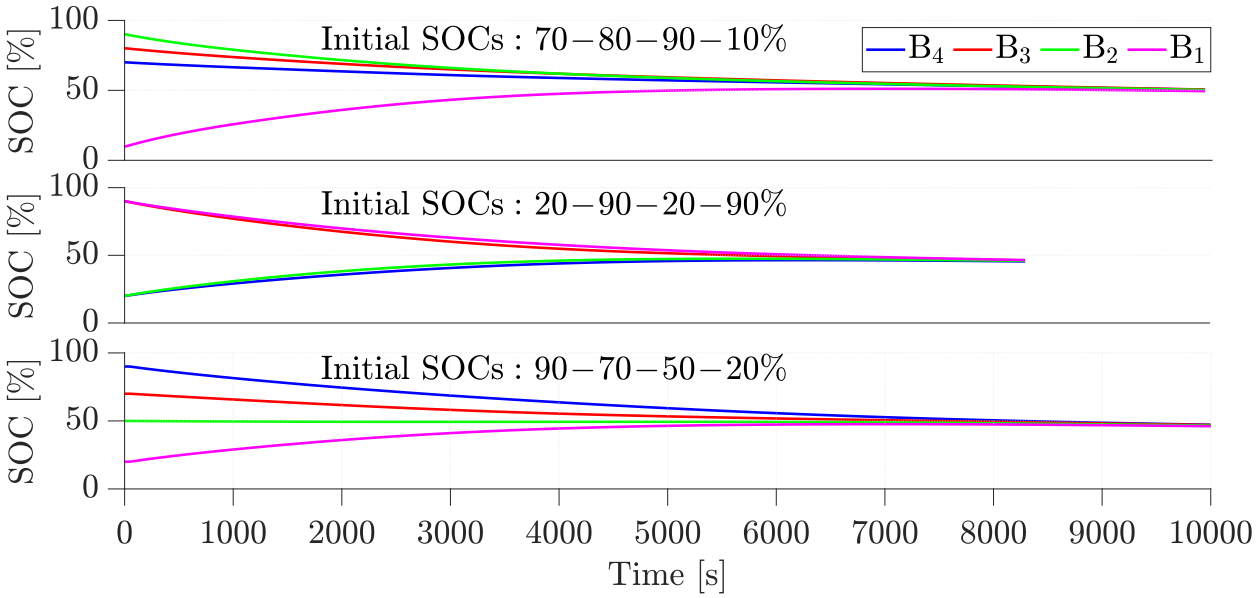

Figure 28: Balancing performance of the active IC balancer across three distinct initial battery SOC distributions at 250 kHz for a cell capacity of 500 mAh, with balancing terminated when the maximum SOC difference among cells is reduced to 1%.

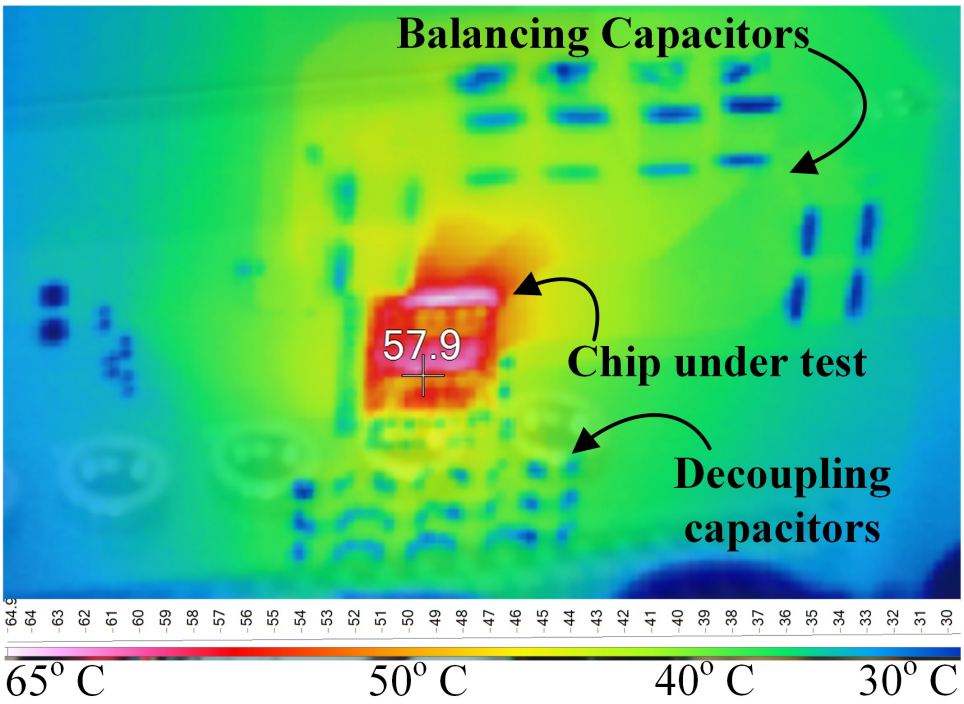

Figure 29: Temperature rise due to balancing currents when the top-most cell is set to 4.3 V and the remaining cells are fixed at 3.3 V.

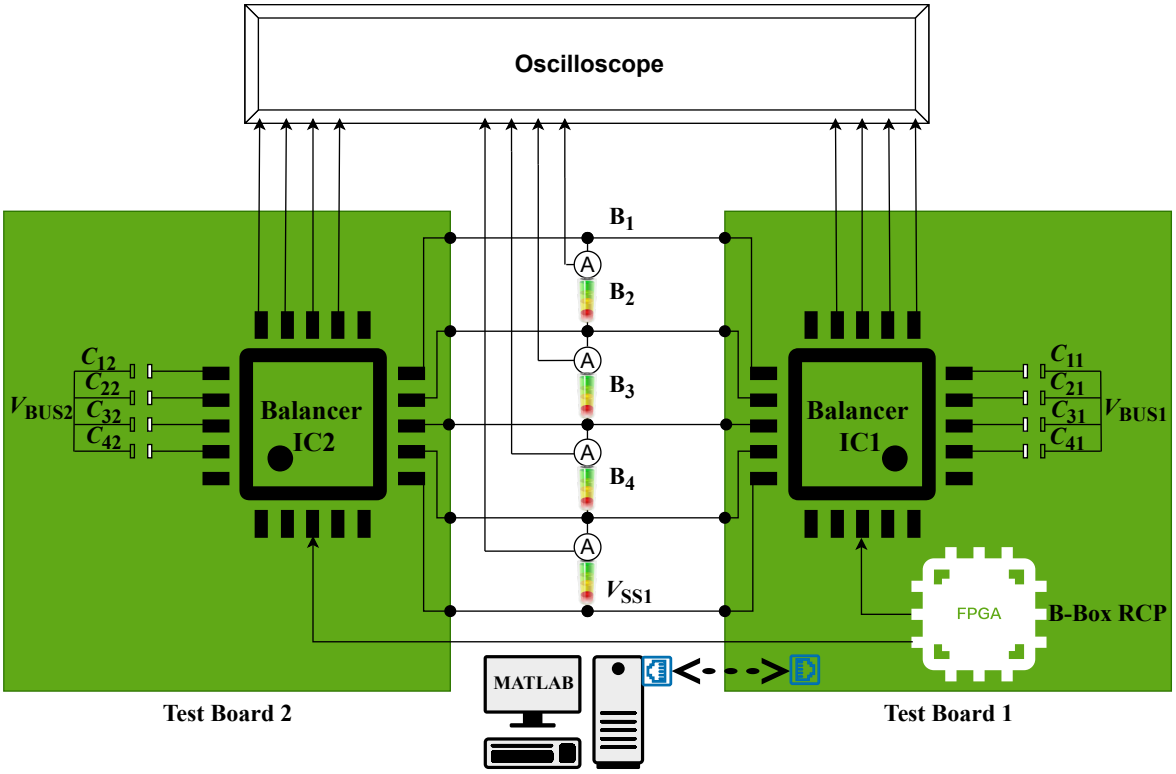

Figure 30: Testbench schematic of the complementary dual-IC balancer

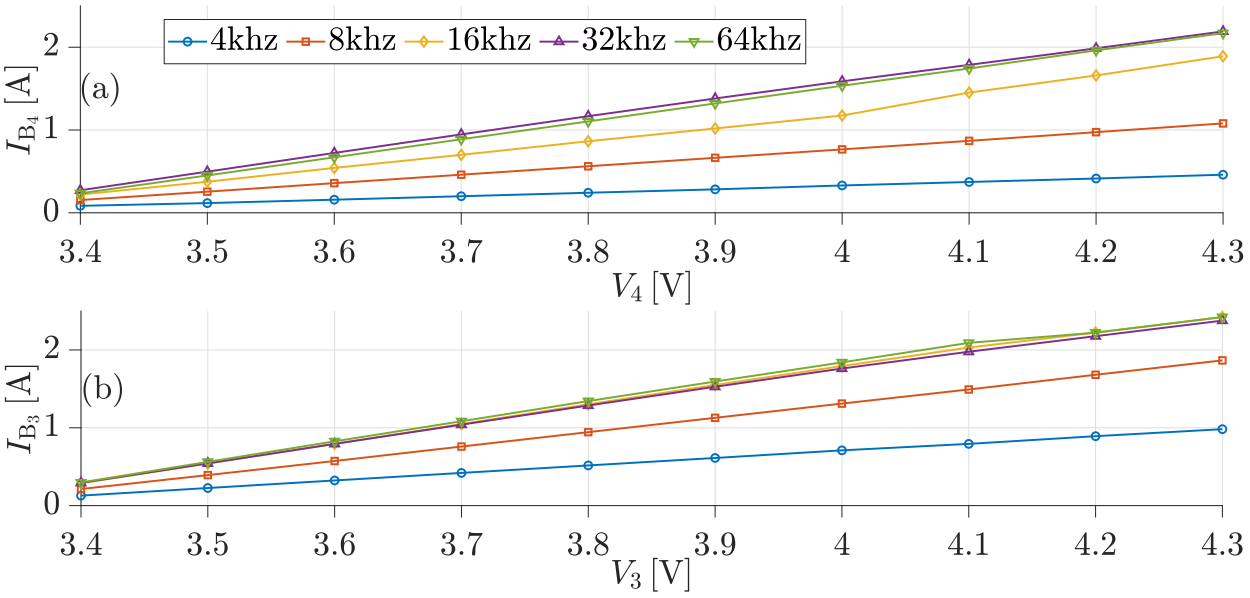

Figure 31: Average battery balancing current variation with voltage imbalance at switching frequencies from 4 kHz to 64 kHz: (a) sweeping the top-most cell voltage (V_4) from 3.4 V to 4.3 V with all other cells fixed at 3.3 V, and (b) sweeping the third cell voltage (V_3) from 3.4 V to 4.3 V with all other cells fixed at 3.3 V.

6.3 Complementary Dual-IC Balancer

To enhance the balancing speed and increase the ratio of the average balancing current to the RMS current, the full-bridge-based balancer discussed in Fig. 7 was evaluated by configuring the two ICs shown in Fig. 16(b–c) together with the test board in Fig. 16(d) as demonstrated in Fig. 30. The obtained results are comparatively discussed against those of the single-IC balancer.

The average balancing current sourced or sunk by each supply over a switching-frequency range of 4 kHz to 64 kHz is shown in Fig. 31. The currents exhibit trends with respect to switching frequency and voltage imbalance that are similar to those observed in the single-IC operation. However, their magnitudes are more linear and nearly doubled compared to the results in Fig. 23, reaching approximately 2.5 A when one cell is at the highest potential and the remaining cells are at 3.3 V. Notably, this performance is achieved at much lower switching frequencies (32–64 kHz), compared to the 250–500 kHz required in the single-IC configuration.

This represents a significant advantage, as it enables a substantial reduction in the required balancing capacitance while allowing operation at higher effective balancing currents without incurring high dynamic losses. Consequently, this approach provides considerable cost benefits, particularly for longer battery strings, where the terminal capacitors must be rated for approximately half of the total string voltage.

Balancing current waveforms are presented in Fig. 32 and Fig. 33 for switching frequencies ranging from 4 kHz to 64 kHz. In Fig. 32, the top-most supply, B_4, is set to 4.2 V while the remaining supplies are fixed at 3.3 V. As a result, B_1 exhibits a positive current waveform I_{B1} that increases with switching frequency, becoming predominantly unidirectional from approximately 8 kHz upward. Similarly, when B_2 is set to 4.2 V, the current I_{B2} transitions from a high-ripple waveform to one with a larger average value above 8 kHz, approaching an optimal current distribution among all supplies at 32 kHz. This indicates that the balancer achieves its highest balancing speed near this frequency.

At lower switching frequencies (below $\sim$8 kHz), the system operates in the SSL, where the equivalent impedance is dominated by the balancing capacitors. As the frequency increases, the operation shifts to FSL, in which the entire switching cycle is utilized for charging and discharging the balancing capacitors. In this regime, energy transfer between higher-voltage and lower-voltage cells is maximized, accelerating the balancing process. The balancing current in the FSL is primarily limited by the on-resistance of the switches, PCB routings, and other parasitic resistances in the current path. At even higher frequencies (beyond 64 kHz), further increases in current are constrained by the parasitic input and output inductances, as was characterized for single IC balancer in Fig. 26.

The average and RMS balancing currents were measured over the switching-frequency range of 4 kHz to 128 kHz, as shown in Fig. 34. The results indicate a high ratio of average to RMS balancing current, particularly for frequencies

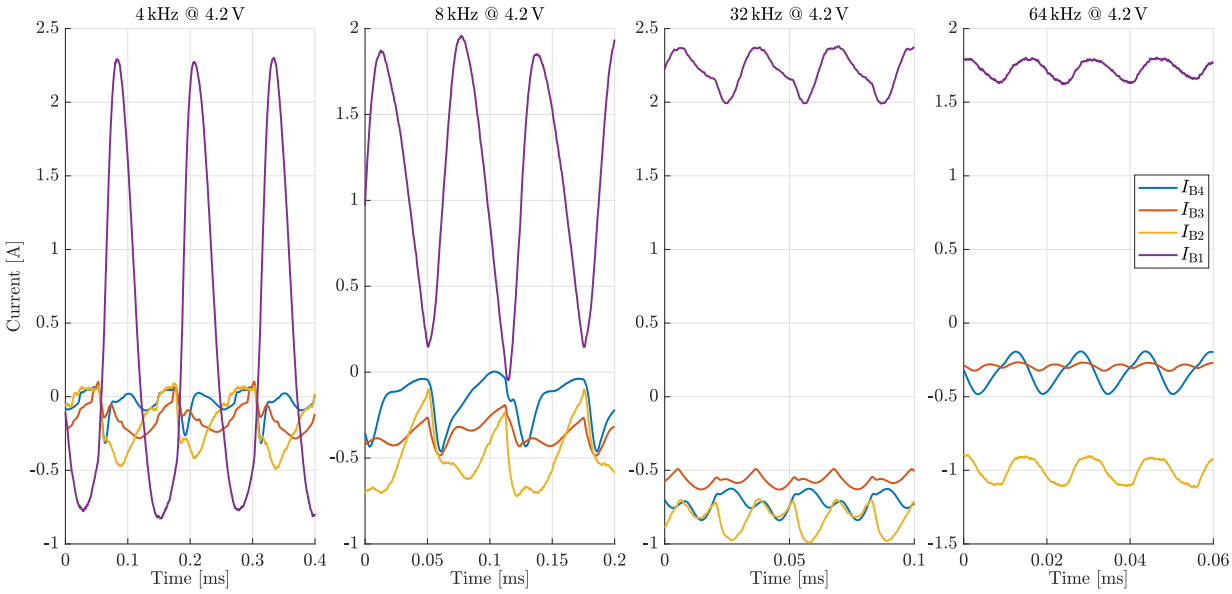

Figure 32: Battery balancing current waveforms of the four cells with the top-most cell voltage (V_1) set to 4.2 V, while the remaining cells are fixed at 3.3 V, across different switching frequencies.

above 20 kHz, where the ratio approaches unity for all battery cells. This characteristic enables faster balancing with reduced self-heating and lower conduction losses, facilitated by the continuous current delivery inherent to the complementary operation of the stacked half-bridge sub-modules. In contrast, Fig. 24 presented the average and RMS currents for a stacked half-bridge circuit (representing one half of the complementary topology). Overall, the average balancing currents are approximately half as large for all cells, and the terminal cells (B1 and B4) achieve a similar DC-to-RMS current ratio only at significantly higher frequencies, approximately four times those required in the complementary stacked half-bridge case.

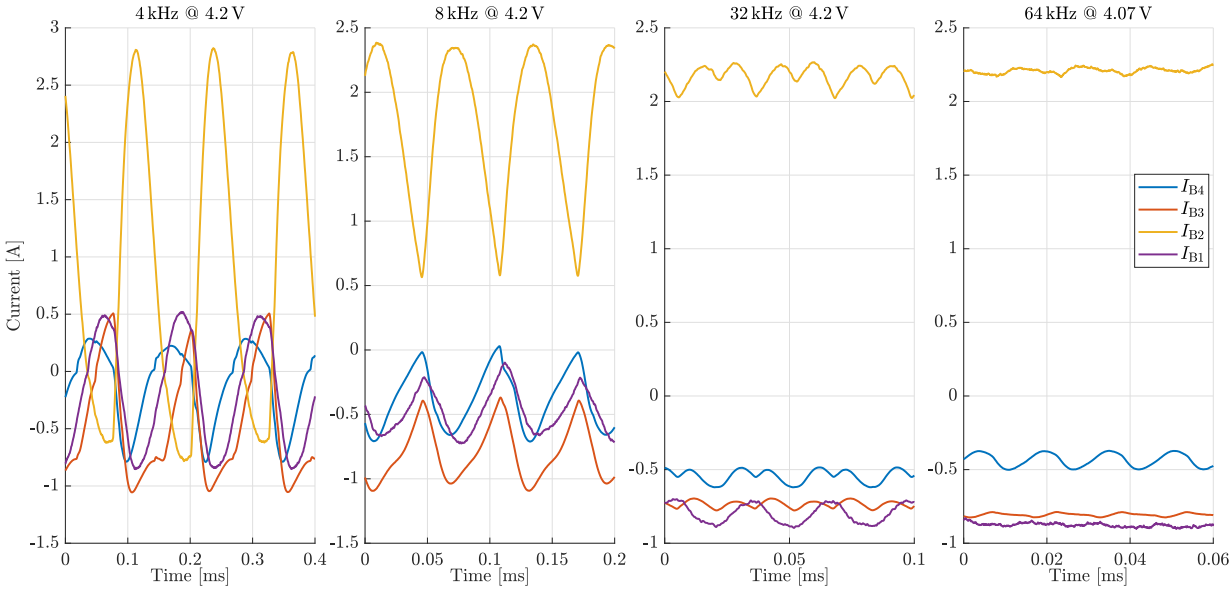

Figure 33: Battery balancing current waveforms of the four cells with the second cell voltage (V_2) set to 4.2 V, while the remaining cells are fixed at 3.3 V, across different switching frequencies.

Figure 35 presents the measured efficiency of the balancing chip as a function of switching frequency.

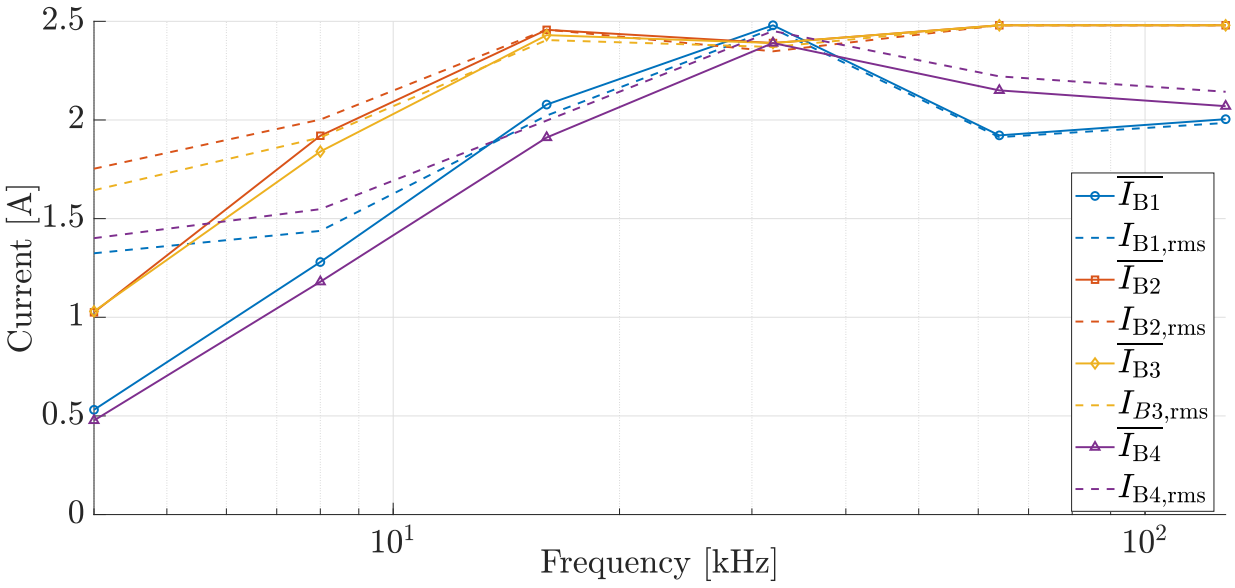

Figure 34: Effect of switching frequency on the average and RMS battery balancing currents of all cells for a fixed imbalance condition of the complementary capacitor balancer (shown in Fig. 7).

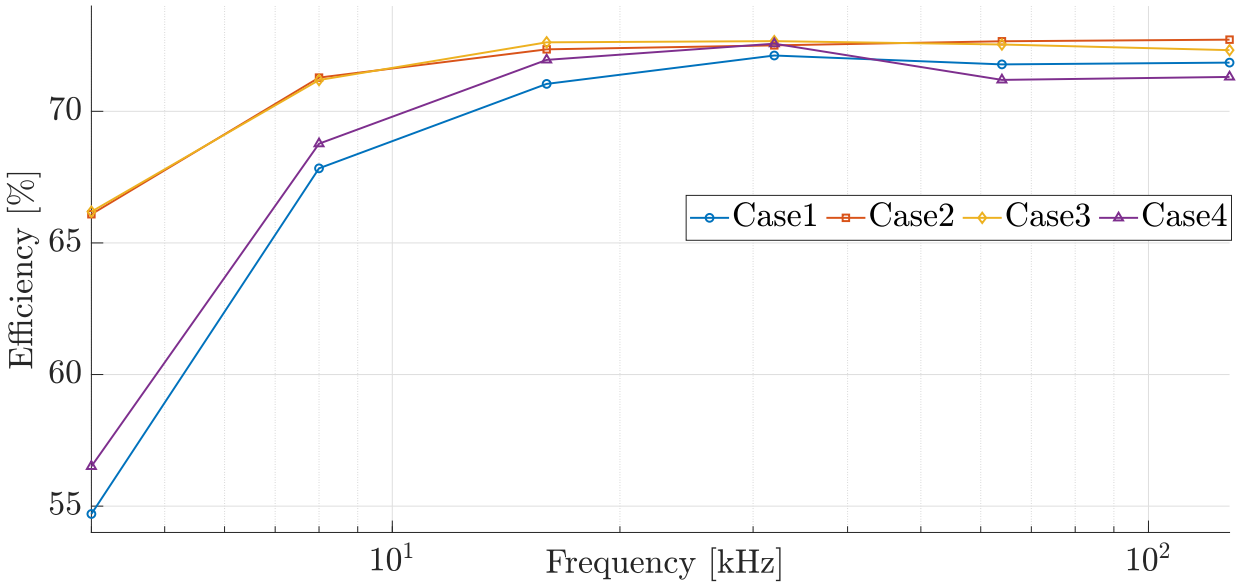

Figure 35: Efficiency variation with switching frequency across four imbalance conditions for the complementary capacitor balancer (shown in Fig. 7), where in each case one cell voltage is set to 4.3 V while the remaining cells are fixed at 3.3 V.

To characterise the efficiency, one cell supply is set to the maximum Li-ion voltage of 4.2 V, while the remaining cell supplies are fixed at 3.3 V to establish a defined voltage differential. The efficiency is calculated as the ratio of the output power, i.e., the power delivered to the lower-voltage cells, to the input power drawn from the higher-voltage cell.

The results show that efficiency increases with switching frequency and reaches its maximum for frequencies above approximately 30 kHz. At lower frequencies (below 10 kHz), the capacitive balancing paths exhibit higher impedance, which limits charge-transfer effectiveness and results in reduced efficiency.

Finally, to validate the circuit's capability of balancing various SOC difference scenarios, Keithley 2281S-20-6 devices were used to emulate Li-ion cells with capacities of 500 mAh. The results in Fig. 36 confirm the dual-IC balancer

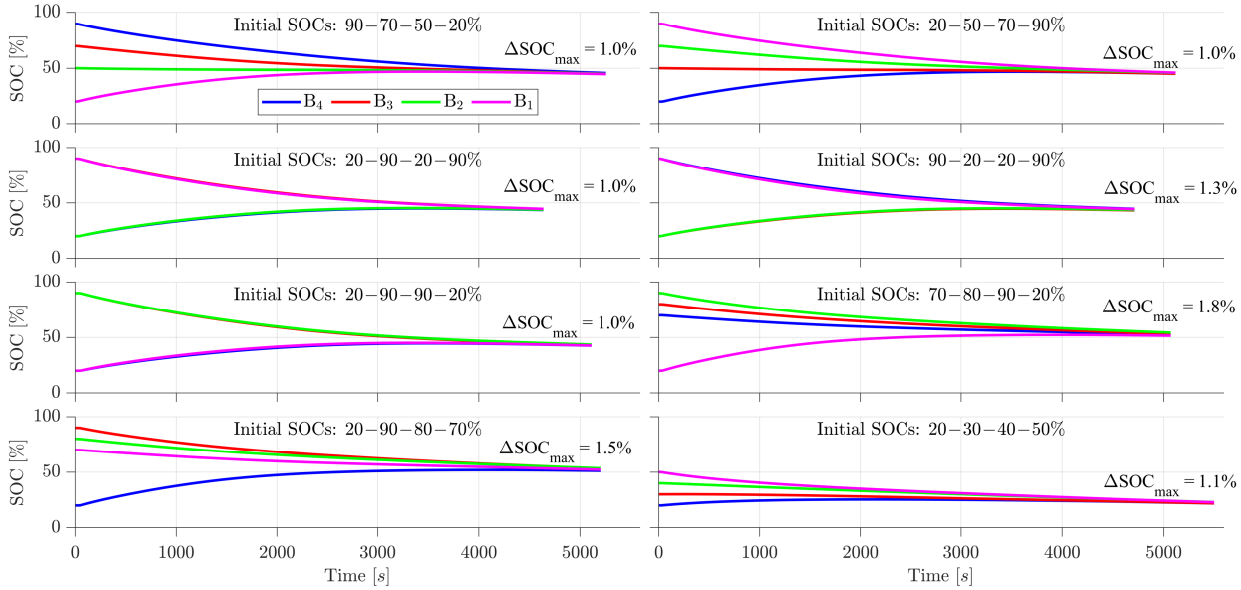

Figure 36: Balancing performance of the complementary capacitor balancer (shown in Fig. 7) across various initial battery SOC distributions at a switching frequency of 32 kHz for a cell capacity of 500 mAh, with balancing terminated when the maximum inter-cell SOC difference is reduced to 1.8–1%.

ability to achieve equalized SOCs to within 1-2%, demonstrating the balancer's high symmetry and higher cell-location dependency compared to the single IC balancer. These observations also agree with the pure discrete realizations of these balancers presented in [16, 34].

7 Comparison with State-of-the-Art Active Balancing Systems

Table 3 compares the proposed on-chip active cell balancer with representative state-of-the-art active battery blancing solutions. Most commercially available products listed in the table implement board-level active balancing architectures, which rely on discrete components and external power stages, resulting in larger form factors and limited scalability in cost-sensitive applications. Among the compared designs, only the MP2643 integrates balancing switches on-chip; however, it is constrained to low cell count and supports only adjacent cell-to-cell energy transfer, which makes balancing a large string of battery cells slow.

In contrast, the proposed design is a fully integrated IC-based active balancer, employing on-chip switching circuitry with external capacitors for energy transfer. The compact silicon area of 3.4 mm^2 enables high scalability, allowing multiple modules of the IC to be deployed across large battery strings while maintaining low system cost. Although the architecture is scalable to support up to eight cells on-chip, the prototype presented in this work is limited to four cells to reduce development complexity and validation cost. Furthermore, the active-mode current consumption can be reduced through design without impacting balancing performance, providing additional flexibility for low-power applications.

A key advantage of the proposed approach is its configurational flexibility, as the external energy transfer capacitors can be arranged in single-tier, multi-tier, mesh, delta, or other topologies to facilitate efficient charge redistribution. This adaptability, combined with full on-chip integration and compact silicon footprint, makes the proposed balancer well suited for scalable and energy-efficient battery management systems, particularly in applications requiring modular expansion and high integration density.

Finally, the balancing current capability of the proposed IC can be further increased by enlarging the width of the N-channel LDMOS switches. In the present prototype, the chip area was primarily constrained by cost considerations rather than fundamental performance limits. As a result, the design is inherently scalable: higher balancing currents can be achieved while preserving the same control and driving architecture. Moreover, the simple and low-cost internal driver rail generation facilitates straightforward extension of the design to support both higher current and higher voltage operation.

Table 3: Comparison with State-of-the-Art BMS Products with Active Balancers

Param.	TI/ADI ICs	JK 16S-15P	JK 16S-20P	Daly BMS	EK-C14S5A	MP2643	**Proposed**
Max. balancing current (A)	2–5	1	2	1	5.5	2	1.3–2.5
No. of cells	16	16	16	24	14	2	4
Single cell voltage (V)	1.8–3.8	1–5	1–5	3–3.7	2.7–4.2	2.4–4.35	2.4–4.3
Active mode current (mA)	10	19	19	50	7	2.97 W	18
Integration level	Hybrid	on-board	on-board	on-board	on-board	on-chip	on-chip

8 Conclusion

This paper has proposed an on-chip integration approach for battery balancing circuits based on stacked half-bridge converter submodules. This included comprehensive circuit analysis, system and circuit-level simulations, and silicon measurements.

The first part of the investigation validated the functionality of a single integrated circuit comprising four stacked half-bridge modules, demonstrating its feasibility as a compact and modular battery balancing solution. The architecture is extendable on-chip up to the voltage limit of the semiconductor process and capable of simultaneous energy transfer among all cells in the string.

The second part of the investigation examined the operation of two integrated circuits working in a complementary manner. This configuration increased the achievable average balancing current and efficiency, accelerated equalisation across a wide range of imbalance conditions, and reduced cell self-heating by maintaining an RMS current close to the average balancing current. The complementary operation further demonstrated the scalability of the proposed approach and its suitability for extending balancing capability beyond single-chip limitations.

Across both investigations, the proposed architecture is modular and stackable, requiring only simple open-loop PWM control signals and eliminating the need for voltage or current sensing. This significantly simplifies system implementation and facilitates direct integration with battery cells in applications with strict size and weight constraints. Compared to discrete balancing solutions, the integrated approach reduces system footprint by incorporating a large number of switches on-chip, simplifies gate driving, and removes the need for isolating transformers or optical drivers.

Performance analysis highlighted the importance of packaging and interconnect design. Optimised layout and packaging can minimise parasitic inductance and resistance associated with bonding wires and PCB traces, preserving the low on-resistance advantage of the integrated switches. This enables higher switching frequencies, faster balancing dynamics, and the use of smaller, lower-cost balancing capacitors. In addition, the low threshold voltage of the switches supports compatibility with a broad range of battery chemistries, allowing efficient operation over a cell-voltage range of approximately 2.4 V to 4.3 V.

Overall, the results demonstrate that integrated, modular battery balancing circuits can provide compact, scalable, and efficient cell equalisation both as stand-alone modules and when combined in complementary configurations.

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References

[1] W. Liu, T. Placke, and K. Chau, "Overview of batteries and battery management for electric vehicles," *Energy Reports*, vol. 8, pp. 4058–4084, 2022.

[2] M. Dubarry, N. Vuillaume, and B. Y. Liaw, "Origins and accommodation of cell variations in li-ion battery pack modeling," *International Journal of Energy Research*, vol. 34, no. 2, pp. 216–231, 2010.

[3] A. Turksoy, A. Teke, and A. Alkaya, "A comprehensive overview of the dc-dc converter-based battery charge balancing methods in electric vehicles," *Renewable and Sustainable Energy Reviews*, vol. 133, p. 110274, 2020.

[4] S. Karmakar, A. K. Bohre, and T. K. Bera, "Recent advancements in cell balancing techniques of bms for evs: A critical review," *IEEE Transactions on Industry Applications*, 2025.

[5] G. Zhu, X. Huang, Y. You, Y. Li, W. Guo, and Z. Zhu, "Multi-cell battery sensing and protection ic with integrated low-temperature-drift reference for series battery pack management," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2025.

[6] Z. Zhao, H. Hu, Z. He, H. H.-C. Iu, P. Davari, and F. Blaabjerg, "Power electronics-based safety enhancement technologies for lithium-ion batteries: An overview from battery management perspective," *IEEE Transactions on Power Electronics*, vol. 38, no. 7, pp. 8922–8955, 2023.

[7] A. Safari, H. Sorouri, A. Oshnoei, and F. Blaabjerg, "A state-of-the-art review on battery cell balancing strategies," *Discover Energy*, vol. 5, no. 1, pp. 1–42, 2025.

[8] C. Pascual and P. T. Krein, "Switched capacitor system for automatic series battery equalization," in *Proceedings of APEC 97-Applied Power Electronics Conference*, vol. 2, pp. 848–854, IEEE, 1997.

[9] A. C. Baughman and M. Ferdowsi, "Double-tiered switched-capacitor battery charge equalization technique," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 6, pp. 2277–2285, 2008.

[10] M. Daowd, M. Antoine, N. Omar, P. Van den Bossche, and J. Van Mierlo, "Single switched capacitor battery balancing system enhancements," *Energies*, vol. 6, no. 4, pp. 2149–2174, 2013.

[11] M.-Y. Kim, C.-H. Kim, J.-H. Kim, and G.-W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 3989–3999, 2013.

[12] Y. Ye and K. W. E. Cheng, "Modeling and analysis of series–parallel switched-capacitor voltage equalizer for battery/supercapacitor strings," *IEEE journal of emerging and selected topics in power electronics*, vol. 3, no. 4, pp. 977–983, 2015.

[13] Y. Ye, K. W. E. Cheng, Y. C. Fong, X. Xue, and J. Lin, "Topology, modeling, and design of switched-capacitor-based cell balancing systems and their balancing exploration," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4444–4454, 2016.

[14] Y. Shang, C. Zhang, N. Cui, and C. C. Mi, "A delta-structured switched-capacitor equalizer for series-connected battery strings," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 452–461, 2018.

[15] Y. Shang, N. Cui, and C. Zhang, "An optimized any-cell-to-any-cell equalizer based on coupled half-bridge converters for series-connected battery strings," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8831–8841, 2018.

[16] M. Z. Tazehkand and M. Baghdadi, "High-performance continuous-current capacitive battery balancer, with flexibility in battery cells connection and independent of cells location," *IEEE Transactions on Power Electronics*, 2025.

[17] Y. Izadi and R. Beiranvand, "A comprehensive review of battery and super-capacitor cells voltage-equalizer circuits," *IEEE Transactions on Power Electronics*, 2023.

[18] S. K. Dam and V. John, "A modular fast cell-to-cell battery voltage equalizer," *IEEE Transactions on Power Electronics*, vol. 35, no. 9, pp. 9443–9461, 2020.

[19] V. B. Vulligaddala, S. Vernekar, S. Singamla, R. K. Adusumalli, V. Ele, M. Brandl, and M. Srinivas, "A 7-cell, stackable, li-ion monitoring and active/passive balancing ic with in-built cell balancing switches for electric and hybrid vehicles," *IEEE Transactions on Industrial Informatics*, vol. 16, no. 5, pp. 3335–3344, 2019.

[20] T. Designs, "16-cell li-ion battery active balance reference design," *Texas Instrum., Dallas, TX, USA*, 2017.

[21] Y. Shang, N. Cui, B. Duan, and C. Zhang, "Analysis and optimization of star-structured switched-capacitor equalizers for series-connected battery strings," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9631–9646, 2017.

[22] B. Wicht, *Design of Power Management Integrated Circuits*. John Wiley & Sons, 2024.

[23] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. De Doncker, "Semiconductor power devices," *Physics, characteristics, reliability*, vol. 2, 2011.

[24] T. Erlbacher, *Lateral power transistors in integrated circuits*, vol. 59. Springer, 2014.

[25] W. Sun, R. Ye, S. Liu, J. Wei, W. Su, F. Lin, G. Sun, and Z. Lin, "Layout arrangement concern for lateral dmos with large geometric array used as output device," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 2, pp. 450–457, 2017.

[26] A. Hölke, D. K. Pal, Y. Hao, K. K. Yaw, E. Kho, G. Kittler, U. Kuniss, and J. Gessner, "A 200v partial soi 0.18 μm cmos technology," in *2010 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 257–260, IEEE, 2010.

[27] C. Rindfleisch and B. Wicht, "A resonant one-step 325 v to 3.3–10 v dc–dc converter with integrated power stage benefiting from high-voltage loss-reduction techniques," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3511–3520, 2021.

[28] D. Disney and Z. J. Shen, "Review of silicon power semiconductor technologies for power supply on chip and power supply in package applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4168–4181, 2013.

[29] F. Udrea, "Soi-based devices and technologies for high voltage ics," in *2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 74–81, IEEE, 2007.

[30] M. Rose and H. J. Bergveld, "Integration trends in monolithic power ics: Application and technology challenges," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 1965–1974, 2016.

[31] Q. Farhat and M. Baghdadi, "Multiple-output level shifters with dead-time control for gate driving in series-stacked voltage domains," *Authorea Preprints*, Feb. 2026. Preprint.

[32] Q. Farhat and M. Baghdadi, "On-chip design and implementation of a battery-cell-level binary-tree multilevel converter," *Authorea Preprints*, Oct. 2025. Preprint.

[33] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35 µm HV-CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 485–497, 2010.

[34] Y. Ye, J. Lin, Z. Li, and X. Wang, "Double-tiered cell balancing system with switched-capacitor and switched-inductor," *IEEE Access*, vol. 7, pp. 183356–183364, 2019.