A SCALABLE HYBRID MULTILEVEL POWER CONVERTER USING LOW-VOLTAGE ON-CHIP POWER MODULES

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ABSTRACT

This manuscript presents a hybrid architecture for scalable multilevel power conversion based on integrated binary-tree multilevel converter (BTMLC) modules and discrete switching stages. The proposed approach partitions voltage synthesis across two domains: high-frequency switching and level generation are implemented on-chip using low-voltage semiconductor devices, while higher-voltage stages are realised using discrete switches operating at lower switching frequencies. This strategy enables high-performance voltage synthesis from battery-cell voltage levels while extending the overall voltage capability beyond the limits of the semiconductor technology.

To enable this architecture, an integrated eight-battery-tap BTMLC module is designed and implemented to dynamically select individual cell voltages and synthesise high-resolution pseudo-sinusoidal waveforms or arbitrary voltage patterns. Novel circuit techniques are introduced to generate gate-driver supply rails for both high-side and low-side switches using low-cost low-voltage devices, with the required rail voltages derived directly from the battery stack. The complete module, including power stages, control logic, gate drivers, level shifters, and protection circuits, is fabricated in a 130-nm BCD process using LDMOS power devices.

Experimental results from a 20.52-mm^2 silicon prototype demonstrate reliable operation and efficient driving of multiple converter switches with low on-state resistance. The converter is packaged in a commercial J-leaded chip carrier for baseline validation and also integrated into custom PCB assemblies with manually wire-bonded chips to reduce conduction path resistance. The scalability of the proposed hybrid architecture is demonstrated by stacking two BTMLC modules and combining their outputs using an off-chip half-bridge stage. Measurements confirm variable-frequency and variable-magnitude waveform synthesis while delivering up to 6 A to a resistive load with a peak efficiency of 98.5%.

Keywords Multilevel converters · Integrated power ICs · Cell-level power conversion · Hybrid IC–discrete architecture · Electric vehicle power electronics · bond-on-active-circuit · BCD technology

1 Introduction

High-performance power converters are critical enablers for modern electrified transportation systems, including battery electric vehicles (BEVs), hybrid aircraft propulsion, and distributed energy platforms. In these applications, power converters regulate the flow of energy between batteries, traction motors, charging infrastructure, and auxiliary subsystems. Improvements in power electronics and battery technologies have thus significantly accelerated the adoption of electric mobility, where compactness, efficiency, and reliability remain primary design objectives [1].

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In battery-powered systems, space and mass constraints limit the amount of electrochemical storage that can be installed. Consequently, maximising the usable energy extracted from each battery cell becomes a defining factor for overall drivetrain performance. Recent research therefore explores converter architectures capable of operating directly from battery-cell voltages, enabling more efficient utilisation of stored energy and improved system integration [2].

Multilevel converters (MLCs) have emerged as a promising alternative to two-level inverters (Fig. 1(a.i)) to achieve these objectives. By synthesising the output voltage from multiple DC sources or capacitive partitions (Fig. 1(a.ii)), MLCs enable the use of low-voltage semiconductor devices while reducing voltage stress per switch, electromagnetic interference (EMI), and total harmonic distortion (THD) [3, 4]. Additional benefits include improved waveform quality, reduced switching losses, enhanced fault tolerance, and lower stress on machine insulation systems [5].

However, the practical implementation of multilevel converters becomes increasingly challenging as the number of voltage levels grows. Conventional multilevel topologies such as the flying-capacitor (FC) (Fig. 1(b.i)) [6], neutral-point-clamped (NPC) (Fig. 1(b.ii)) [7], self-balancing generalized topology (P2) (Fig. 1(b.iii)) [8], and cascaded bipolar switched cells (CBSC) (Fig. 1(b.iv)) [9] require a large number of power switches together with their associated gate drivers and auxiliary circuits [10]. As the number of voltage levels increases, the number of switches and gate-driving circuits grows rapidly, leading to increased system complexity, implementation cost, parasitic losses, and reduced scalability [11].

To improve the utilisation of battery cells and reduce DC-link voltage stress, several battery-integrated multilevel inverter (BIMI) and battery-integrated modular multilevel converter (BI-MMC) architectures have been proposed [12, 13, 14, 15]. In these systems, each battery cell or small cell group is interfaced with a dedicated power-conversion submodule, forming a cascaded converter structure that synthesises the overall output voltage. Representative implementations include battery modular multilevel management system (BM3), half-bridge and full-bridge modular submodules, as illustrated in Fig. 1(c.i–c.iv). While such approaches provide advantages in terms of modularity and improved waveform quality, they introduce significant control and gate-driving complexity due to the large number of floating switches and isolated voltage domains [16]. Furthermore, increasing the number of voltage levels leads to reduced efficiency, as the larger number of switches in the conduction path results in higher power losses compared to conventional two-level inverters [17].

One promising direction for addressing these challenges is monolithic integration of power stages and control circuitry. Monolithic integration can reduce parasitic inductances, simplify packaging, and enable compact implementations by integrating switches, gate drivers, and sensing circuits on a single chip [18]. GaN-based integrated converters have demonstrated high switching speeds and reduced losses, with several works reporting monolithic half-bridge or three-level converter implementations [19, 20]. However, large-scale integration of complex multilevel converter architectures remains difficult in GaN technologies due to limited device libraries, lack of complementary devices, and substrate coupling effects [21].

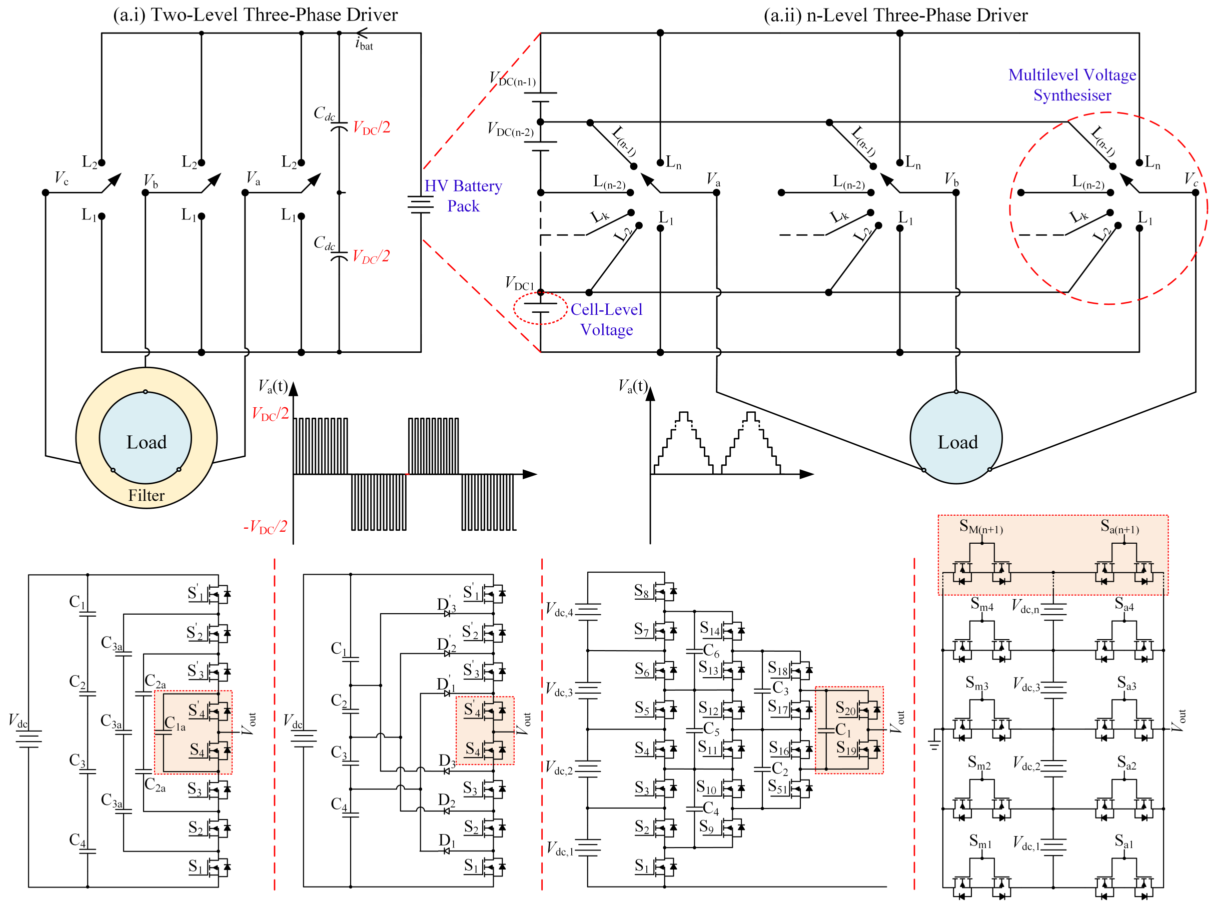
In contrast, BCD (Bipolar–CMOS–DMOS) technologies offer a mature and versatile platform for integrating low-voltage CMOS logic, analogue circuits, and lateral high-voltage power devices within a single fabrication process [22]. These technologies enable compact implementation of driver circuits, level shifters, and voltage regulators together with power switches, making them attractive for integrated power converters operating at battery-cell voltage levels [23, 24].

Despite these advances, most existing monolithic power integrated circuits (ICs) integrate only basic converter stages such as half-bridge or full-bridge structures. Large-scale multilevel conversion directly from battery cells has received comparatively little attention. Implementing such architectures entirely with discrete components is impractical due to the large number of switches, isolated gate drivers, and floating power supplies required.

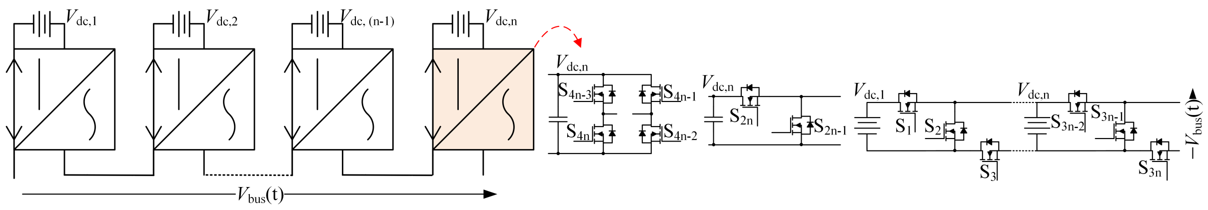
To address these limitations, this work proposes a hybrid IC–discrete architecture for high-voltage power conversion based on a binary-tree multilevel converter (BTMLC). The proposed concept performs high-frequency switching and voltage synthesis using integrated low-voltage devices on chip, while higher-voltage stages are implemented using discrete components operating at lower switching frequencies. This voltage–frequency allocation allows the converter to exploit the superior switching performance of lateral on-chip devices while maintaining scalability to higher voltage levels.

The BTMLC architecture enables power processing directly from battery-cell voltages using low-voltage switches, thereby facilitating distributed energy processing and improved battery utilisation [23]. In addition, the battery cells themselves can be used to supply integrated gate-driver circuits through on-chip regulators, eliminating the need for isolated DC–DC supplies and reducing system complexity.

The proposed approach therefore combines the advantages of monolithic integration and modular converter architectures, enabling scalable high-voltage synthesis while maintaining compact implementation and high efficiency. Although the circuit-level techniques presented in this work are demonstrated using the BTMLC topology, the underlying hybrid



(b.i) FCML converter (b.ii) NPC converter (b.iii) P2 converter (b.iv) CBSC



(c.i) MMC (c.ii) Full bridge (c.iii) Half bridge (c.iv) BM3

Figure 1: Overview of MLC architectures

integration methodology may also be applied to other multilevel converter architectures intended for battery-cell-level power processing.

This manuscript advances the state-of-the-art of multilevel power converters by

- Proposing a hybrid IC–discrete architecture for high-voltage synthesis that combines high-frequency lateral on-chip devices with higher-voltage vertical off-chip devices. This approach enables high–power-density multilevel converters operating directly from battery-cell voltages while supporting unified power-processing functions including motor driving, charging, and cell balancing.
- Demonstrating the stacking capability of the BTMLC converter IC to synthesise 50 V half-sine waveforms under variable-voltage and variable-frequency operation. Experimental measurements include on-state resistance, conversion efficiency, heat distribution, and thermal resistance.
- Developing a new implementation of the BTMLC architecture incorporating compact driver-rail supply generators and integrated control circuits that utilise the available battery-cell voltage sources.

- Designing and implementing laterally diffused MOS (LDMOS) power switches with low on-state resistance, providing at least 6 A continuous current capability.
- Demonstrating reliable wire bonding of bond-on-active-circuit (BOAC) pad structures in low-dielectric-constant (k) silicon technology, improving area efficiency, reducing metallisation resistance, and lowering fabrication cost.

2 Review of Hybrid Architectures and the Extension of Voltage Levels in Multilevel Converters

MLC topologies can be systematically derived and extended using structured composition principles. In [25], a general derivation framework is presented in which converter structures are generated from basic switching cells using horizontal and vertical topology conformation rules. In the horizontal conformation approach, switching cells are classified as a base cell and module cells. The base cell appears once in the topology, whereas module cells can be cascaded horizontally to increase the number of voltage levels. This enables the synthesis of several well-known converter families such as the active NPC, nested NPC, and stacked multicell converters, by repeatedly connecting module cells to the output node of the preceding stage.

An alternative approach is vertical conformation, where identical converter modules are stacked and interfaced with a voltage-selection or unfolding stage that typically operates at the fundamental output frequency. In this configuration, additional voltage levels are generated by stacking more modules or by increasing the internal level count of the module itself. Such vertically stacked architectures form the basis of many modular multilevel converters used in medium-voltage applications, such as stacked FC and NPC converters [25].

Another widely used technique for increasing the number of voltage levels is the cascading of H-bridge building blocks with an existing converter stage. While this method can effectively extend the output voltage resolution, it often introduces non-uniform voltage ratings among devices and capacitors, which reduces modularity and complicates practical implementation when many cascaded stages are employed [25].

Beyond these topology derivation approaches, recent work has explored hierarchical structures for achieving high numbers of voltage levels with reduced device count. In [10], a generalized derivation method is proposed for tree-type active NPC converters. In this method, multilevel topologies are constructed from hierarchical combinations of two-level bridge cells and three-level neutral-point-piloted cells. The resulting structure resembles a tree network in which each stage increases the number of accessible dc-link nodes and therefore the achievable voltage levels. Using this approach, an $(n + 1)$-level converter can be realised using only $2n$ active switches without requiring flying capacitors, while maintaining a single current path for each switching state. Although such tree-based structures reduce passive components and device count, they are still typically implemented using discrete switching networks and therefore face practical challenges when large numbers of floating switches and gate drivers are required.

The evolution of MLCs has also led to the emergence of hybrid converter architectures that combine multiple circuit concepts to improve performance. As discussed in [26], modern MLC research increasingly explores hybrid configurations that merge features from conventional topologies such as NPC, FC, cascaded H-bridge, and modular multilevel converters. These hybrid structures aim to optimise trade-offs between device count, passive component requirements, voltage stress distribution, and power density. In some implementations, hybrid architectures combine different semiconductor technologies, where wide-bandgap devices operate at high switching frequencies while silicon-based devices operate at lower frequencies to achieve an improved distribution of switching and conduction losses.

Hybrid device utilisation has also been investigated in practical converter implementations. For example, hybrid Si–SiC multilevel converters allocate switching tasks according to device capabilities, where SiC MOSFETs operate at high switching frequencies while silicon IGBTs perform low-frequency switching functions [27]. Such partitioning allows the converter to exploit the fast switching characteristics of wide-bandgap devices while retaining the high-current capability of silicon devices.

More generally, recent work has attempted to formalise the synthesis of multilevel converters using unified topological building blocks. In [28], multilevel converters are decomposed into two fundamental functional units: level generators (LGs), which produce discrete voltage levels from dc sources, and level selectors (LSs), which connect these levels to the output according to the desired switching state. This abstraction provides a unified framework for analysing and deriving multilevel converter topologies across voltage-source, current-source, and matrix converter families.

Another related concept is the internal parallel converter architecture proposed in [29], where each converter phase consists of a low-switching-frequency stage combined with multiple parallel high-switching-frequency modules. This structure enables hybrid device utilisation and modular operation while reducing current stress in high-frequency devices. Interleaving the parallel modules further increases the effective number of output voltage levels without significantly increasing control complexity.

While these approaches provide systematic methods for extending voltage levels and improving converter performance, most of them assume fully discrete implementations. Consequently, the integration challenges associated with large numbers of floating switches, gate drivers, and isolated supplies remain largely unaddressed when converters operate directly from battery-cell voltage levels.

The architecture proposed in this work builds upon these concepts by combining modular voltage synthesis with a hybrid integration strategy. In the proposed approach, high-frequency switching and voltage synthesis are implemented using integrated low-voltage devices on chip, while higher-voltage stages are realised using discrete components operating at lower switching frequencies. This hybrid IC–discrete partitioning enables scalable high-voltage operation while preserving the compactness, performance, and integration advantages of monolithic power electronics.

Motivated by these observations, this paper proposes a hybrid converter architecture based on an integrated binary-tree multilevel converter module that operates directly from battery-cell voltage levels. The on-chip BTMLC module performs high-frequency voltage synthesis and level selection using integrated lateral semiconductor devices and associated control circuitry, forming a compact building block that can be replicated and stacked. To extend the overall voltage capability beyond the limits of the semiconductor technology, discrete switching stages are employed at the system level to multiplex the outputs of multiple BTMLC modules. By allocating high-frequency switching to the integrated modules and reserving higher-voltage operation for lower-frequency discrete stages, the proposed architecture enables scalable multilevel conversion while maintaining high power density, reduced parasitic effects, and improved integration capability. The operating principle and implementation of the proposed architecture are described in the following section.

3 Proposed Hybrid IC–Discrete Architecture for High-Voltage Power Conversion Using Battery-Cell-Level Modules

The proposed converter architecture extends the BTMLC concept proposed in [23] to higher-voltage operation by combining integrated-circuit (IC) modules with discrete power devices. The key idea is to partition voltage and switching-frequency stresses across two domains: a high-frequency, low-voltage IC domain and a lower-frequency, higher-voltage discrete domain. This heterogeneous arrangement aims to enable efficient high-voltage power conversion while retaining the advantages of highly integrated low-voltage circuitry.

Figure 2 illustrates the overall concept. The high-voltage DC link is decomposed into multiple low-voltage segments corresponding to individual battery cells. Each segment is processed by an on-chip BTMLC module that performs high-frequency switching using lateral low-voltage devices optimised for fast operation and low switching losses. The outputs of these IC modules are then combined using discrete off-chip devices that operate at higher voltage but significantly lower switching frequency.

This allocation of voltage and frequency stresses allows each device class to be used in its optimal operating region. On-chip switches operate at high frequency with relatively small voltage stress, enabling efficient waveform synthesis and compact integration. In contrast, the discrete off-chip switches are responsible for extending the overall voltage capability of the system. Since these devices switch at much lower frequencies, their switching losses remain negligible, allowing them to be optimised primarily for low conduction losses and high current capability.

The voltage capability of a single BTMLC module is ultimately limited by the breakdown voltage of the chosen semiconductor technology. In the present implementation, this limit constrains the design to an eight-tap configuration. Higher system voltages can therefore be achieved either by adopting technologies with greater breakdown capability (e.g., silicon-on-insulator (SOI)-based processes) or by stacking multiple BTMLC modules at the board level.

A simplified version of this expansion is illustrated in Fig. 3, where two tap-of-eight (TO8) IC modules are combined to realise a sixteen-tap converter. The additional discrete switching stage synthesises the final output waveform and enables operation beyond the voltage limits of a single chip. This stacking principle provides a scalable pathway for constructing higher-voltage and higher-power systems while maintaining compatibility with mainstream low-voltage IC technologies.

The feasibility of this approach is experimentally validated by interconnecting two BTMLC modules and an external half-bridge stage, demonstrating operation beyond the voltage limit of a single integrated module.

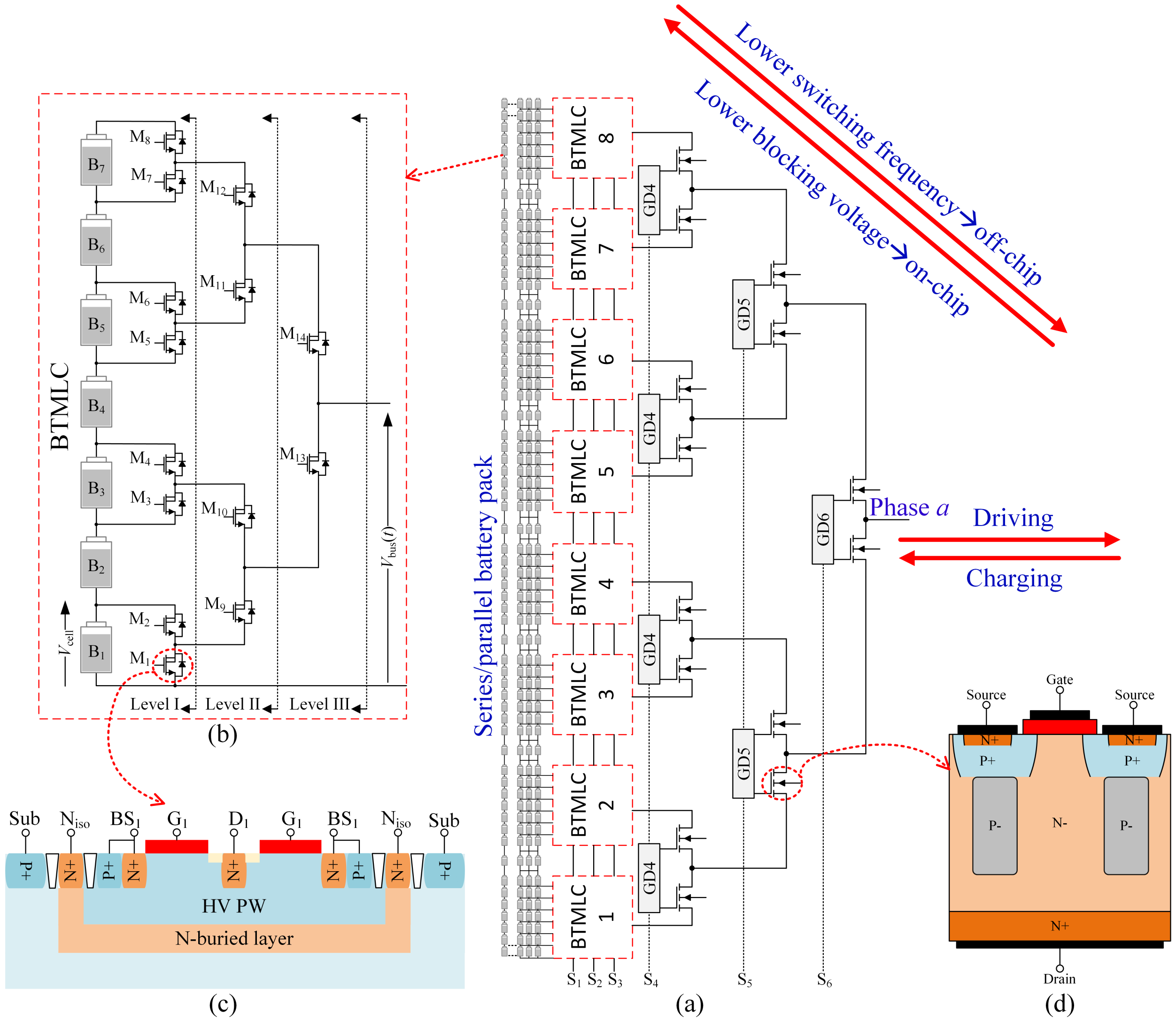


Figure 2: (a) Proposed hybrid multilevel converter combining IC-domain and discrete-domain modules; (b) on-chip battery-cell-level binary-tree multilevel converter (BTMLC); (c) lateral low-voltage high-performance on-chip isolated devices; (d) vertical off-chip devices for higher-voltage and lower-frequency operation.

4 Binary-Tree Multilevel Converter as a Scalable IC Building Block

The integrated building block used in this work is the binary-tree multilevel converter (BTMLC), originally introduced in [23]. The architecture is shown conceptually in Fig. 2(b). It interfaces of a set of series-connected battery inputs, denoted B_1–B_7, each providing a voltage equal to the cell voltage V_{cell}.

The converter is organised hierarchically into multiple switching levels. In the eight-tap implementation considered here, three levels of switching stages are used (Level I–III). Each level consists of complementary switch pairs arranged as half-bridge or chopper cells. The stages are driven by shared complementary control signals and are designed with identical device voltage ratings within each level.

The topology follows a binary-tree structure in which the number of available output voltage levels grows exponentially with the number of switching stages. For a converter with k hierarchical levels, the number of positive voltage taps is given by

$$n = 2^k, \qquad k \in \mathbb{Z}_{\geq 1}. \tag{1}$$

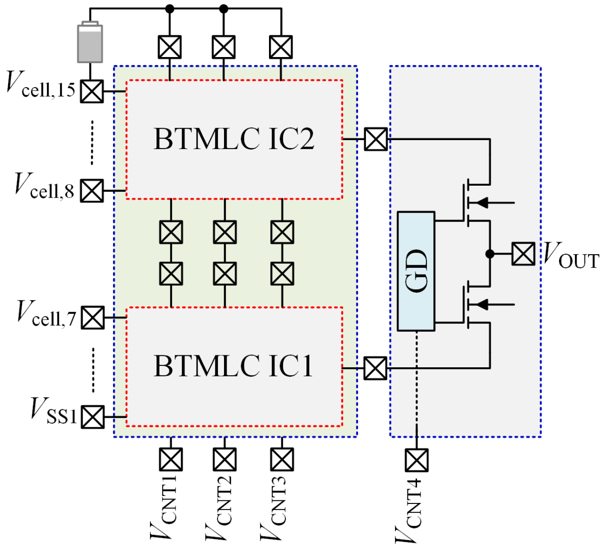


Figure 3: Converter expansion for higher voltage operation using tap-of-eight (TO8) IC modules, demonstrating the extension to sixteen voltage taps.

In the prototype presented in this work, $k = 3$, resulting in eight discrete voltage levels between 0 and $7V_{\text{cell}}$. The number of switches required for the level-generation network scales as

$$N_{\text{sw}} = 2n - 2. \tag{2}$$

A key property of the BTMLC is the systematic scaling of voltage stress and switching frequency across the different levels. The voltage blocking requirement for switches in level j is

$$V_{\text{blk},j} = V_{\text{cell}} 2^{j-1}, \qquad j = 1, \ldots, \log_2(n), \tag{3}$$

while the switching frequency decreases proportionally with the level index according to

$$f_{\text{sw},j} \propto \frac{1}{2^{j-1}}. \tag{4}$$

Consequently, the lowest-voltage switches operate at the highest switching frequency, whereas devices exposed to higher voltage stresses switch at proportionally lower frequencies. This intrinsic allocation of voltage and frequency enables an efficient implementation using integrated low-voltage devices for the high-frequency stages and discrete high-voltage devices for the lower-frequency stages.

When the converter is used to synthesise AC waveforms, a polarity-generation stage (typically implemented using an H-bridge) can be added to produce a bipolar output waveform. This stage operates at the output fundamental frequency and therefore imposes minimal switching losses.

From a power-loss perspective, the BTMLC exhibits two primary loss components: conduction losses due to the on-state resistance of the conducting switches and dynamic losses associated with the charging and discharging of device capacitances. Because the switching frequency decreases exponentially with the level index, higher-voltage devices operate at significantly lower switching frequencies, which naturally limits their dynamic losses.

This hierarchical voltage–frequency scaling forms the basis of the hybrid architecture explored in this work, where high-frequency switching stages are implemented on chip using low-voltage devices, while higher-voltage stages can be realised using discrete components operating at lower switching frequencies. Detailed analytical loss modelling and switch-sizing procedures are presented in [23].

For a converter with $\log_2(n)$ levels, the instantaneous conduction losses can be approximated as

$$p_{\text{cond}}(t) = i^2(t) \sum_{j=1}^{\log_2 n} R_{\text{on},j}. \tag{5}$$

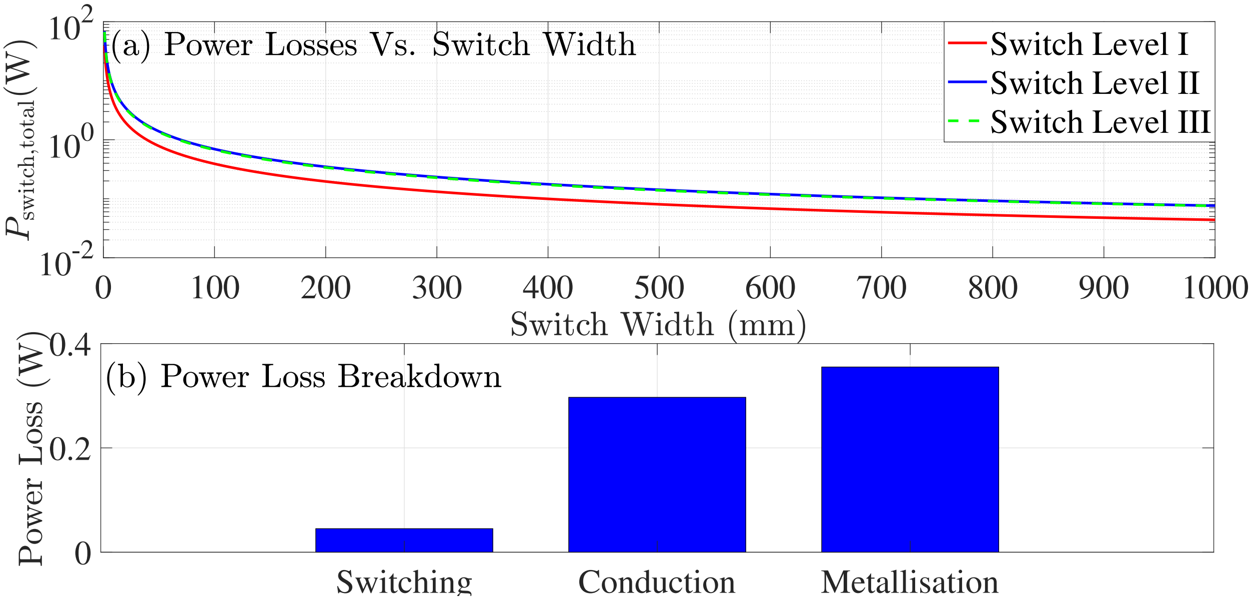


Figure 4: (a) Total power loss per switch versus switch width for Level I–III at $I_{\text{rms}} = 5$ A and $f_{\text{out}} = 10$ kHz. (b) Loss distribution under the same operating conditions.

Using the analytical model in [23], the switch power losses for the three levels of the proposed 8-level BTMLC were evaluated under operating conditions of 5 A rms current and 10 kHz output frequency. In this implementation, the switches were rated at 5 V, 10 V, and 16 V for Level I, Level II, and Level III, respectively. The total estimated loss is approximately 0.7 W.

The loss distribution indicates that switching losses are relatively small (6.5%), whereas conduction losses dominate, consisting of channel resistance losses (42.6%) and metallisation resistance losses (50.9%). The metallisation contribution slightly exceeds the intrinsic channel resistance of the devices.

For a 16-tap configuration realised by stacking two BTMLC modules, the proportion of on-chip switching losses increases to approximately 21.7% under the same operating conditions, although conduction losses remain the dominant component.

5 Circuit Implementations

The complete circuit implementation of the proposed BTMLC is presented in Fig. 5. The design incorporates both the power stages and the control stages of the converter. The power stage is realised using NDMOS switches rated at 5 V, 10 V, and 16 V for Level I, Level II, and Level III, respectively. The control stage performs signal level shifting, dead-time generation, and gate driving. Furthermore, the driver supply rails are derived internally with minimal overhead, eliminating the need for auxiliary dc–dc converters or bulky regulators. This functionality is achieved by utilising low-cost technology devices in conjunction with the readily available series-connected battery cells.

The maximum voltage rating of the converter is constrained by the junction breakdown voltage between the substrate and the isolation layer in Fig. 2(c). For reliable operation, the device bodies are tied to their respective sources, while for the NDMOS device the isolation layer taps are biased to the potential of one battery cell above the drain and source terminals.

5.1 Voltage level-shifters

The voltage level-shifters are required to convert the control signals from the logic domain to the voltage domains of each low-side and high-side switches. Two types of voltage level shifters are used, static-V_{SSH} level shifters that utilise battery cells for level shifting and floating V_{SSH} cross-coupled level shifters.

To up-shift the control signal to the low-side switches, a stack of series-connected switches whose gates are tied to the cell-voltage taps has been used. Three identical circuits are used for the three levels and they are controlled by inputs V_{CNT1}, V_{CNT2}, and V_{CNT3}. The principle of operation of this level shifter is explained in detail in [24].

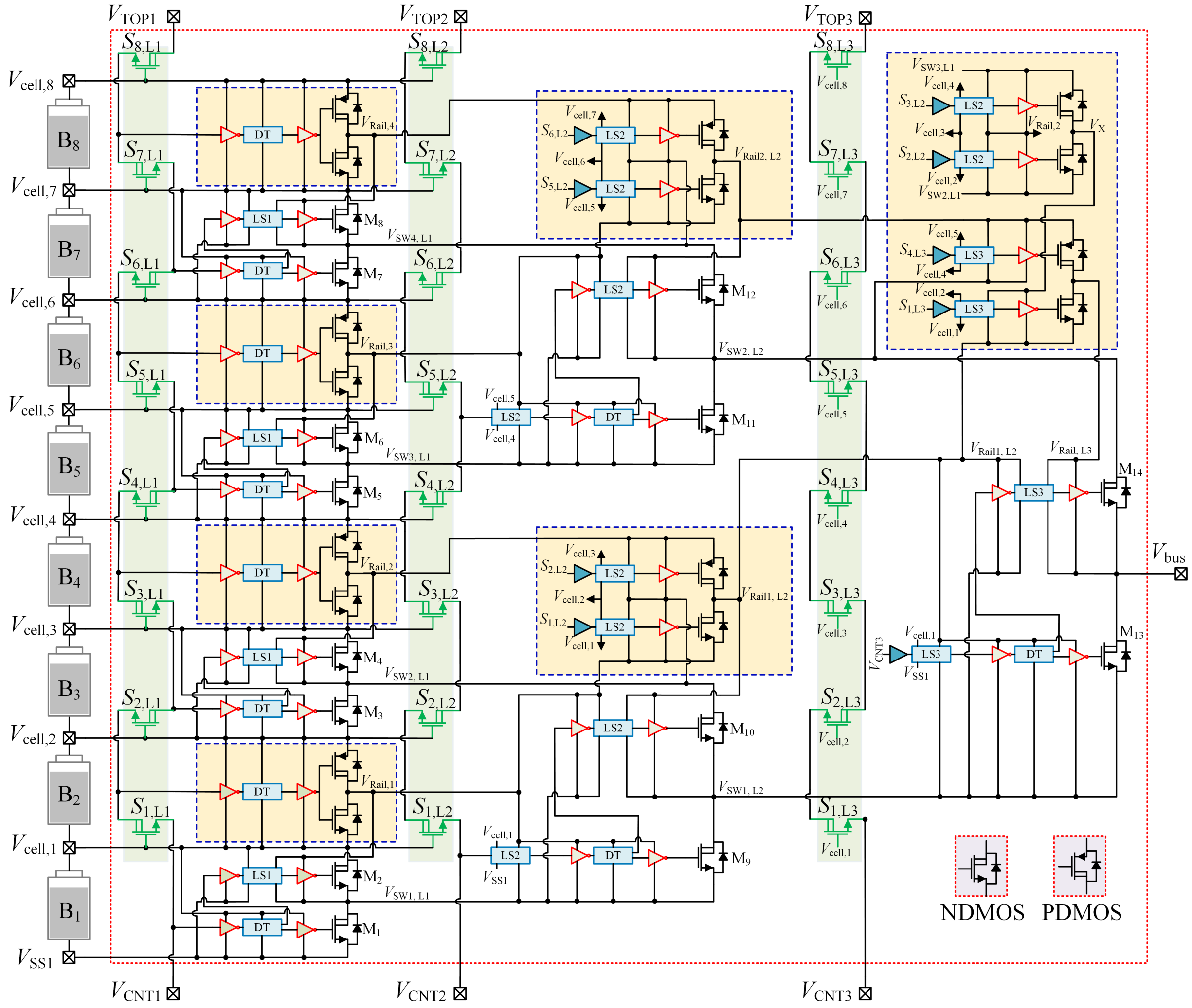


Figure 5: Proposed circuit design of the eight-tap BTMLC, with 'LS1', 'LS2', and 'LS3' denoting cross-coupled level-shifter circuits and 'DT' denoting dead-time generator blocks. Dimensions= 200–400 mm.

The output signals of the stacked level-shifter circuits are subsequently used to control the operation of the half-bridge submodules that directly connect with the battery cells, e.g., $V_{\text{cell},1}$, $V_{\text{cell},2}$, ...$V_{\text{cell},7}$. The floating level shifter circuits ("LS1/LS2/LS3" blocks) have been used for translating the signals translated by the stacked level shifter to the high-side switches in Level I and to both high-side and low-side switches in Levels II and III. This is required since the sources of these switches (in Levels II and III) are not fixed and can vary based on the state of each control signal. Therefore, these circuits have been implemented using a cross-coupled level shifter with non-static V_{SSH} capability, as shown in Fig. 6(a). For correct DC operation, the aspect ratios of the PDMOS and NDMOS devices to the PMOS pull-up devices have been sized according to the design methodology proposed in [30]. The dead-time generation circuit ("DT" block) is shown in Fig. 6(b). It receives the level-shifted input signal and generates a two-phase waveform with a dead-time period determined by the introduced delay. This delay is implemented using RC sections placed between the NAND gates and the buffer stages (omitted from Fig. 6(b)).

5.2 Level I Circuit Implementation

The Level I circuit of the converter comprises four half-bridge power stages, implemented using 5 V NDMOS devices connected across four battery cells.

Each half-bridge control stage integrates several key functions: CMOS inverters as gate drivers, a dead-time generator, a cross-coupled level shifter, and a high-side driver-rail supply circuit.

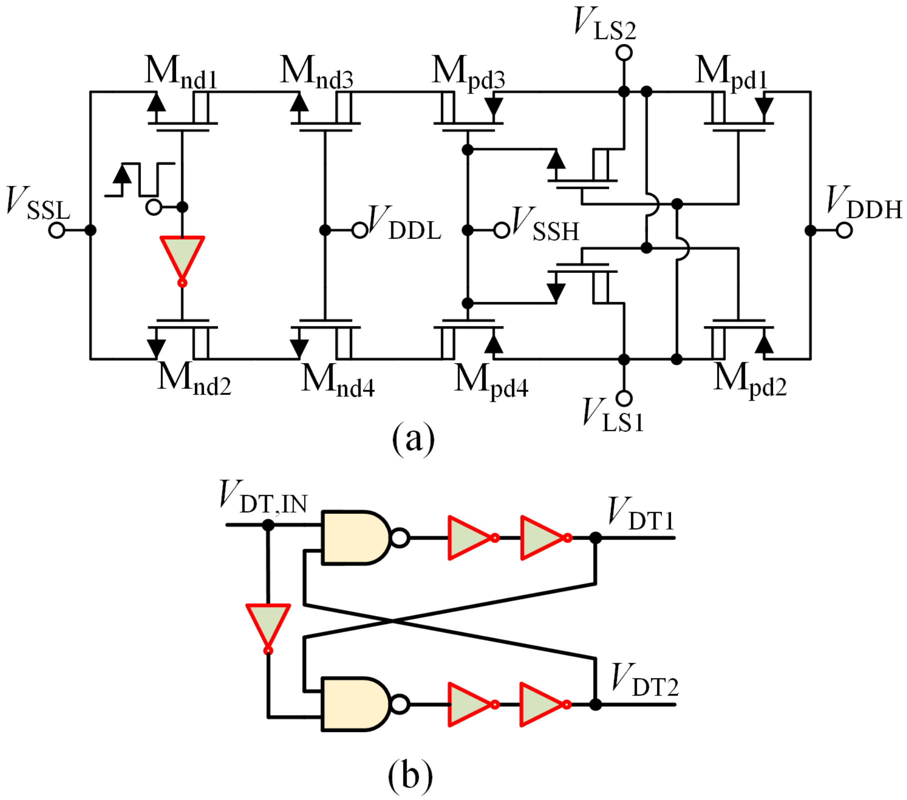


Figure 6: (a) Cross-coupled, non-static V_{SSH} level-shifter circuit. (b) NAND-based two-phase non-overlapping clock (dead-time) generator circuit.

As mentioned earlier, the control signal V_{CNT1} is level-shifted through stacked NDMOS switches, and the resulting signals are applied to the two-phase dead-time generation circuit, ensuring non-overlapping gate signals for both the low-side and high-side switches.

The high-side control signal is further level-shifted by the cross-coupled circuit, with V_{SSH} tied to the output switching node of each half-bridge submodule ($V_{SW1,L1}$—$V_{SW4,L1}$). The high-side level shifters are supplied by V_{DDH}, connected to $V_{Rail,1}$–$V_{Rail,4}$, which are derived from the upper battery cells of each submodule.

The driver-rail supply is realised using a compact push–pull circuit whose control logic mirrors that of the low-side power switch. When the high-side device is turned on, its gate is driven through the CMOS inverter to $V_{Rail,1}$ (in the bottom-most submodule), which is connected to $V_{cell,2}$ through the push-up PDMOS device. Conversely, when the low-side switch is on and the high-side switch is off, $V_{Rail,1}$ is pulled down to $V_{cell,1}$, as illustrated in Fig. 7. As a result, the gate–source voltage of the high-side device is maintained at one-cell voltage, while the voltage stress across the driver circuit and pull-up level-shifter devices is also limited to a single cell, ensuring reliable operation in both states. Given a threshold voltage of 0.9–1.3 V, a cell voltage above 2.5 V is sufficient for efficient switching.

5.3 Level II Circuit Implementation

The second-level switches, M_9–M_{12}, are implemented using 10 V NDMOS devices. The control architecture of each half-bridge in this level is similar to that of Level I, with the addition of a cross-coupled level shifter (“LS2” block) at the input. The control signal V_{CNT2} is level-shifted using a stacked level-shifter circuit in conjunction with cross-coupled level shifters to the appropriate nodes: $V_{SW1,L1}$ and $V_{SW1,L2}$ for the bottom half-bridge, and $V_{SW3,L1}$ and $V_{SW2,L2}$ for the top half-bridge.

In addition to the power-stage control circuits, the driver-rail supply generators, with outputs $V_{Rail1,L2}$ and $V_{Rail2,L2}$, are also driven by the level-shifted versions of V_{CNT2}.

Since M_9 shares its source with M_2, and M_{11} with M_6, the low-side devices M_9 and M_{11} in Level II derive their driver-rail voltages from $V_{\mathrm{Rail},1}$ and $V_{\mathrm{Rail},3}$, respectively, which are generated in the Level I circuit. For instance, when M_9 is turned on, $V_{\mathrm{SW1,L1}}$ toggles between $V_{\mathrm{cell},1}$ and V_{SS1}, depending on the states of M_1 and M_2, and $V_{\mathrm{Rail},1}$ is used to drive M_9. A similar condition applies to M_{11}, which is driven from $V_{\mathrm{Rail},3}$.

In contrast, the high-side devices M_{10} and M_{12} in Level II require dedicated push–pull stages rated similar to power-stage voltage. These push–pull circuits generate $V_{\mathrm{Rail1,L2}}$ for the gate driver of M_{10} and $V_{\mathrm{Rail2,L2}}$ for that of M_{12}.

Specifically, for M_{10}, $V_{\mathrm{Rail},2}$ is connected to $V_{\mathrm{Rail1,L2}}$ when the device is on, and $V_{\mathrm{Rail},1}$ is connected when it is off, as illustrated in Fig. 7.

An analogous mechanism applies in the upper half-bridge, where $V_{\mathrm{Rail2,L2}}$ is switched between $V_{\mathrm{Rail},4}$ and $V_{\mathrm{Rail},3}$ to power the gate driver of M_{12}.
These driver-rail generation circuits ensure that only a single-cell voltage is applied across the high-side gate drivers under all operating conditions, thereby enabling the reliable use of low-voltage switches.

5.4 Level III Circuit Implementation

The Level III power stage, consisting of switches M_{13} and M_{14}, is implemented using 16 V NDMOS devices. The control circuit architecture follows a structure similar to that of Level II, incorporating multi-stacked and floating level-shifters, a dead-time generator, and CMOS inverter gate drivers. The control signal V_{CNT3} is used to control this stage and is also level-shifted to provide appropriate signals to the control circuitry responsible for generating the driver-rail supply voltage ($V_{\mathrm{Rail,\,L3}}$) for the high-side switch M_{14}.

The gate driver of the low-side switch M_{13} is powered by the push-pull stage output from Level II, specifically $V_{\mathrm{Rail1,L2}}$, analogous to the operation of the low-side switch in Level II.

The generation of the high-side gate drive voltage in this stage is more complex and requires dedicated push-pull stages capable of selecting the appropriate cell voltage based on the state of the high-side switch. These small switches generate the driver-rail supply voltage $V_{\mathrm{Rail,\,L3}}$ and must withstand four cell voltages, equivalent to the voltage blocking capability of the Level III power switches. Controlled by signals $S_{1,\mathrm{L3}}$ and $S_{4,\mathrm{L3}}$, which follow the logic of the Level III control signal V_{CNT3} but operate in the $V_{\mathrm{cell},1}$-$V_{\mathrm{cell},2}$ and $V_{\mathrm{cell},4}$-$V_{\mathrm{cell},5}$ voltage domains, these switches select between $V_{\mathrm{Rail2,L2}}$ and $V_{\mathrm{Rail1,L2}}$ for output to $V_{\mathrm{Rail,L3}}$, as demonstrated in Fig. 7. When M_{14} is turned on, $V_{\mathrm{Rail,L3}}$ is connected to $V_{\mathrm{Rail2,L2}}$; when it is off, $V_{\mathrm{Rail1,L2}}$ is selected. This ensures that $V_{\mathrm{Rail,L3}}$ is consistently one cell voltage higher than $V_{\mathrm{bus}}(t)$, thereby enabling proper turn-on of the high-side switch.

The gate driver for the low-side switch within the Level III high-side switch driver-rail generator is powered by an output voltage denoted V_{X}. This voltage is derived from another auxiliary push-pull circuit, controlled by the Level II level-shifted signals $S_{2,\mathrm{L2}}$ and $S_{3,\mathrm{L2}}$. This circuit toggles V_{X} between $V_{\mathrm{SW2,L1}}$ and $V_{\mathrm{SW3,L1}}$, thereby maintaining a consistent single-cell voltage across the gate driver of the Level III driver-rail supply generator.

Overall, the proposed circuit techniques offer a low-cost solution for driving the switches in the BTMLC architecture. They avoid the use of special devices such as high-voltage resistors, Zener diodes, or other costly components that require large layout area and are less portable across technology platforms. As a result, the BTMLC design is more easily adaptable to a wide range of technologies.

6 Simulation Results

The proposed BTMLC circuit design was simulated using Cadence Virtuoso (Spectre) including post-layout parasitic extraction to verify its functional performance under NLC.

The NLC strategy generates switching commands by comparing a reference waveform to the discrete voltage levels of the stacked input cells. As shown in Fig. 8, a sinusoidal reference with a DC offset equal to its amplitude is applied. This ensures the reference remains within the available positive voltage range of the eight-tap BTMLC. The reference is continuously compared against the discrete cell-level voltages, producing the control signals illustrated in Fig. 9. These signals drive the switches in Levels I–III of the converter and are translated to their respective floating domains using the stacked level shifter described in the circuit design section.

The gate–source voltages of representative switches from Levels I–III are shown in Fig. 10. The waveforms confirm that the driver-rail generation circuits provide sufficient and stable gate overdrive across all voltage domains. The corresponding drain–source voltages are presented in Fig. 11, demonstrating correct turn-on and turn-off behaviour.

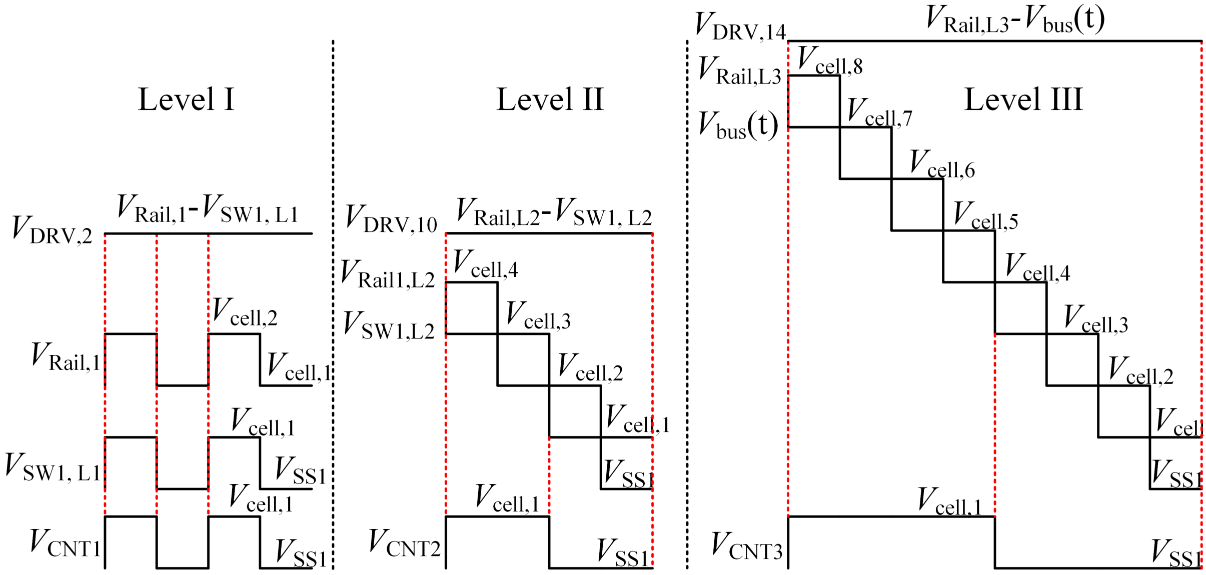


Figure 7: Illustration of the synthesis of the driver-rail supply voltages for switches in Levels I-III.

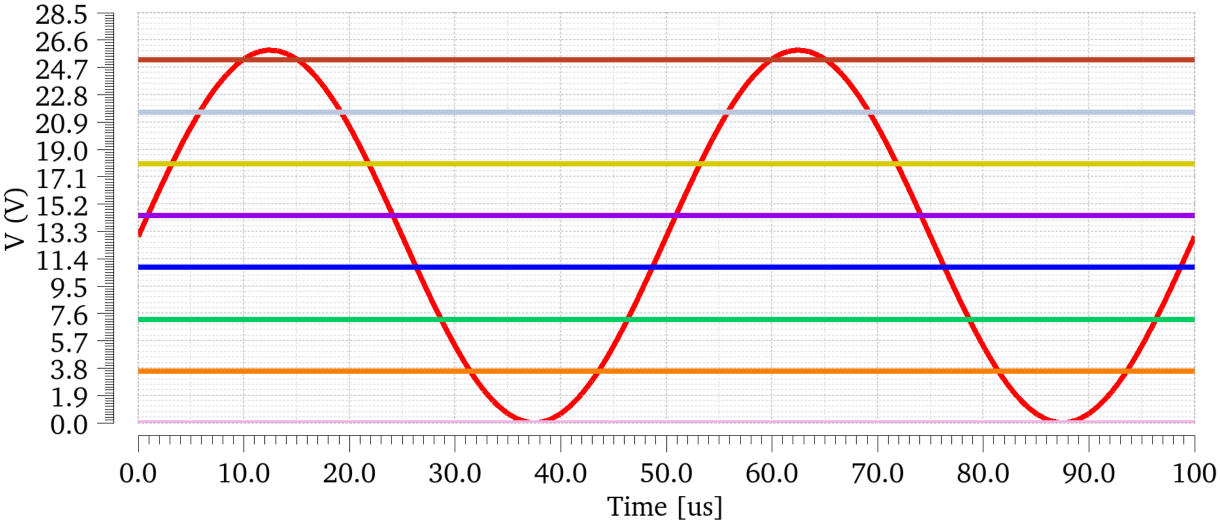


Figure 8: Reference voltage and NLC voltage levels

The resulting output voltage and load current for a 4 Ω resistive load are shown in Fig. 12. The converter successfully synthesises a staircase approximation of the sinusoidal reference while delivering the corresponding load current.

These results confirm correct multilevel waveform synthesis and proper load driving capability under NLC operation. Because the converter operates at fine cell-voltage resolution (3.6 V per level), the NLC approach inherently achieves low harmonic distortion without requiring high-frequency PWM. This significantly reduces switching frequency and associated switching losses compared to conventional two-level converters, where PWM is necessary to emulate intermediate voltage levels.

7 Experimental Results

The proposed converter design was fabricated using a 130-nm BCD technology. All power switches are implemented using N-type devices to minimise on-state resistance and reduce the layout area.

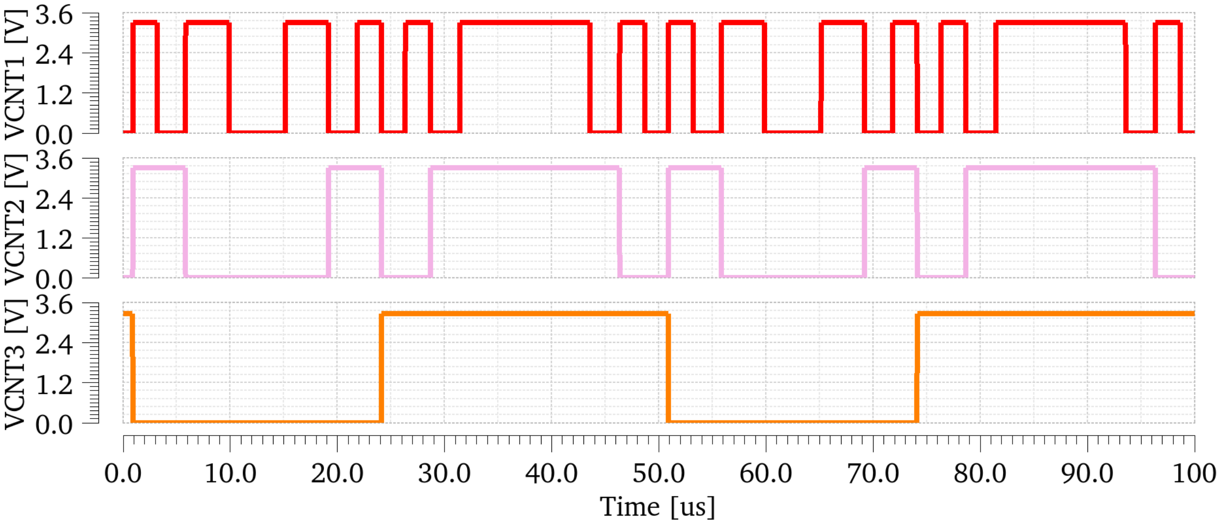


Figure 9: Outputs of the NLC modulator

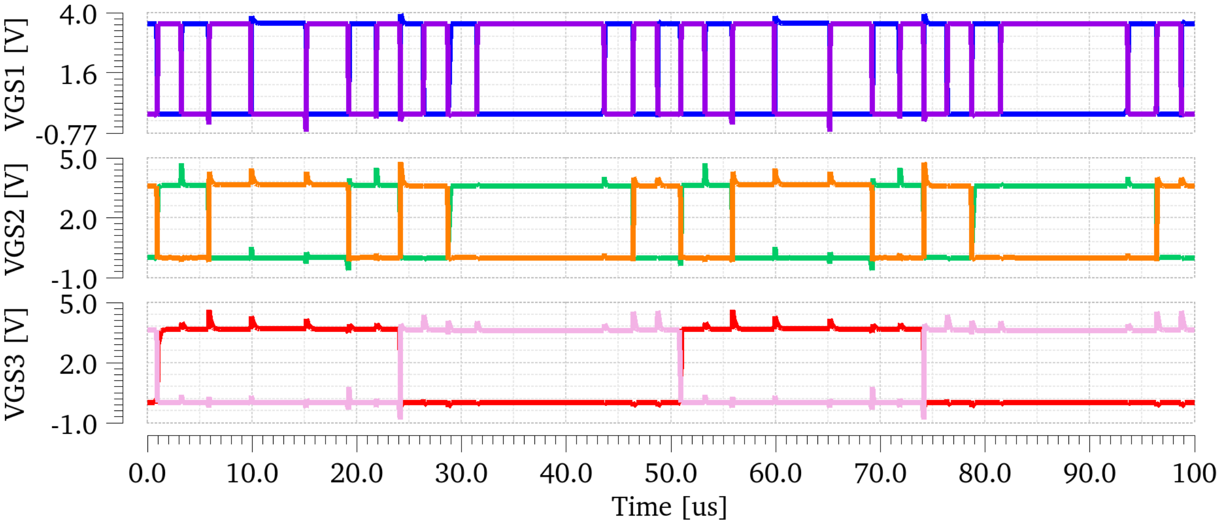


Figure 10: Gate-source voltages of high and low-side switches for each BTMLC level

To optimise area efficiency and lower metallisation resistance, power pads are placed directly over the active regions of the devices using a BOAC pad structure. The total chip area is $20.52\,\mathrm{mm}^2$, and the top-level layout is shown in Fig. 13(a). The top part of the chip includes the four lower battery taps, while the bottom part contains the remaining four taps, with the output terminal located at the center of the chip.

The experimental validation of the fabricated BTMLC chip is carried out using three approaches.

First, to verify the correct and reliable operation of the proposed control circuits, including voltage level shifters, gate drivers, and driver-rail supply generators, the chip is packaged in a commercial JLCC, which allows access to multiple test points for characterisation.

Second, a high-current BTMLC chip is implemented on a custom board with manual wire bonding to enable higher current operation and to estimate resistance and efficiency.

Finally, to validate high-voltage operation, two BTMLC chips are stacked on a board to synthesise higher-voltage waveforms from sixteen battery taps.

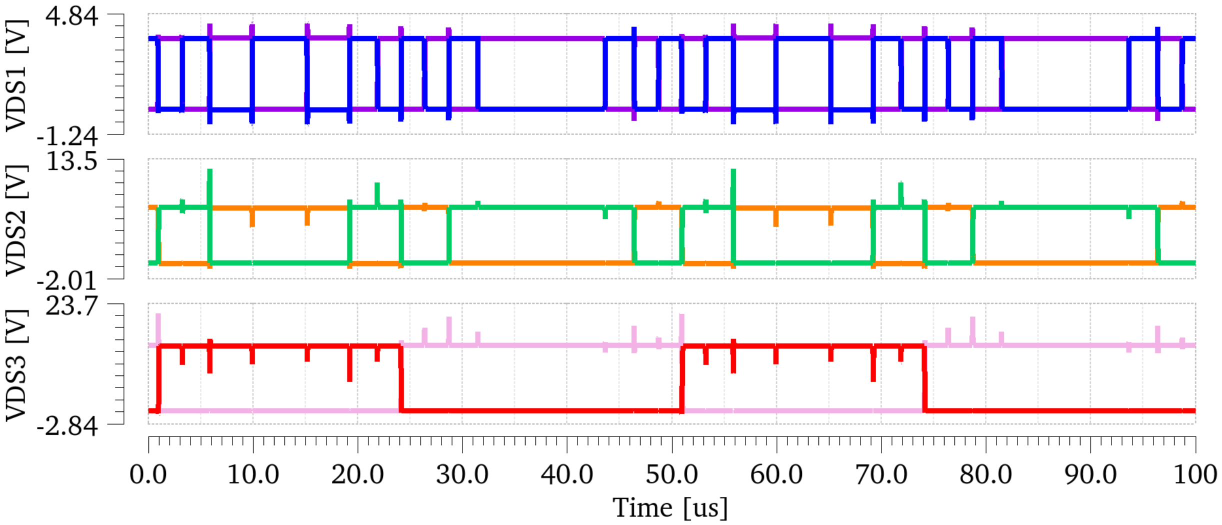


Figure 11: Drain-source voltages of high and low-side switches for each BTMLC level

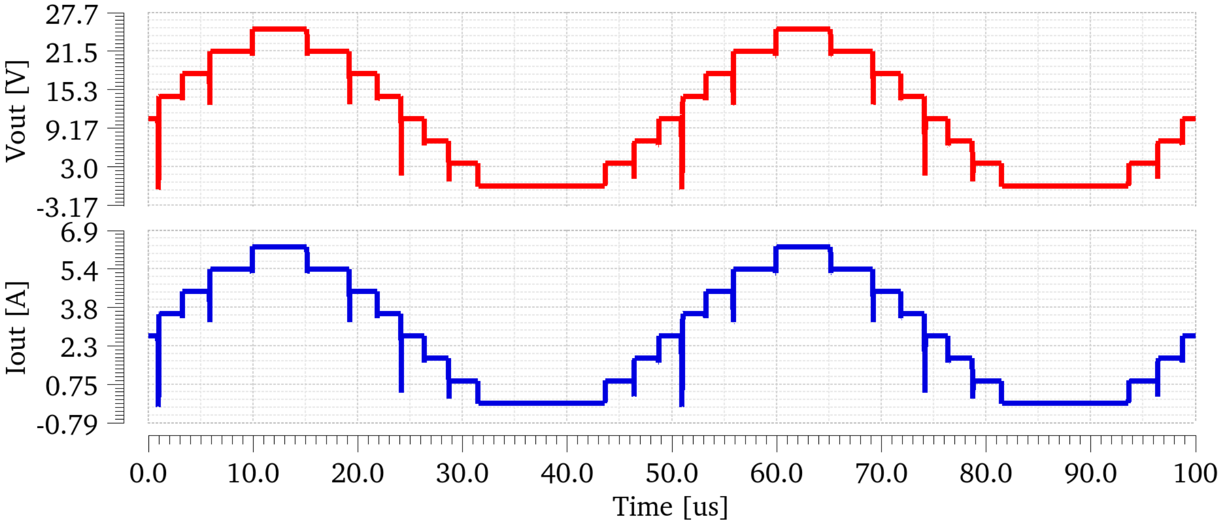


Figure 12: Output voltage and load current at inputs of 3.6 V and 5 kHz output frequency

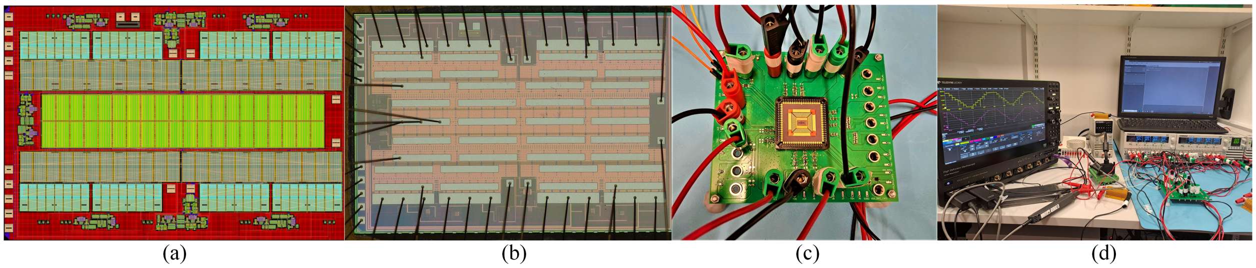
7.1 Basic Functional Validation Using a JLCC Package

To facilitate testing and provide access to the converter test points, the prototype was packaged in a JLCC. A chip micrograph with wire bonds is shown in Fig. 13(b). Each power pad is wire-bonded using three 25 μm gold wires, which is sufficient for basic functional validation. Several internal pads were included to investigate resistance reduction through external interconnect techniques such as additional wire bonds or flip-chip stud bumping. These options, however, were not explored in this work. Only the peripheral pads were used for PCB connection and current delivery.

The output was taken from one side of the chip using three wire bonds, since the opposite side contains other circuits (not shown in the figure). This resulted in a suboptimal current path and an increased series resistance, but the configuration is sufficient to demonstrate the fundamental operation of the proposed control circuits.

To validate the chip's functionality as a multi-tap voltage selector, the test board shown in Fig. 13(c) was employed. The JLCC package was mounted in a dedicated socket on a two-layer PCB with decoupling capacitors across the multiple supply rails.

The test-bench setup in Fig. 13(d) was established to operate the system, which is schematically similar to the one used in Part I in Fig. **??**. The converter was driven by three logic signals generated by a B-Box RCP microcontroller.



(a) (b) (c) (d)

Figure 13: (a) Top-level converter chip layout (5474 μm × 3750 μm). (b) Die micrograph wire-bonded to a JLCC-84 package. (c) Test board with 84-pin JLCC socket and decoupling capacitors. (d) Test-bench setup including logic microcontroller, multi-channel power supplies, resistive loads, and oscilloscope with voltage and current probes.

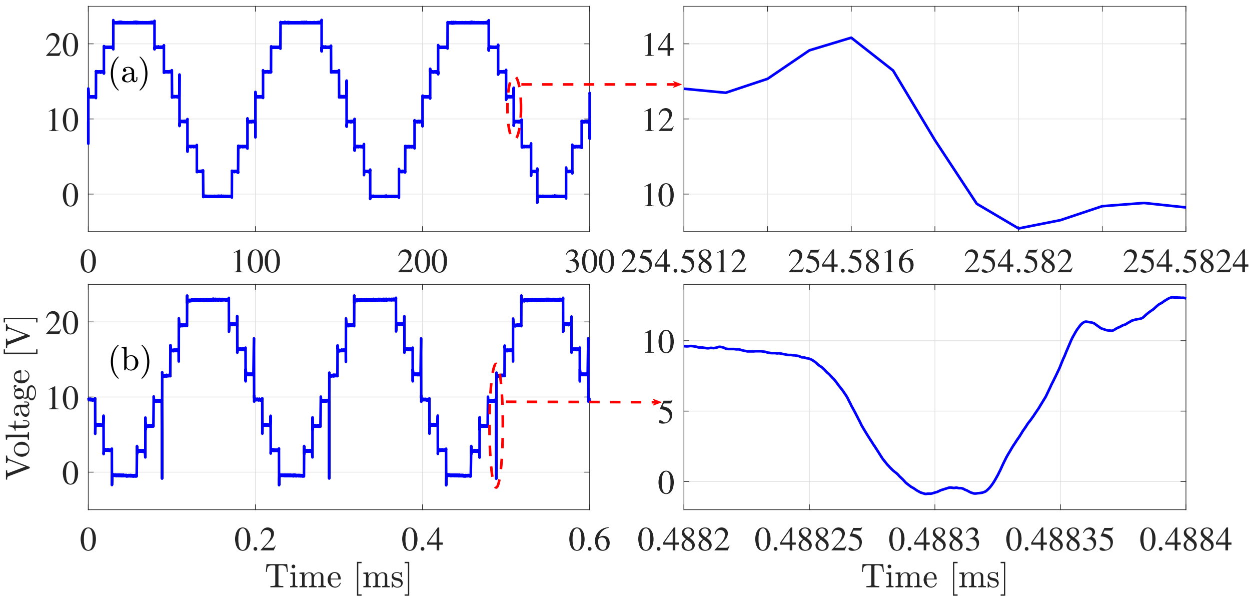


Figure 14: Measured converter output voltage waveforms at frequencies of (a) 10 Hz and (b) 5 kHz.

An additional supply provided $V_{\text{cell},8}$, which is required only for the top-most module in a multi-chip stacked configurations.

Under no-load conditions, the measured output voltage waveforms are shown in Fig. 14(a)-(b) for output frequencies of 10 Hz and 5 kHz. The right-hand subplots provide zoomed-in views of the measured output voltage transitions.

An overshoot is observed in Fig. 14(a) during the switching transition from $V_{\text{cell},4}$ to $V_{\text{cell},3}$. This overshoot arises due to the specific switching sequence: prior to the transition, the low-side switches in Level I and Level II (M_5 and M_{11}), along with the high-side switch in Level III (M_{14}), are all turned on. During the transition from $V_{\text{cell},4}$ to $V_{\text{cell},3}$, switch M_6 turns on first, followed by the switches in Level II and Level III, which causes the output voltage to momentarily reach the higher-tap voltage.

A short voltage dip, lasting approximately 100 ns, is also observed in Fig. 14(b) during the transition from $V_{\text{cell},3}$ to $V_{\text{cell},4}$. In this case, the output voltage briefly drops to zero since the low-side switches in Level I and Level II turn on first, with the Level III switches engaging shortly afterward.

These results demonstrate the capability of the proposed design to synthesise staircase voltage waveforms over a wide frequency range, with a voltage waveform resolution equal to a single cell level.

To enable current delivery to a resistive load, the voltage taps were decoupled using surface-mounted ceramic capacitors of varying capacitance values: 0.1 μF, 0.33 μF, 10 μF, and 22 μF. Figures 15(a)-(b) present the output voltage and corresponding current waveforms at 10 Hz and 5 kHz. Initially, each tap voltage was configured to 3.3 V and then increased to 3.4 V at 5 kHz.

A noticeable voltage drop is observed, primarily due to one-sided long wire bonds at the output pads. The current is forced to traverse horizontally across the chip output pad, introducing high path resistance. Despite this packaging limitation, the converter is capable of delivering approximately 2.5 A, which is close to the fusing current of the three parallel 25 μm gold wire bonds.

The path resistance, R_{path}, is estimated from the DC measurements summarised in Table 1. In this test, the converter was operated as a DC-DC voltage tap-selector, delivering approximately 2 A of DC current to a variable resistive load across all output voltage levels, ranging from 3.3 V to 23.3 V. The estimated path resistance is approximately 0.4 Ω, which encompasses various contributors within the current path, including wire-bonding resistances, PCB trace resistances, package lead and connector cable resistances.

It is also observed that the input and output currents are nearly identical, with maximum difference of approximately 10 mA. This current difference accounts for the consumption of the stacked level shifter circuits.

Thermal performance was also evaluated. The temperature rise was recorded for two operating conditions: (1) when a constant 2 A DC current was drawn from the highest voltage tap, and (2) during operation under time-varying conditions corresponding to the waveforms in Fig. 15(a). These thermal profiles are presented in Figs. 16. For the 2 A DC case, the peak temperature reached approximately 66°C, concentrated around the output pad and tap seven, as expected. Under time-varying operation, the temperature reduced to around 46°C due to a lower average output current (approximately

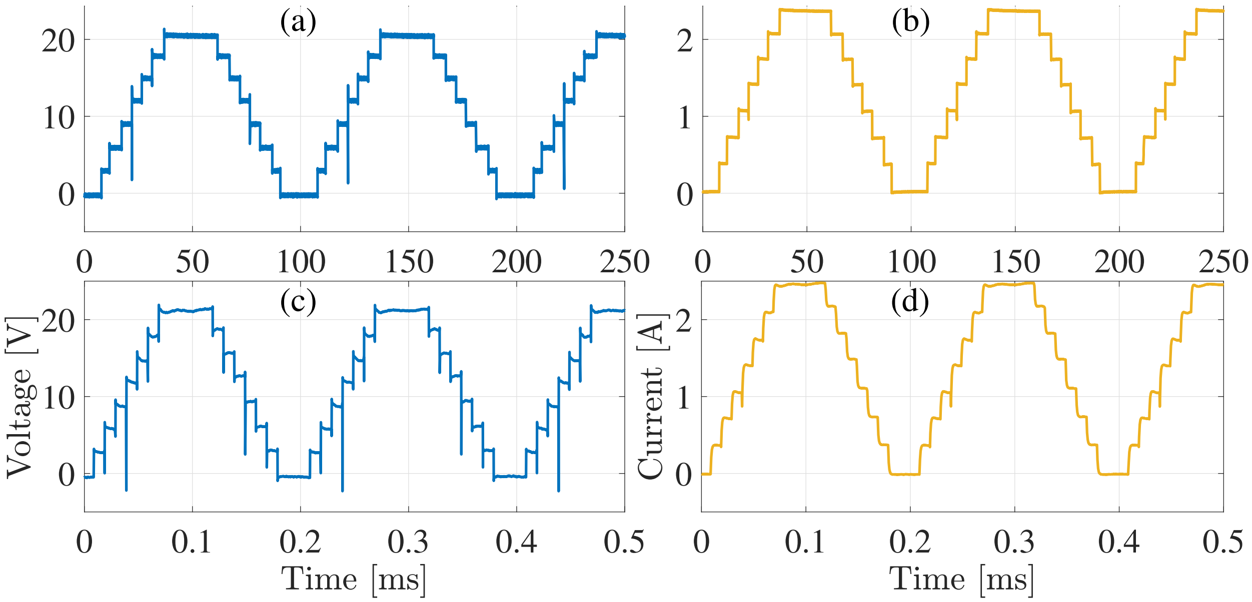


Figure 15: Measured output voltage and current waveforms: (a)–(b) at 10 Hz and 3.3 V input and (c)–(d) at 5 kHz and 3.4 V input.

Table 1: Measured DC parameters

V_{in} (V)	V_{out} (V)	I_{out} (A)	P_{out} (W)	I_{in} (A)	R_{path} (Ω)
3.3	2.484	2.004	4.663	2.009	0.408
6.6	5.782	2.005	11.22	2.010	0.409
9.9	9.088	2.010	17.77	2.015	0.406
13.2	12.41	2.007	24.37	2.0098	0.395
16.5	15.73	2.010	31.02	2.017	0.385
19.8	19.03	2.006	37.53	2.014	0.385
23.1	22.31	1.995	43.79	2.006	0.395

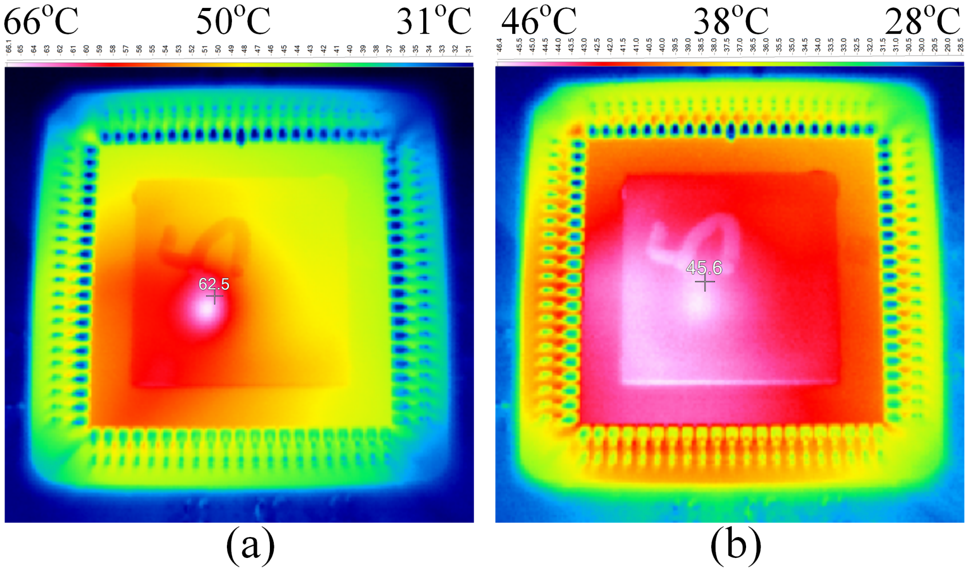


Figure 16: (a) Heat map for 2 A constant load current, (b) Heat map for time-varying load current with NLC modulation and 10 Ω load

half of the DC value). In this case, the heat distribution is more spread across the upper voltage taps and output pad regions.

To characterise the performance of the proposed control circuits and drivers of the converter, Fig. 17 shows the measured gate-source voltage (V_{GS}) waveforms for different switching pairs, acquired asynchronously with pseudo-sinusoidal NLC. These results validate the functionality of the proposed gate drive voltage generation circuits, which successfully derive appropriate drive voltages directly from the input sources.

The measured dead-time and rise/fall time durations are well correlated with the preset design values. Levels I and II exhibit dead-times of approximately 80–85 ns, while Level III shows a longer dead-time of around 250 ns. The gate-source voltage in Level I rises to 90% of its final 3.3 V value within 60 ns and falls in about 30 ns. In Level II, the rise and fall times are approximately 190 ns and 35 ns, respectively. The slowest transition is observed in Level III, with rise and fall times of approximately 350 ns and 50 ns. The transition speeds of the V_{GS} waveforms are primarily influenced by the sizes of the transistors used in the driver-rail generation circuits. As expected, Level III exhibits the slowest response, since the control signals must propagate through the first and second levels of the driver-rail generation hierarchy.

The measured drain-to-source voltage (V_{DS}) waveforms for switches in Level I, Level II, and Level III are shown in Fig. 18. These waveforms confirm that the devices operate well within their maximum rated voltage limits: 3.3 V for Level I, 6.6 V for Level II, and 13.2 V for Level III when the input voltages are set to 3.3 V.

Figure 19(a)–(n) presents measurements of several converter nodes, taken with respect to ground, while synthesising a half-sine waveform using NLC. These measurements include both gate voltages and internal switching node voltages. The results confirm the reliable operation of the converter circuit under realistic switching sequences used to synthesise a half-sine waveform and validate the proposed driver-rail generators and other control signals processing circuits. For example, Figures 19(e) and (f) display the outputs of the top two half-bridge submodules in Level I, $V_{\mathrm{SW3,L1}}$ and $V_{\mathrm{SW4,\,L1}}$. The first switches between 13.2 V and 16.5 V, while the second switches between 19.9 V and 23.1 V. These measurements demonstrate that all Level I submodules successfully achieve the expected output voltage swings with full tap-to-tap transitions.

7.2 Higher-Current and Higher-Voltage Validation

To enable higher-current and higher-voltage operation of the BTMLC IC, a custom two-layer PCB with an ENIG surface finish was developed. The ENIG coating improves the reliability of the wire-bonding process. The PCB incorporates 0.1 μF and 22 μF ceramic decoupling capacitors to suppress high-voltage transients and mitigate inductive ringing, thereby allowing pulsed current delivery through multiple converter terminals. Each power pad was bonded with 10–12

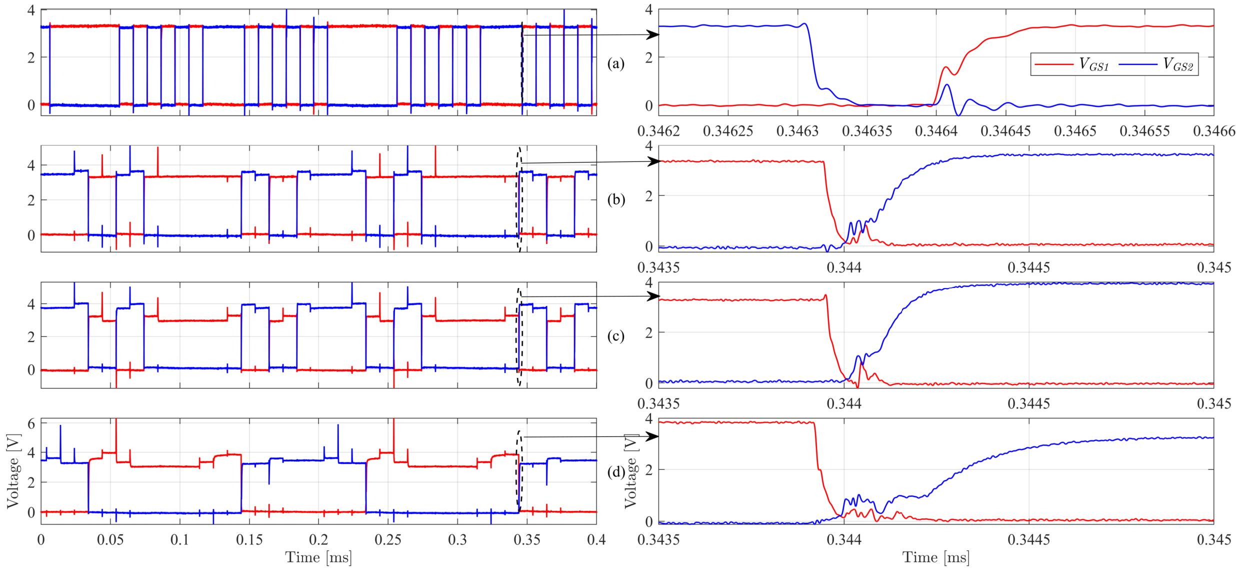


Figure 17: Measured gate-source voltage waveforms of the high-side and low-side switches for (a) Level I second half-bridge submodule, (b) Level II first half-bridge submodule, (c) Level II second half-bridge submodule, and (d) Level III half-bridge submodule.

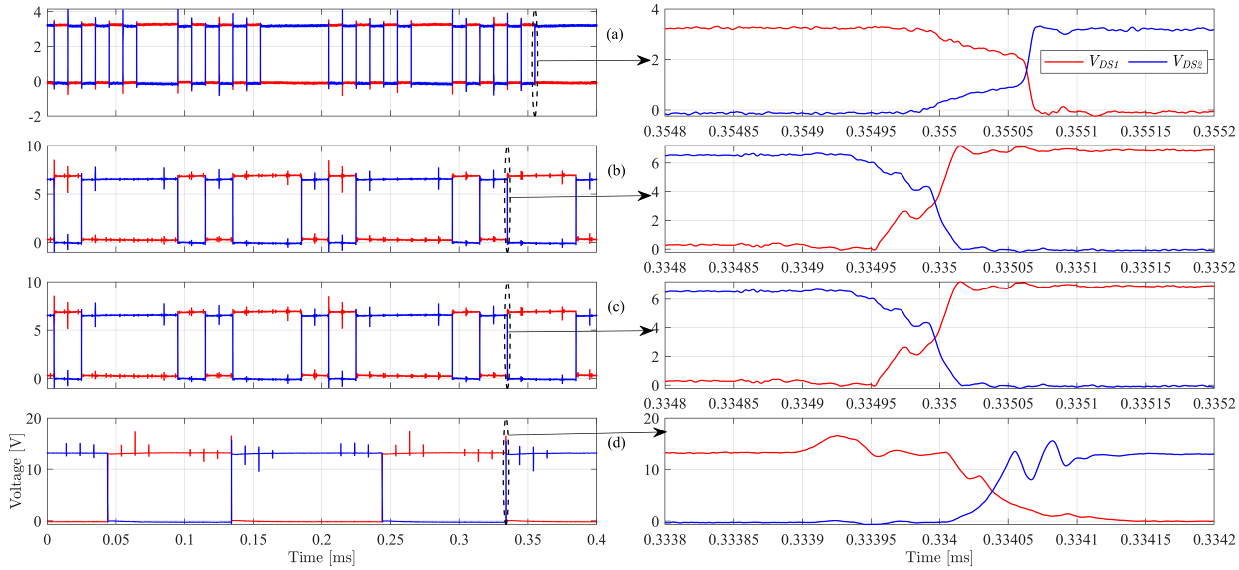


Figure 18: Measured drain-source voltage waveforms of the high-side and low-side switches for (a) Level I second half-bridge submodule, (b) Level II first half-bridge submodule, (c) Level II second half-bridge submodule, and (d) Level III half-bridge submodule.

aluminium wire bonds of 33 μm diameter. Contrary to the JLCC packaging, the output pads were wire-bonded from both sides using multiple distributed wires across the chip area to improve current handling capability. Two wire-bonded BTMLC dies are shown in Fig. 20(a)–(b).

The wire-bonding process confirmed the robustness of the BOAC power pad structures using a fine-pitch flat-wedge bonding method, further verifying their feasibility and reliability.

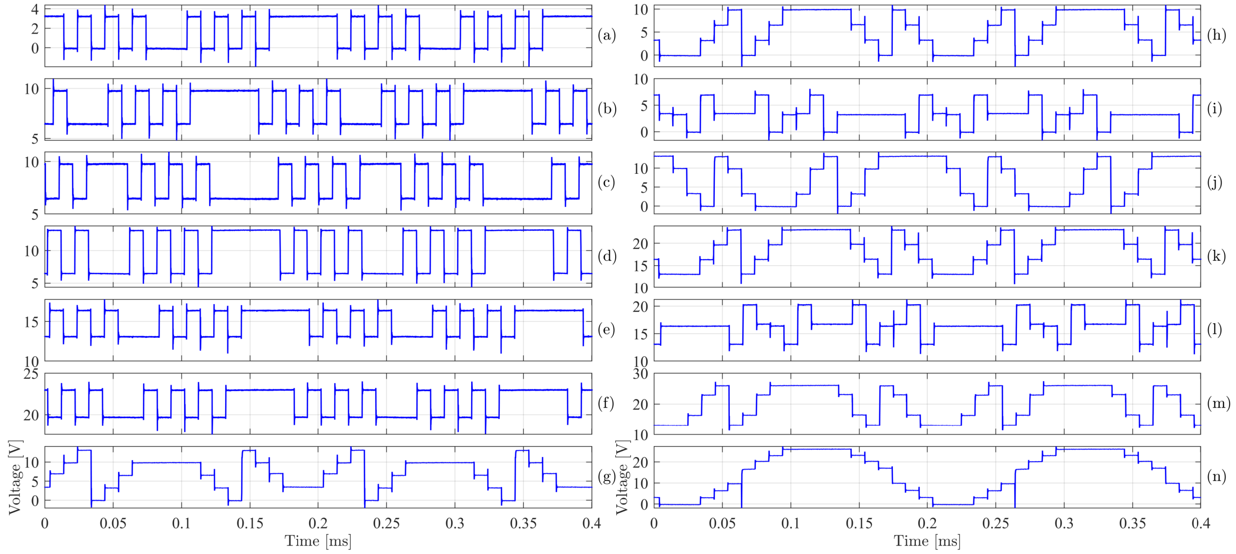


Figure 19: Measured voltage waveforms under NLC modulation at 5 kHz switching frequency and 3.3 V input voltage for: (a) $V_{\mathrm{SW1,L1}}$, (b) $V_{\mathrm{SW2,L1}}$, (c) gate voltage of M_3, (d) gate voltage of M_4, (e) $V_{\mathrm{SW3,L1}}$, (f) $V_{\mathrm{SW4,L1}}$, (g) gate voltage of M_{13}, (h) $V_{\mathrm{SW1,L2}}$, (i) gate voltage of M_9, (j) gate voltage of M_{10}, (k) $V_{\mathrm{SW2,L2}}$, (l) gate voltage of M_{11}, (m) gate voltage of M_{12}, and (n) gate voltage of M_{14}.

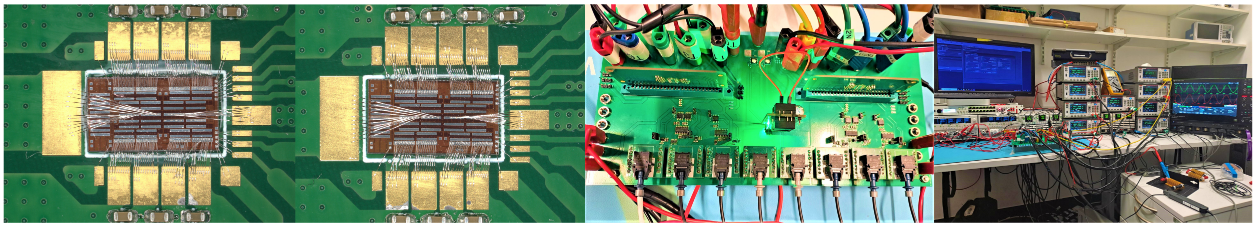

(a) (b) (c) (d)

Figure 20: (a)–(b) Micrographs of BTMLC dies wire-bonded to daughter PCBs using 10–12 AL 33 μm wire bonds per pad, with decoupling capacitors. (c) Test board (motherboard) with edge-connector sockets for daughter boards, and an external half-bridge stage with plug-in gate driver (centre). (d) Test-bench setup showing the test board connected to 16 power supplies and resistive loads, controlled by a B-box microcontroller, with an oscilloscope equipped with voltage and current probes.

To simplify the characterisation process, a 50-contact card-edge connector was employed to interface the daughterboard PCBs containing the wire-bonded BTMLC dies with test-board, as illustrated in Fig. 20(c). The test-board was designed with two edge-connector sockets, enabling rapid plug-in/plug-out of multiple daughterboards.

To extend the operating voltage, an external half-bridge submodule with a dedicated gate driver was included on the test-board PCB, combining the outputs of two BTMLC modules as illustrated in Fig. 3(c). This configuration enabled higher-voltage operation using sixteen battery/supply voltage taps. The complete test-bench for validating the high-current and high-voltage operation of the BTMLC ICs is shown in Fig. 20(d).

To characterise the converter with the proposed packaging method, the path resistance was evaluated by operating a single converter module as a DC–DC tap-selector while sourcing DC currents from 2 A to 6 A. As shown in Fig. 22, the estimated total resistance across all voltage taps ranged from 60 mΩ to 85 mΩ over the tested current range. The resistance was obtained from the static voltage drop at each current level for the selected tap. Although differences are visible between taps, the absolute variation remains relatively modest, typically within a range of approximately 20–25 mΩ across the full current span. It should be noted that the truncated vertical axis (starting at 55 mΩ rather than zero) visually exaggerates these differences. When viewed relative to the nominal resistance level (around 70–80 mΩ), the spread is comparatively small. Furthermore, accurate measurement of milliohm-level resistance in a converter IC is inherently challenging. The extracted values include contributions from bond wires, PCB traces, contact resistances,

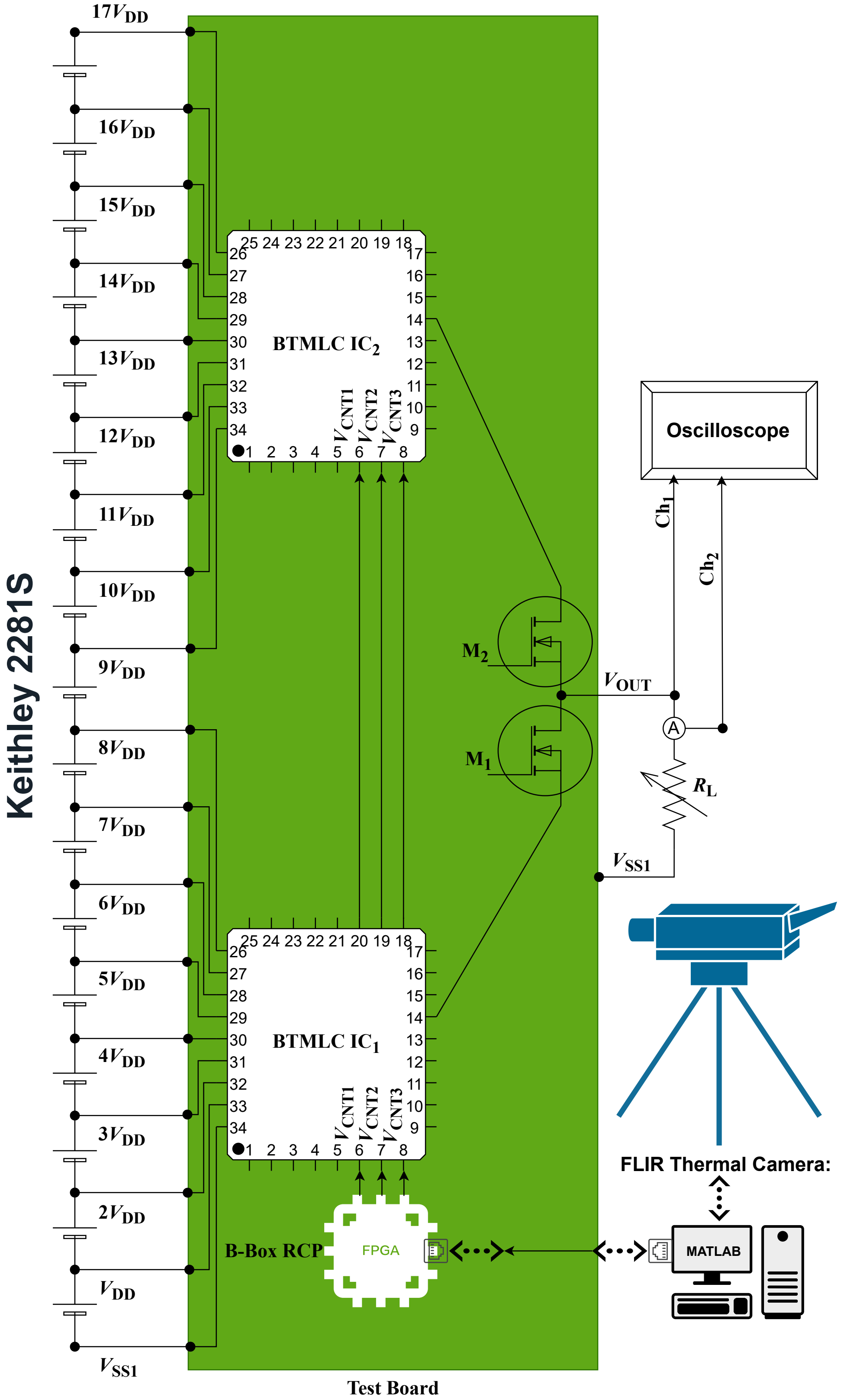


Figure 21: Schematic of the stacked BTMLC ICs testbench

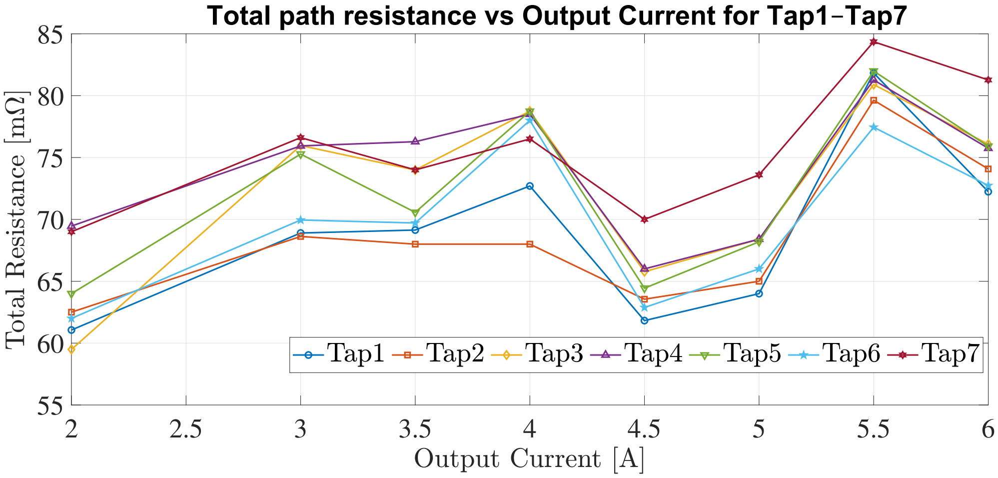


Figure 22: Measured converter total path resistance across all voltage taps

and measurement lead parasitics, all of which introduce uncertainty. Small current-sensing and thermal effects can also influence the results. Consequently, the observed variation should be interpreted within the limits of measurement accuracy, and overall the resistance consistency across taps can be considered satisfactory.

To estimate the efficiency, each single voltage tap was selected to supply a constant DC current from 2 A to 6 A. For each operating point, the input power drawn from the corresponding battery cells and the output power delivered to the load were measured. The efficiency was then calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}} I_{\text{out}}}{P_{\text{in}}}. \tag{6}$$

This procedure was repeated for each selectable voltage tap, enabling comparison of efficiency performance across different conduction paths and current levels, as shown in Fig. 23.

The measured efficiency varied from 98.5% to 85%, demonstrating the effectiveness of the optimised converter layout and the positive impact of the BOAC pads design. Further efficiency improvement is expected if the daughterboards are interfaced directly without the edge-connector sockets, which were primarily included to facilitate rapid testing.

The variation in efficiency across selectable voltage taps can be explained by examining the relationship between output power and conduction losses. For a given load current I, the dominant loss mechanism is conduction loss, which can be approximated as $P_{\text{loss}} = I^2 R_{\text{path}}$, where R_{path} represents the total effective resistance of the conduction path.

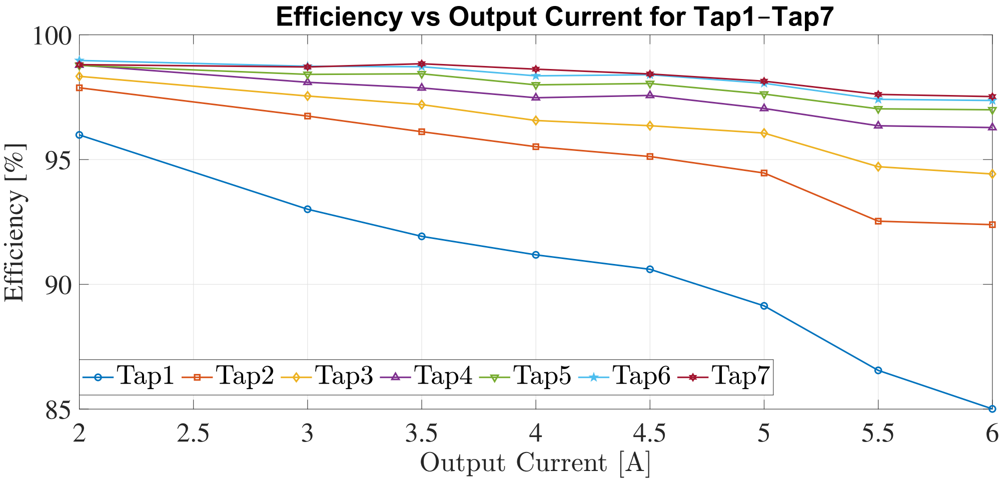


Figure 23: Converter efficiency with load current across all selectable voltage taps

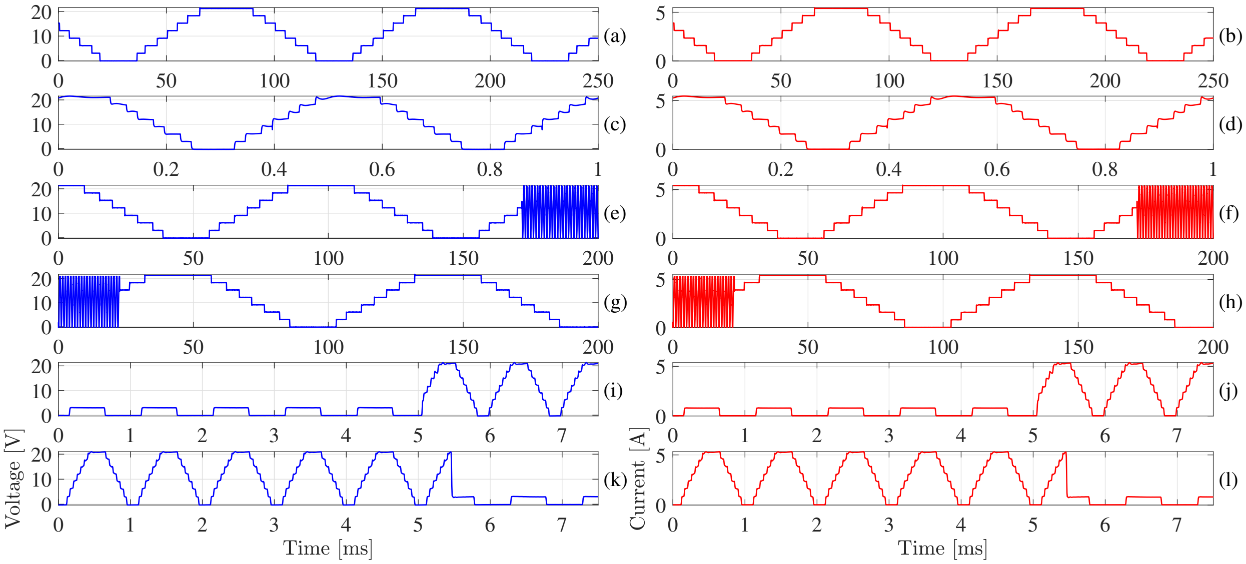


Figure 24: Measured output voltage and current waveforms for a single BTMLC module at: (a)–(b) 4 Ω load at reference NLC frequency of 10 Hz, (c)–(d) 4 Ω load at reference NLC frequency of 2 kHz, (e)–(f) NLC reference frequency dynamically varied from 10 Hz to 1 kHz, (g)–(h) NLC reference frequency dynamically varied from 1 kHz to 10 Hz, (i)–(j) NLC reference voltage varied arbitrarily from 3.3 V to 23.1 V, and (k)–(l) NLC reference voltage varied arbitrarily from 23.1 V to 3.3 V.

Although the number and type of switches in the conduction path are constant for different taps, the output power scales with the selected voltage level according to $P_{\text{out}} = V_{\text{out}}I$. Therefore, at higher voltage taps, the same absolute conduction loss represents a smaller fraction of the output power, resulting in improved efficiency.

Conversely, as the load current increases, conduction loss increases quadratically ($\propto I^2$), while output power increases only linearly ($\propto I$). Consequently, the relative contribution of conduction loss becomes larger at higher currents, leading to the observed reduction in efficiency with increasing load current. These trends are based on the assumption that conduction losses dominate the efficiency behaviour of the converter.

An NLC-based set of measurements was performed to validate time-varying, high-current operation with variable frequency and voltage steps. As shown in Fig. 24(a)–(b) and Fig. 24(c)–(d), the converter successfully delivered current to a 4 Ω load at reference NLC frequencies of 10 Hz and 2 kHz, respectively. Furthermore, the reference frequency was dynamically varied from 10 Hz to 1 kHz and vice versa, as illustrated in Fig. 24(e)–(f) and Fig. 24(g)–(h), while maintaining robust operation throughout the transitions. Finally, the NLC reference voltage was varied arbitrarily between 3.3 V and 23.1 V in both directions, as shown in Fig. 24(i)–(j) and Fig. 24(k)–(l), demonstrating stable converter response to rapid voltage changes.

These results confirm the converter's robustness under dynamic frequency and voltage variations, highlighting its potential for deployment in larger systems requiring higher-voltage and higher-current operation for practical applications.

To demonstrate the stacking capability of the proposed converter, two BTMLC modules were interfaced with sixteen supply taps, with their outputs multiplexed by an off-chip power stage employing 50 V power MOSFETs, as illustrated in Fig. 21. While this additional circuitry was not optimised for low on-state resistance or compactness, it served to validate the feasibility of voltage stacking. A corresponding set of output voltage and current measurements, obtained with an 8 Ω load, is presented in Fig. 25. As observed, the stacked configuration synthesises voltage waveforms with sixteen discrete steps of 3.3 V resolution, producing smooth half-sine waveforms while simultaneously delivering current to the load at varying frequencies and voltage levels. For example, the reference modulation waveform was stepped from 3.3 V to 49.5 V and vice versa in Fig. 25(g)–(h) and Fig. 25(i)–(j), respectively, demonstrating a robust and stable dynamic response even at such large voltage steps.

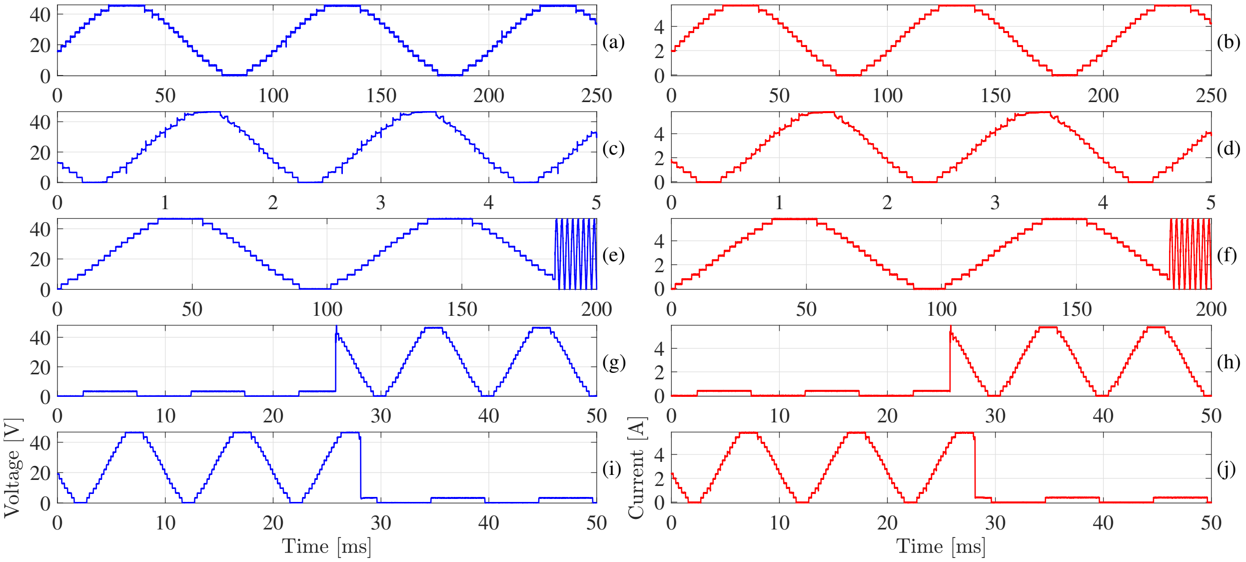


Figure 25: Measured output voltage and current waveforms for two stacked BTMLC modules at: (a)–(b) 8 Ω load at reference NLC frequency of 10 Hz, (c)–(d) 8 Ω load at reference NLC frequency of 500 Hz, (e)–(f) NLC reference frequency dynamically varied from 10 Hz to 500 Hz, (g)–(h) NLC reference voltage varied arbitrarily from 3.3 V to 49.5 V, and (i)–(j) NLC reference voltage varied arbitrarily from 49.5 V to 3.3 V.

7.3 Thermal Resistance Estimation

A voltage-selection pass element was characterized at the highest tap while delivering a load current of 6 A. The effective on-path resistance was measured as 82 mΩ, as shown in Fig. 22. A thermal camera measurement reported a peak chip temperature of $T_{\text{chip}} = 102°\text{C}$ and a minimum temperature on the surrounding PCB pads of $T_{\text{pcb}} = 28°\text{C}$, as depicted in Fig. 26. Assuming the dominant loss mechanism is ohmic (conduction) loss in the pass path, the dissipated power is

$$P_{\text{cond}} = I^2 R_{\text{path}}. \tag{7}$$

Substituting the measured values results in 2.952 W.

The corresponding voltage drop across the path is

$$\Delta V = I R_{\text{path}} = 6\ \text{A} \cdot 0.082\ \Omega = 0.492\ \text{V}. \tag{8}$$

The temperature rise from the local surroundings to the hottest region of the chip is

$$\Delta T = T_{\text{chip}} - T_{\text{pcb}} = 102 - 28 = 74°\text{C}. \tag{9}$$

An effective thermal resistance from the chip hot-spot to the local environment (approximated here by the nearby PCB pad temperature) can be estimated as

$$\theta_{\text{eff}} \approx \frac{\Delta T}{P_{\text{cond}}} = \frac{74°\text{C}}{2.952\ \text{W}} = 25.1\ °\text{C/W}. \tag{10}$$

This result indicates that, under the present mounting and layout conditions, each additional watt of dissipated power raises the chip hot-spot temperature by approximately 25 °C relative to the local PCB temperature.

Although the electrical efficiency can be high, the absolute heat generated at high current can still be significant. In this case, an on-path resistance of 82 mΩ at 6 A leads to nearly 3 W of conduction loss, which is sufficient to produce a large temperature rise if the thermal resistance to ambient is high. The observed large temperature gradient between the chip (102°C) and surrounding copper pads (28°C) suggests limited heat transfer from the heat-generating region into the PCB copper.

The large temperature difference observed between the chip hot-spot and the surrounding PCB pads indicates that heat removal from the active region is limited by the thermal coupling between the silicon and the board. In the present experimental configuration, the dominant heat-flow path is therefore constrained by the die attach material, the

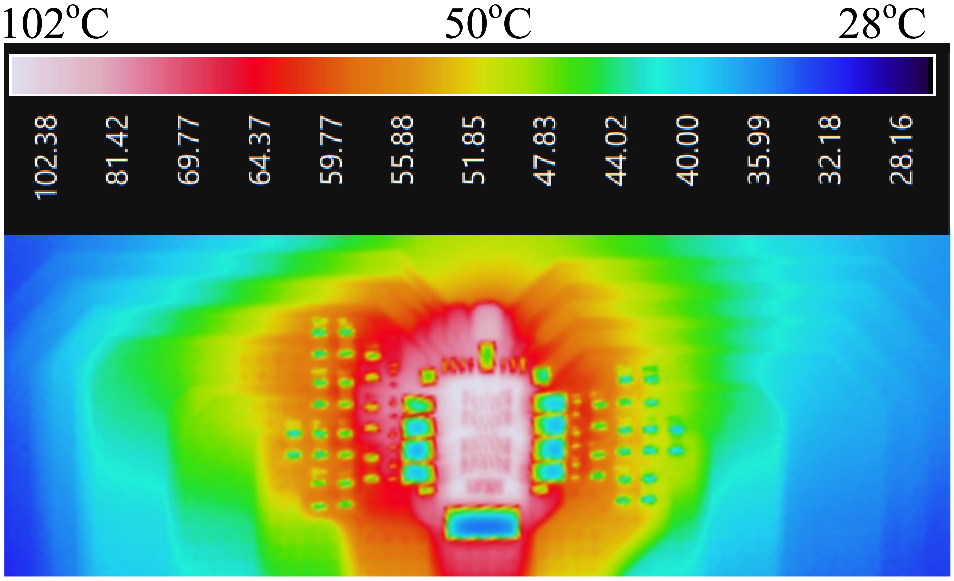


Figure 26: Heat map for 6 A DC current drawn from eighth tap without any external cooling

available copper area, and the absence of efficient vertical heat spreading into the PCB. Consequently, the measured effective thermal resistance of approximately $25\ ^\circ\mathrm{C}/\mathrm{W}$ is mainly determined by the thermal impedance between the heat-generating region and the surrounding copper planes.

This result suggests that the thermal behavior of the device is strongly dependent on the quality of the thermal interface and the PCB heat-spreading capability. In particular, the weak thermal coupling between the chip and the large copper pads explains the coexistence of a high chip temperature ($102^\circ\mathrm{C}$) and a comparatively low PCB temperature ($28^\circ\mathrm{C}$). The experiment therefore highlights that, even for moderate conduction losses, insufficient thermal extraction can lead to substantial local temperature rises.

From an experimental standpoint, these observations indicate that any modification that enhances the thermal coupling between the chip and the MOSFETs, or increases the effective heat-spreading area, would reduce the temperature gradient between the active region and the board and thus lower the peak operating temperature. The measured data provide a quantitative reference for evaluating such improvements in subsequent prototypes or mounting configurations.

Overall, the temperature rise is governed by the product $P_{\mathrm{cond}}\theta_{\mathrm{eff}}$; therefore, reducing either the dissipated power (via lower R_{path}) or the effective thermal resistance (via improved heat extraction and spreading) will decrease the maximum chip temperature.

8 Conclusion

This work presented a hybrid architecture for scalable multilevel power conversion based on binary-tree multilevel converter integrated circuit modules combined with discrete switching stages. The proposed approach enables voltage synthesis directly from battery-cell voltage levels while extending the overall converter voltage capability through external stages operating at lower switching frequencies. By partitioning high-frequency switching and level generation to integrated low-voltage devices, the architecture achieves compact implementation and improved efficiency while maintaining scalability to higher voltage levels.

To enable this architecture, a fully integrated eight-tap BTMLC module was designed and fabricated in a 130-nm BCD technology using LDMOS power devices. The converter integrates the power switches, control logic, gate drivers, voltage level shifters, and protection circuitry within a single chip. A low-cost gate-drive supply architecture was developed to derive the required driver rails directly from the battery stack using standard devices, allowing a larger portion of the silicon area to be dedicated to the power devices, thereby improving power-conversion efficiency and increasing current capability.

In addition, a BOAC layout strategy was implemented to reduce die area and conduction resistance by placing bond pads directly above the power switches. The reliability of this approach was verified experimentally by attaching multiple wire bonds to the BOAC pads without device failure, demonstrating the feasibility of this packaging strategy in low-k technologies.

Experimental results from the fabricated prototype confirmed robust operation over a wide operating range. Initial validation using a commercial JLCC package demonstrated reliable operation up to 2.5 A, while optimised packaging with multiple wire bonds enabled output currents of up to 6 A. Furthermore, the scalability of the proposed architecture was demonstrated by stacking two BTMLC modules and combining their outputs through an external half-bridge stage, enabling voltage synthesis beyond the breakdown limits of the semiconductor technology.

These results demonstrate that the proposed hybrid IC–discrete architecture provides a compact, scalable, and cost-effective solution for multilevel power conversion. The BTMLC module therefore represents a promising building block for future high-voltage converters, battery-integrated power electronics, and compact motor drive systems.

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