# Power Circuit AI: Designing Power Electronic Circuits for Motor Drives with Generative Artificial Intelligence

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***Abstract*—The design of power electronic converters is a multi-physics optimization challenge that has traditionally resisted the high levels of automation seen in digital VLSI. While Large Language Models (LLMs) offer a promising interface for capturing high-level design intent, they inherently lack the domain understanding required to generate manufacturing-ready hardware, often resulting in hallucinations and invalid netlists. This paper presents a novel, autonomous multi-agent framework that orchestrates the end-to-end design of power electronic circuits from natural language specifications to clean Printed Circuit Boards (PCBs) without fine-tuning the underlying LLMs. The proposed methodology utilizes a constrained environment to bridge the stochastic gap between generative AI and rigid Electronic Design Automation (EDA) tools. The logical validity of the circuit is ensured by deploying specialized agents for device specification, component selection, SKiDL-based netlist generation, and layout completion. The framework is validated through the autonomous generation of a 400V 3-phase converter for a variable frequency drive. Results demonstrate that while the system achieves 100% logical connectivity and automated routing, transitioning from logical correctness to physics-aware layout optimization and adhering to creepage and clearance requirements remains a critical frontier. The study concludes that pairing LLM agents with deterministic auto routers solves the connectivity problem but requires further integration of physics-based feedback loops to meet the requirements of commutation loop inductance, thermal management, creepage, and clearance requirements. Additionally, it also details the placement limitations within the schematic and flags any components that have not been included.**

***Index Terms*—Artificial Intelligence, Circuit AI, Power Circuit AI, Generative Design, Electronic Design Automation, Large Language Models, Layout, Schematics, Printed Circuit Boards, Power Electronics, Hardware Synthesis, PCBs**

## I. Introduction

The design of power electronic (PE) systems, particularly variable frequency motor drives (VFDs) [1], remains a highly manual and expert-driven endeavor that has resisted the high levels of automation standard in digital logic synthesis. Traditionally, this design flow is an iterative process requiring deep domain expertise to navigate multi-dimensional trade-offs between performance, power density, and thermal reliability [2], [3]. For motor drives, this complexity is magnified by the requirement to integrate high-speed switching power stages with sensitive analog current sensing and complex control logic, all while managing the extreme $dv/dt$ and $di/dt$ transients associated with wide-bandgap (WBG) semiconductors like Gallium Nitride (GaN) and Silicon Carbide (SiC) [4], [5]. Unlike digital design, where Boolean logic can be abstracted away from silicon layout until later stages, PE circuits operate in a continuous-time regime where signal integrity is tightly coupled to physical device placement [6]. A seemingly minor change in trace geometry can introduce parasitic inductances that lead to switch-node oscillations, increased EMI, or even catastrophic failure due to noise-induced false turn-on [7], [8]. Hence, the traditional Electronic Design Automation (EDA) suites are architected for human-in-the-loop interaction rather than autonomous orchestration [9]. While command-line interfaces and scripting backends provided by tools like LTspice, KiCad, and OrCAD facilitate programmatic manipulation of primitives, they remain fundamentally imperative. These low-level application programming interfaces (APIs) fail to bridge the stochastic gap between a high-level functional specification (e.g., `Design a 1kW GaN-based VFD`) and a verified netlist, as they necessitate extensive manual coding to translate abstract intent into deterministic circuit specifics.

Generative Artificial Intelligence (AI) offers a transformative paradigm for breaking these bottlenecks. Large Language Models (LLMs) have demonstrated the ability to parse natural-language specifications and generate circuit descriptions, effectively serving as high-level design assistants [9]. Lin et al. [10] developed a chatbot, 'PE-GPT', for assisting users in designing power electronic systems. However, current generative models face severe domain-specific barriers. LLMs are prone to hallucinations, often suggesting nonexistent components or invalid pinouts [11]. PE-GPT [10] leveraged a knowledge base using retrieval augmented generation (RAG) to prevent hallucinations. Moreover, they lack understanding of electrical and electronic engineering domains, which is essential for meeting constraints such as creepage, clearance, and thermal limits. While stand-alone AI can propose creative solutions, it cannot guarantee the validity required for fabrication-ready hardware [12].

Recent literature has focused on solutions for the sub-tasks of circuit design [13]. *AnalogCoder* [12] utilized LLMs for training-free Python code generation to produce SPICE netlists, while *AnalogXpert* [14] introduced Eulerian-path sequence representations for topology discovery. Circuit-AI op-

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timized the bill of materials (BoM) and ran circuit simulations using LTspice and MATLAB [15]. Frameworks like *SPICEPilot* [16] have explored AI-guided SPICE code generation and simulation management. *AnalogGenie* [17] attempted to address the issue of data scarcity by generating topologies of analog circuits. Despite these advances, a significant gap remains: none of these systems orchestrate the end-to-end design flow from natural language directly to a physically verified, DRC-clean PCB package.

This paper presents a novel autonomous agentic framework that bridges this gap. Our work explores the research question: `Can an LLM generate functionally complete circuit artifacts from abstract user queries?`. The major contributions of this work are as follows:

- **Autonomous agentic workflow:** A multi-agent iterative circuit design framework is created to ensure functional validity across the netlists, schematic, and PCB.
- **Validation**: We illustrate the utility of the multi-agent framework with a `3 phase VFD for 1.5kW, 400VAC motor with a braking chopper`.

The paper is organized as follows. Section II revisits the current practice in circuit design with EDA tools. The proposed methodology is presented in Section III. Section IV presents a case study that demonstrates the detailed specification, selected components, and generated schematic and PCB for a given user prompt. The success and the scope of improvement are discussed in Section V. Finally, Section VI concludes our work.

## II. Circuit Design Workflow

The design life cycle of the PE converter for a motor drive begins well before engaging EDA software, initiating with a rigorous problem specification and component selection phase. The engineer first defines critical system parameters, such as input/output voltage levels, power levels, overload capabilities, and ambient temperature constraints, which directly dictate the topology (e.g., AC-DC-AC structures for variable frequency drives) and thermal management strategies. Based on the required switching and fundamental frequencies and critical system parameters, the designer selects the semiconductor technology, choosing between silicon (Si), SiC, or GaN devices to balance efficiency against cost [2], [5], [18]. This selection process, often conducted through distributor databases, prioritizes high power density and cost-effectiveness while adhering to safety margins for voltage and current. Crucially, engineers must synthesize information from component application notes to determine the necessary external circuitry and layout recommendations, ensuring that the selected devices function reliably within their specified operating areas.

Following the selection phase, the logical circuit definition is executed within the schematic capture environment of the EDA tool [19]. Components are instantiated from verified libraries, and electrical connectivity is established to reflect the chosen topology. At this stage, the designer integrates regulatory constraints directly into the logical design by defining specific net classes for various system voltages, user potential voltage, and earth ground voltage. This practice ensures that safety standards, such as IEC-defined creepage and clearance distances, are codified early in the design process to guide the subsequent physical layout. Circuit integrity is then validated using an electrical rules check (ERC) to identify logical disconnects.

The transition to the physical Printed Circuit Board (PCB) layout creates a complex optimization problem involving mechanical, thermal, and electrical constraints [6], [20]. The process begins with defining the board stackup and boundary geometry, often requiring an iterative approach to balance board size against the copper area required for high-current traces and mechanical constraints. Component placement is a critical step where the designer manually positions switching devices to minimize commutation loop areas, thereby reducing parasitic inductance and radiated electromagnetic interference (EMI) [21], [22]. Routing involves the meticulous separation of sensitive signal planes from noisy power planes to prevent coupling issues [20], [23]. The workflow concludes with a comprehensive design rules check (DRC) and 3D mechanical inspection, generating the necessary Gerber files and Bill of Materials (BOM) for fabrication only after all geometric and electrical conflicts are resolved.

Despite the automation provided by modern EDA tools, the design's effectiveness ultimately relies on engineering judgment and heuristic decision-making throughout the workflow. In the specification phase, the human being is essential for evaluating non-linear trade-offs between component cost, switching losses, and thermal complexity [11]. During the physical layout phase, the engineer's understanding of electromagnetic fields is indispensable. Tasks such as interpreting application notes to optimize gate driver placement [24] or implementing bootstrapping techniques in the gate driver for cost-effective operation heavily depend on domain expertise. Furthermore, the verification stage requires human oversight to interpret DRC violations, distinguishing between critical manufacturing errors and acceptable design intentionalities. Ultimately, the EDA tool serves as a precision instrument, but the design quality is determined by the engineer's ability to navigate the intersection of theoretical physics, safety standards, and practical manufacturability.

## III. Proposed Methodology

The proposed methodology is driven by harnessing the intelligence of AI agents to serve as surrogates to human intelligence and decision-making. An AI agent is essentially an autonomous system that perceives its environment, reasons through complex problems, and uses external tools to execute actions toward achieving a specific goal without continuous human intervention. For instance, the component selection agent (see Section III-B) accepts the device specifications, searches the component database (analogous to DigiKey or Mouser) for relevant components, and returns a bill of materials (BOM). The proposed framework leverages an agentic approach, where agents handle human tasks at each phase

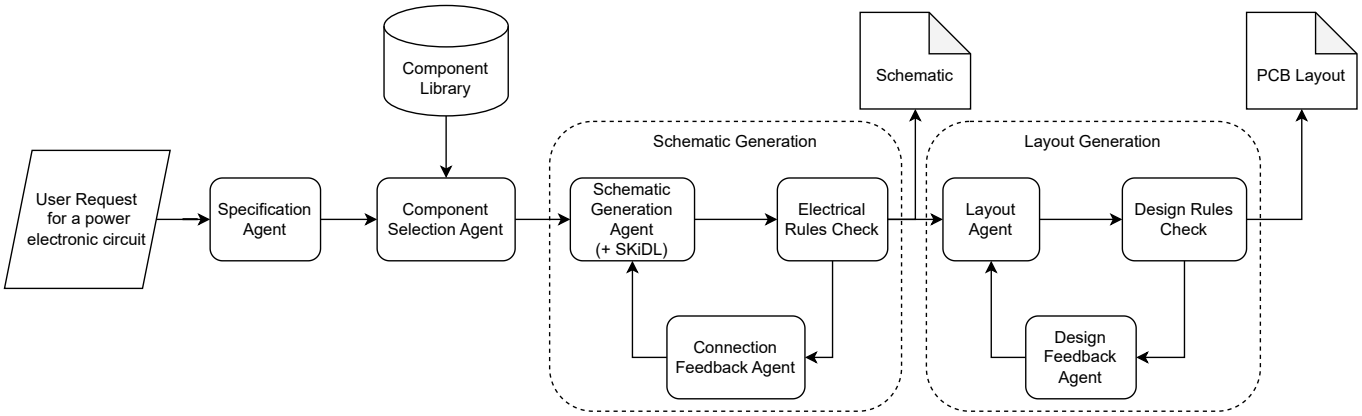


Fig. 1. An agentic circuit design pipeline with each agent serving as a surrogate for humane tasks

of circuit design, as shown in Fig. 1. We do not fine-tune any LLM. We use a plug-and-play approach with off-the-shelf models rather than fine-tuning, enabling instant upgrades to the underlying LLMs without the resource-intensive need to fine-tune them for power electronics applications. Our methodology relies on the synergy of agents to perform human tasks, with EDA tools for functional tasks.

### A. Specification Agent

To bridge the stochastic gap between natural language and engineering rigor, the specification agent translates the high-level user prompts into a structured deterministic parameter space. This agent is injected with an expert persona and the target application to extract critical parameters that dictate topology and device selection. The normalized schema explicitly captures the *Switching Frequency* ($f_{sw}$) to determine the viability of Silicon IGBTs versus SiC/GaN MOSFETs. It defines *Overload Capacity* and *Ambient Temperature* ($T_{amb}$), which are mathematically mapped to required current safety margins. Input constraints are parsed to distinguish between grid-tied AC inputs (requiring rectification) and DC sources, while output requirements define the modulation strategy (e.g., SPWM, SVPWM) and voltage levels. Crucially, the agent infers implicit system requirements, such as the necessity of a braking chopper for high-inertia motor loads or specific galvanic isolation barriers based on voltage class. This structured schema serves as the immutable contract for the downstream synthesis agents.

### B. Agentic Component Selection

A dedicated agent functions as a virtual procurement engineer, querying component databases (analogous to DigiKey or Mouser) based on relevance. The agent validates component ratings against the operating point, ensuring that the breakdown voltages ($V_{ds}$) and continuous current ratings ($I_d$) satisfy the defined voltage, overload, and thermal de-rating factors.

### C. Schematic Generation

*1) Schematic Generation Agent:* Following component selection, a Synthesis Agent generates the connectivity logic using the SKiDL Python library [25], effectively writing code to define the circuit netlist. To prevent the floating net hallucinations common in LLMs [12], [14], this agent enforces that every non-passive pin terminates at a named net or an explicit 'No-Connect' flag. This code-first approach allows for modular reuse; identical inverter legs are instantiated via loops rather than manual copy-pasting, ensuring symmetry and reducing the risk of logical errors.

*2) Verification and Correction (ERC):* Once the SKiDL script is generated, it is compiled into a netlist, and a deterministic Electrical Rules Check (ERC) is executed. This step is critical, as LLM-generated circuits often contain subtle connectivity violations that do not cause syntax errors but might result in non-functional hardware. Common errors detected at this stage include:

- Floating pins and unconnected nets: High-impedance inputs and named nets left unconnected. If those pins are essential for hardware operation, it could result in non-functionality.
- Pin Type Conflicts: Incompatible connections (e.g., *Output* connected to *Output*) or *Power Input* pins not driven by a defined source (missing *Power Flag*), which impede valid netlist generation.

Upon detecting errors, the system triggers the *connection feedback agent*. Instead of random regeneration of the circuit, this agent parses the raw ERC log file. It correlates the error code (e.g., `Pin not driven`) with the specific line number in the SKiDL script. Acting as a design reviewer, the feedback agent generates a corrective prompt explaining the violation logic (e.g., `the VCC pin on U1 is defined as a Power Input but is connected to a passive net; insert a PowerFlag to validate the source`). This structured feedback is passed back to the schematic generation agent, which revises the code. This loop continues iteratively until the design creates a netlist with zero ERC violations.

### D. Layout Generation

*1) Layout Agent:* The transition from netlist to PCB layout is managed by the layout agent, which handles board dimensioning, component placement, and routing. The agent generates a placement script that manipulates the PCB coordinate system directly. Following placement, an automated routing engine is invoked.

*2) Verification and Correction (DRC):* The final and most critical stage is the deterministic Design Rules Check (DRC), which validates the board against manufacturing constraints. Typical errors identified in this phase include:

- Clearance Violations: Copper features placed closer than the minimum dielectric spacing allows (e.g., between high-side and low-side gate signals).
- Courtyard Overlaps: Physical component bodies intersecting due to dense placement.
- Unrouted Nets: Net antennas that the auto router failed to resolve due to congestion.

When the DRC engine flags violations, the reports are fed to the *design feedback agent*. This agent translates coordinate-based error logs into semantic instructions to address the spatial issues identified by the layout agent. This cycle of placement modification and DRC validation repeats until the design is clean, at which point the system exports the Gerber files and drill maps for fabrication.

## IV. Case Study: 3-Phase Converter for Motor Drive Applications

To evaluate the framework's capability to handle power-specific topologies, the system was tasked with designing a `3 phase VFD for 1.5kW, 400VAC motor with a braking chopper`. The input specification requires high-voltage components to achieve a design compatible with the 400V AC motor and the applicable power rating. The detailed technical specification offered by the specification agent is included in Table I.

### A. Component Selection and Circuit Topology

As illustrated in the generated schematic (Fig. 2), the component selection agent opted for a discrete implementation rather than an integrated power module. The selected components are listed in Table II. Our component library is based on KiCAD9 [19]. The input rectification stage is constructed from discrete high-voltage diodes (D1 - D6) arranged in a bridge configuration to rectify the AC mains. For the DC link, the agent selected two large electrolytic capacitors (C1 and C2) connected in series. This topology is consistent with standard practices for 400V AC inputs (approx. 540-565V DC bus), allowing the use of 400-450V rated capacitors to support the total bus voltage.

The inverter stage comprises six discrete IGBTs (Q1–Q7) in TO-247 packages. A prominent feature of the synthesized design is the inclusion of a large wire-wound resistor (R7, 100Ω 2kW) and an associated control switch, indicating the agent successfully inferred the need for a dynamic braking capability to manage regenerative energy.

TABLE I
Technical Specifications of the VFD System

| Parameter (Symbol) | Specification / Constraint |
|---|---|
| ***System Ratings*** | |
| Nominal Power ($P_{\text{nom}}$) | $1.5\,\text{kW}$ |
| Overload Capacity ($I_{\text{OL}}$) | $115\%$ for $60\,\text{s}$ and $125\%$ for $3\,\text{s}$ |
| Max. Ambient Temperature ($T_{\text{amb}}$) | $+40^{\circ}\text{C}$ |
| Cooling Method | Forced Air Convection |
| Input Stage | AC |
| ***Input Interface*** | |
| Grid Voltage ($V_{\text{grid}}$) | $400\,\text{V}_{\text{rms}} \pm 10\%$ ($3\phi$) |
| Grid Frequency ($f_{\text{grid}}$) | $50\,\text{Hz}$ |
| Rectifier Topology | 6-Pulse Diode Bridge |
| ***DC Link Characteristics*** | |
| Nominal Bus Voltage ($V_{\text{DC}}$) | $540 - 565\,\text{V}_{\text{DC}}$ |
| Voltage Ripple ($\Delta V_{\text{DC}}$) | $< 3\%$ of $V_{\text{DC}}$ |
| Braking Threshold ($V_{\text{brk}}$) | $680\,\text{V}_{\text{DC}}$ |
| ***Inverter Stage*** | |
| Semiconductor Type | Silicon IGBT (1200 V Class) |
| Switching Frequency ($f_{\text{sw}}$) | $8.0\,\text{kHz}$ (SVPWM) |
| Peak Current ($I_{\text{pk}}$) | $\geq 4.0\,\text{A}$ |
| Deadtime ($t_{\text{dt}}$) | $2.0\,\mu\text{s}$ |

### B. Physical Layout Realization

The *Layout Agent* produced the printed circuit board shown in Fig. 3. The high-current path flows from the input rectifier diodes at the center, through the DC link capacitors (bottom left), and into the IGBT inverter bridge (top side).

## V. Results and Discussion

The generated hardware artifacts demonstrate the framework's ability to autonomously traverse the stochastic gap from abstract intent to concrete geometry. However, expert review of the generated PCB revealed specific strengths and critical domain-specific limitations.

### A. Connectivity and Logical Validity in Schematics

The primary success of this experiment is the complete logical integrity of the design. As evidenced by the schematic, the agent correctly synthesized a standard VFD topology. The feedback loops described in the methodology successfully prevented common LLM hallucinations, such as unconnected nets or mismatched pin counts. However, anti-parallel diodes across the IGBTs, decoupling capacitors for reduced commutation loop inductance should be added for a complete design of the power stage in the converter. A clear distinction of the power and gate components is a limitation in the generated schematic.

### B. Layout Quality and Power Integrity

The PCB passed 100% connectivity checks, meaning every logical node in the schematic has a corresponding physical path on the board. While the board is electrically continuous, the physical layout exhibits characteristics typical of constraint-driven auto routers (e.g., Free Routing) rather than expert human design.

- **Component Placement and Routing:** The layout does not clearly demarcate the power stage from the control

TABLE II
COMPLETE BILL OF MATERIALS AND COMPONENT SPECIFICATIONS

| Ref. Des. | Qty. | Component | Value / Specification | Package / Footprint |
|---|---|---|---|---|
| ***Power Semiconductors*** | | | | |
| Q1 – Q7 | 7 | IGBT (N-Ch) | 1200 V, 25 A, $V_{CE(sat)} < 2.0$ V | TO-247-3 (Vertical) |
| D1 – D6 | 6 | HV Rectifier | 1600 V, 10 A, Standard Recovery | DO-201AD (Axial) |
| ***Capacitors*** | | | | |
| C1, C2 | 2 | Electrolytic | 470 $\mu$F, 450 V, 105°C Snap-in | Radial D18.0mm P7.50mm |
| C3 | 1 | Film (MKP) | 1.0 $\mu$F, 1000 $V_{DC}$ (Snubber) | Rect. L10.0mm (MKS4) |
| C4 | 1 | Ceramic (X7R) | 10 nF, 50 V | SMD 0603 (1608 Metric) |
| ***Resistors*** | | | | |
| R1, R2 | 2 | Thick Film | 220 kΩ, 0.5 W, High Voltage | SMD 1206 (3216 Metric) |
| R3 – R5 | 3 | Thick Film | 1.0 MΩ, 0.25 W | SMD 1206 (3216 Metric) |
| R6 | 1 | Thick Film | 10 kΩ, 0.1 W, 1% Precision | SMD 1206 (3216 Metric) |
| R7 | 1 | Wirewound | 100 Ω, 2 kW (Braking Pulse) | Axial Power L25.0mm |
| R8 – R14 | 7 | Thick Film | 10 Ω, 0.1 W (Gate Series) | SMD 0603 (1608 Metric) |
| R15 – R21 | 7 | Thick Film | 10 kΩ, 0.1 W (Gate Pull-down) | SMD 0603 (1608 Metric) |
| ***Connectors*** | | | | |
| J1, J2 | 2 | Screw Terminal | 4-Pos, 5.08 mm Pitch, 24 A | Phoenix MKDS-1,5-4 |
| J4 | 1 | Screw Terminal | 2-Pos, 5.08 mm Pitch, 24 A | Phoenix MKDS-1,5-2 |
| J3 | 1 | Pin Header | 12-Pos, 2.54 mm Pitch | Vertical Header 1x12 |

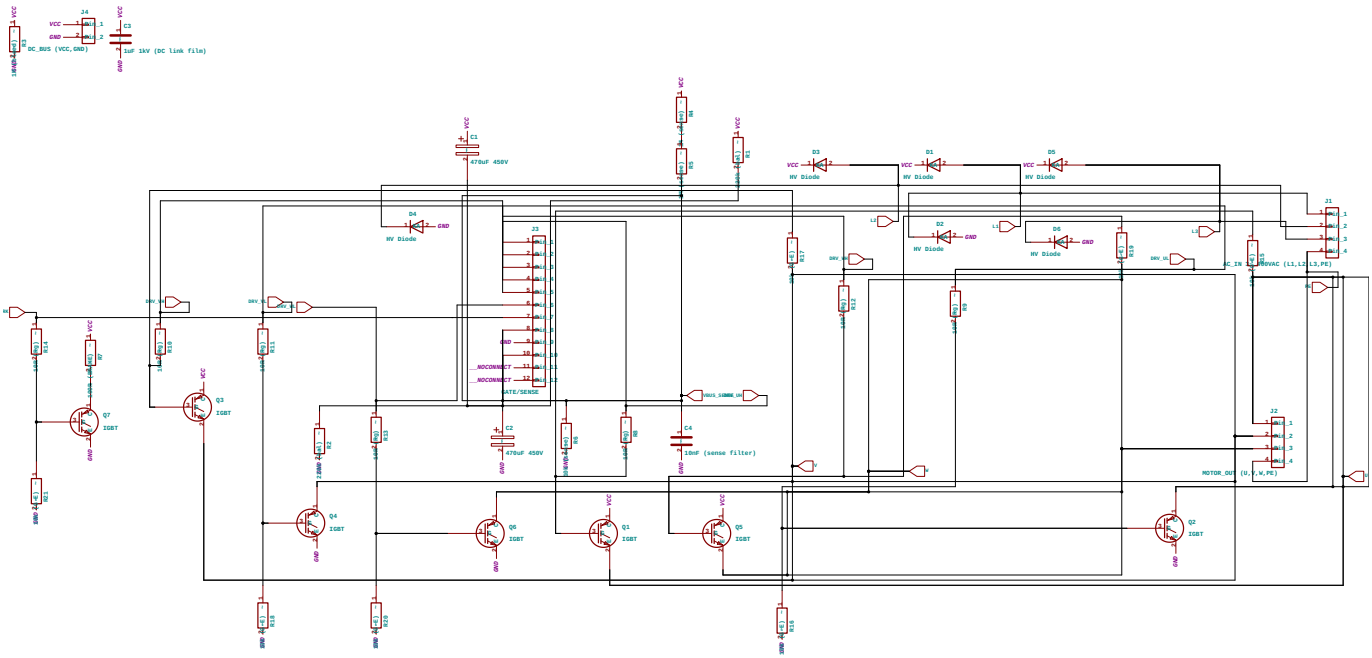

Fig. 2. Detailed schematic of the multi-phase power conversion stage, illustrating the integration of power switching devices in the rectifier and inverter stage and braking circuitry.

signals. The connections utilize equal trace widths. The optimal trace width and layout constraints are not implemented effectively. The TO-247 devices are arranged in a dense cluster without explicitly allocating the clearance for the heatsink. While the footprint was respected, the thermal volume required for proper airflow or heatsink attachment was not accounted for by the layout agent.

- **Commutation Loop Inductance:** The placement of the DC link capacitors (C1, C2) relative to the furthest inverter legs (e.g., Q1, Q2) creates a significantly large physical loop area. In hard-switching applications, this parasitic inductance ($L_\sigma$) will induce substantial voltage overshoots ($V_{peak} = V_{DC} + L_\sigma \frac{di}{dt}$) across the switches, potentially necessitating aggressive snubber circuits that are not present currently. $V_{peak}$ is the maximum voltage stress across the switches.
- **Creepage and Clearance:** The layout agent fails to strictly adhere to the creepage and clearance requirements.

Future work will ensure the proper implementation of the

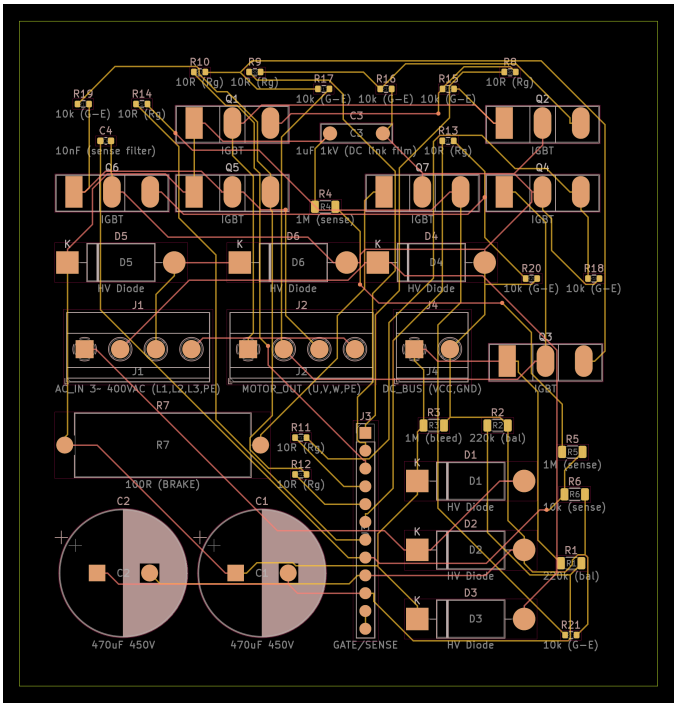


Fig. 3. PCB layout for the 3-phase inverter demonstrating the spatial partitioning between the high-voltage power stage (C1, C2, R16, Q1–Q7) and low-voltage control signals

integrated physics-based cost functions (e.g., minimizing loop area, creepage, and clearance) in the layout agent's feedback mechanism to elevate the design from being connected to being compliant.

## VI. Conclusion

This work introduces and validates an autonomous, agentic framework capable of translating natural language prompts into physically verifiable power electronic hardware. By avoiding fine-tuning in favor of a retrieval-augmented, multi-agent architecture, we successfully demonstrated a workflow that immunizes the design process against common LLM hallucinations, such as floating nets and non-existent components. The orchestration of SKiDL scripting and containerized EDA tools enabled the seamless generation of a 3-phase input-to-3-phase output schematic and PCB layout for a VFD application.

However, the results highlight a significant dichotomy between logical validity and physical performance. While the framework navigated the component selection and connectivity requirements, the agent was unable to distinguish between power and gate signals. The physical layout of the DRC-clean PCB exhibited limitations characteristic of constraint-driven auto routers. Specifically, the lack of physics-aware placement logic resulted in suboptimal commutation loop areas and gate signal routing and in noncompliance with clearance and creepage requirements. Such artifacts could introduce detrimental parasitic inductances, EMI issues, and inoperable hardware in practical high-switching-frequency operation.

Future research will focus on elevating the system from generating connected designs to compliant designs and ensuring complete component selection. This involves improving the integration of physics-based cost functions, specifically targeting power transfer and loop inductance, directly into the layout agent's feedback mechanism. It would also improve schematic readability and ensure complete component selection. Ultimately, this work establishes a foundational step toward a fully autonomous design assistant that not only automates the manual tedium of schematic capture but also assists in the complex optimization inherent to modern power electronics.

## References


[1] M. Bruha, K. Pietiläinen, and A. Rauber, "High speed electrical drives–perspective of vfd manufacturer," in *E3S Web of Conferences*, vol. 178. EDP Sciences, 2020, p. 01006.

[2] A. H. Mohamed, H. Vansompel, and P. Sergeant, "Electrothermal design of a discrete gan-based converter for integrated modular motor drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 5, pp. 5390–5406, 2021.

[3] M. M. Swamy, J.-K. Kang, and K. Shirabe, "Power loss, system efficiency, and leakage current comparison between si igbt vfd and sic fet vfd with various filtering options," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 3858–3866, 2015.

[4] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide bandgap devices in ac electric drives: Opportunities and challenges," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 3–20, 2019.

[5] F. Baskurt, K. Boynov, and E. Lomonova, "The half-bridge sic-mosfet switching cell: implementation in a three phase motor drive," in *8th IEEE Young Researchers Symposium in Electrical Power Engineering (YRS 2016)*, 2017.

[6] N. Lourenço, R. Martins, and N. Horta, "Layout-aware sizing of analog ics using floorplan & routing estimates for parasitic extraction," in *2015 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2015, pp. 1156–1161.

[7] D. J. Rogers and P. Lakshmanan, "Low-inductance snubber arrays for high-power, high-bandwidth switch-mode amplifiers," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2015, pp. 2557–2564.

[8] B. Zhang and S. Wang, "A survey of emi research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, 2020.

[9] J. Pan, G. Zhou, C.-C. Chang, I. Jacobson, J. Hu, and Y. Chen, "A survey of research in large language models for electronic design automation," *ACM Transactions on Design Automation of Electronic Systems*, vol. 30, no. 3, pp. 1–21, 2025.

[10] F. Lin, X. Li, W. Lei, J. J. Rodriguez-Andina, J. M. Guerrero, C. Wen, X. Zhang, and H. Ma, "Pe-gpt: A new paradigm for power electronics design," *IEEE Transactions on Industrial Electronics*, 2024.

[11] K. Xu, R. Qiu, Z. Zhao, G. L. Zhang, U. Schlichtmann, and B. Li, "Llm-aided efficient hardware design automation," *arXiv preprint arXiv:2410.18582*, 2024.

[12] Y. Lai, S. Lee, G. Chen, S. Poddar, M. Hu, D. Z. Pan, and P. Luo, "Analogcoder: Analog circuit design via training-free code generation," in *Proceedings of the AAAI Conference on Artificial Intelligence*, vol. 39, no. 1, 2025, pp. 379–387.

[13] H. Chae, S. Kim, S. Poddar, X. Gao, S. Li, and D. Z. Pan, "Towards generative ai for analog and rf ic design: From spec to layout," in *2025 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. IEEE, 2025, pp. 1–9.

[14] H. Zhang, S. Sun, Y. Lin, R. Wang, and J. Bian, "Analogxpert: Automating analog topology synthesis by incorporating circuit design expertise into large language models," in *2025 International Symposium of Electronics Design Automation (ISEDA)*. IEEE, 2025, pp. 772–777.

[15] V. Raval, M. Zeid, and P. Enjeti, "Circuit-ai: An advanced large language model (llm) based ai-agent for bill of materials (bom) optimization, circuit simulations & design," in *2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE)*. IEEE, 2025, pp. 1–7.

[16] D. Vungarala, S. Alam, A. Ghosh, and S. Angizi, "Spicepilot: Navigating spice code generation and simulation with ai guidance," in *2024 IEEE International Conference on Rebooting Computing (ICRC)*. IEEE, 2024, pp. 1–6.

[17] J. Gao, W. Cao, J. Yang, and X. Zhang, "Analoggenie: A generative engine for automatic discovery of analog circuit topologies," *arXiv preprint arXiv:2503.00205*, 2025.

[18] K. Lee and M. M. Swamy, "Quantitative evaluation between si-igbt and sic-mosfet based adjustable speed drive systems with long cables," in *2025 IEEE Energy Conversion Conference Congress and Exposition (ECCE)*, 2025, pp. 1–8.

[19] KiCad Development Team, "Kicad EDA: Open source electronic design automation software," 2026, open-source EDA suite originally developed by Jean-Pierre Charras. Accessed: 2026-02-05. [Online]. Available: https://www.kicad.org/

[20] V. Anand, V. Singh, and V. K. Ladwal, "Study on pcb designing problems and their solutions," in *2019 International Conference on Power Electronics, Control and Automation (ICPECA)*, 2019, pp. 1–5.

[21] V. Baker, B. Fan, R. Burgos, V. Blasko, and W. Chen, "3d commutation-loop design methodology for a silicon-carbide based 15 kw, 380: 480 v matrix converter with pcb aluminum nitride cooling inlay," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2020, pp. 233–238.

[22] Q. Le, T. Evans, Y. Peng, and H. A. Mantooth, "Peec method and hierarchical approach towards 3d multichip power module (mcpm) layout optimization," in *2019 IEEE International Workshop on Integrated Power Packaging (IWIPP)*. IEEE, 2019, pp. 131–136.

[23] G. Ala, G. Giglia, E. Francomano, M. Di Piazza, M. Luna, and G. Conte, "Design of emi filters using multi-objective optimization," in *2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe)*. IEEE, 2018, pp. 1–5.

[24] B. Mondal and B. A. Karuppaswamy, "Design of si-igbt gate driver for inverter applications," in *2021 IEEE 12th Energy Conversion Congress & Exposition-Asia (ECCE-Asia)*. IEEE, 2021, pp. 743–748.

[25] D. Vandenbout and Xess Corp., "Skidl: Design electronic circuits using python," https://github.com/devbisme/skidl, 2025, accessed: 2026-02-05.