Physical Dilemma of Large-Area Advanced-Node Chips: Irreversible Narrowing of Interconnect Channels

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Abstract

Under the current physical laws, there are only two pathways to improve chip computing power: first, scaling down the process to increase transistor density, and second, directly expanding the chip area. Both approaches are constrained by geometric boundaries and fundamental physical laws, and have approached their limits at advanced technology nodes. Starting from geometry, quantum mechanics, thermodynamics, and statistical physics, this paper systematically demonstrates the device-level physical bottlenecks of advanced-node single chips, including quantum tunneling, voltage scaling failure, and uncontrolled statistical fluctuations. It points out the exponential yield degradation of large-area chips and reveals that Chiplet and advanced packaging only

shift costs rather than eliminate fundamental contradictions caused by interconnect narrowing, such as drastic resistance increase, thermal runaway, signal crosstalk, and thermomechanical reliability failure. Results show that advanced-node chips cannot achieve large-area integration while maintaining acceptable signal integrity and heat dissipation capability. Based on physical constraints, this paper proposes the only feasible solution: mature-node Chiplet, which reduces interconnect pressure through low transistor density and implements system integration with traditional packaging, returning to a physically self-consistent design paradigm.

Keywords

Advanced Node; Interconnect Channel; Narrowing Effect; Resistance; Thermal Dissipation; Chiplet; Mature Process; Physical Limit

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Introduction

The improvement of chip computing power is strictly limited by two-dimensional geometric constraints: the total number of transistors on a chip equals the product of chip area and transistor density per unit area. Thus, there are only two ways to enhance computing power: scaling transistor feature size to increase density (Moore’s Law path) and enlarging the physical chip area (area-driven path). For decades, the semiconductor industry has evolved along the former path, pushing

technology nodes toward the atomic scale. However, as feature sizes enter the deep-nanometer regime, constraints from physical laws have changed from manageable to insurmountable, and both pathways have reached dead ends.

Most existing studies focus on new materials, structures, and packaging to sustain process scaling, but generally avoid a core fact: the irreversible narrowing of interconnect channels inherent to advanced nodes has evolved from a performance bottleneck to a physical dead end. Based on fundamental physical laws, this paper decomposes the systematic dilemmas of advanced-node chips in devices, interconnection, yield, heat dissipation, and reliability. It proves that schemes such as 2.5D/3D packaging and Chiplet cannot resolve underlying contradictions, and finally provides a technically feasible route consistent with physical laws.

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1 Only Two Paths for Performance Improvement: Geometric Constraints

A chip is a two-dimensional physical entity, and its computing capacity is determined by the total number of transistors it can hold, following the basic geometric relation:

$$Total\,Transistors = Chip\ Area \times Transistor\ Density\ per\ Unit\ Area$$

Within the current physical framework, no third path exists for improving computing power. Architecture innovation, advanced packaging, heterogeneous integration, and other techniques are only combinations or compromises of the two paths and cannot break the two-dimensional geometric constraint.

Path 1: Process Scaling: Increasing density by continuously shrinking transistor size, the core of Moore's Law [1].
Path 2: Chip Area Expansion: Accommodating more transistors with larger physical dimensions while keeping density unchanged.

This paper proves that under advanced nodes, Path 1 is limited by interconnect narrowing, resistance, power consumption, and thermal effects; Path 2 is restricted by exponential yield degradation; advanced packaging and Chiplet only shift internal contradictions to the packaging interface without eliminating physical conflicts.

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2 Device-Level Physical Bottlenecks of Advanced-Node Single Chips

Apart from interconnect bottlenecks, advanced-node transistors

themselves have hit boundaries defined by three physical laws, forming unbreakable hard constraints.

2.1 Quantum Tunneling Effect

When transistor channel length approaches the atomic scale, electrons can cross potential barriers directly via quantum tunneling, making complete device turn-off impossible. Leakage current increases exponentially with size reduction. This effect originates from fundamental quantum mechanics and cannot be eliminated by material optimization or process improvement.

2.2 Dennard Scaling Failure and Power Boundary

Dennard scaling once supported the paradigm of "size reduction, proportional voltage drop, and constant power density" [2]. However, threshold voltage cannot be reduced infinitely due to thermodynamic limits, terminating voltage scaling prematurely. As density continues to double, power density doubles accordingly, eventually triggering thermal runaway.

2.3 Uncontrolled Statistical Fluctuation

When the number of dopant atoms in the channel drops to a few dozen, random fluctuations cause significant variation in threshold voltage among transistors. The slowest devices limit operating frequency, while the fastest accelerate self-heating and aging, resulting in uncontrolled yield and reliability at the atomic scale.

Quantum mechanics, thermodynamics, and statistical physics independently conclude that the path relying solely on process scaling is physically unsustainable.

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3 Yield Catastrophe of Large-Area Chips

Direct fabrication of large-area advanced-node chips leads to exponential yield degradation. In semiconductor manufacturing, defect density per unit area is approximately constant, and chip yield decreases exponentially with increasing area [5]. Doubling chip area does not merely halve yield but drives it into an unacceptable range rapidly, causing cost runaway and commercial infeasibility. Even if physically producible, such chips are economically unviable [8].

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4 Intrinsic Conflict Between Chiplet and Advanced Nodes

To avoid the yield trap of monolithic large chips, the industry adopts the Chiplet architecture: splitting functions into multiple small dies assembled into a complete system via advanced packaging [6]. This scheme does not eliminate contradictions but transfers the on-chip interconnect bottleneck to the inter-die interface.

Transistor density of advanced nodes is orders of magnitude higher than that of mature nodes. For the same chip area, the number of signals and I/O channels increases drastically. However, the physical perimeter of the chip is fixed, forcing all external channels into a limited edge length and causing continuous interconnect narrowing, triggering a series of physical disasters.

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5 Systematic Failure Caused by Interconnect Channel Narrowing

5.1 Mandatory Constraint of Ultra-High Alignment Accuracy

To accommodate massive channels within a limited interface, line width and spacing must shrink to the nanometer scale, forcing packaging

processes to meet sub-micron alignment accuracy. Misalignment directly leads to sharp increases in contact resistance, signal attenuation, and crosstalk. High precision is not an optional technical choice but a mandatory physical constraint imposed by advanced-node narrowing.

5.2 Channel Narrowing and Drastic Resistance Increase

As channel count N surges within a fixed perimeter, channel width follows:

$$w \propto 1/N$$

Combined with the resistance law:

$$R = \rho L/(w \cdot t)$$

Reduced width increases resistance inversely. Meanwhile, electron surface scattering intensifies at nanoscale widths, further raising effective resistivity—overall resistance can increase by more than an order of magnitude [3].

5.3 Signal Attenuation and Repeater-Induced Thermal Runaway

High resistance causes severe RC delay and signal attenuation. Inserting repeaters is a traditional compensation method, but it is infeasible in

advanced nodes [4]:

1. Repeaters introduce additional power consumption and heat sources;
2. Power density of advanced nodes is inherently extremely high;
3. Massive channels lead to dense repeater distribution and local hotspots;
4. Higher temperature further increases leakage and power consumption, forming positive feedback and eventual thermal runaway.

5.4 Uncontrollable Signal Crosstalk

Narrowed channels reduce line spacing synchronously, sharply increasing coupling capacitance and mutual inductance between adjacent lines and raising crosstalk noise significantly. Suppressing crosstalk requires wider spacing or shielding lines, further compressing already crowded channel width and creating an unsolvable cycle [3].

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6 Advanced Packaging: Cost Shifting Instead of Conflict Resolution

6.1 Triple Dilemmas of 2.5D Packaging

1. Thermal Dissipation Degradation: Interposers and stacking block heat flow; high-power-density chips quickly hit the thermal limit and are

forced to throttle.

2. Cost Runaway: High-precision processes raise packaging cost to near wafer-processing cost, with marginal benefits approaching zero [8].

3. Thermomechanical Reliability Failure: Mismatched thermal expansion coefficients of different materials, local hotspots causing non-uniform expansion and warpage, accelerated fatigue failure of micro-bumps. Macroscopic temperature control cannot eliminate micron-scale temperature differences, so the failure mechanism cannot be eradicated [7].

6.2 Thermal Dead End of 3D Packaging

3D stacking attempts to bypass perimeter bottlenecks vertically, but heat from middle layers must conduct horizontally to edges for dissipation, with thermal resistance increasing significantly with distance. Under high power density of high-performance logic chips, core temperature quickly exceeds limits, making it only suitable for low-power memory devices.

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7 Conclusion and Physically Feasible Path

7.1 Conclusion

Advanced-node chips face an irreconcilable conflict between fixed

area/perimeter geometric constraints and the explosion of interconnect channels caused by soaring transistor density, leading to:

1. Irreversible narrowing of interconnects and exponential resistance rise [3];
2. Thermal runaway caused by repeater-based compensation [4];
3. Uncontrollable signal crosstalk [3];
4. 2.5D/3D packaging only shifts costs without solving physical conflicts [7];
5. Large-area chips are commercially unfeasible due to yield issues [5][8].

Advanced-node chips cannot achieve stable, high-performance large-area integration; all related schemes violate fundamental physical laws.

7.2 The Only Path Indicated by Physical Laws: Mature-Node Chiplet

Interconnect narrowing is a unique dilemma of advanced nodes. Mature-node chips have low transistor density, requiring fewer I/O channels per unit area, so channel width does not need to be compressed to the nanometer scale, offering natural advantages:

1. With sufficient line width and low resistance, repeaters can be safely inserted to extend transmission distance and expand chip area without causing thermal runaway [3][4];
2. Low power density eliminates significant hotspots and ensures high thermal reliability [7];
3. Low alignment accuracy requirements enable traditional packaging;
4. Chiplet architecture avoids yield pitfalls and is economically feasible [6][8].

Fabricating small dies with mature processes and integrating systems via traditional packaging does not pursue ultimate single-point density but system-level physical self-consistency. This is not technological retrogression but respect for physical laws—the only sustainable route in the post-Moore era.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," in IEEE Solid-State Circuits Society Newsletter, vol. 11, no. 3, pp. 33-35, Sept. 2006, doi: 10.1109/N-SSC.2006.4785860.
keywords: {Integrated

circuits;Computers;Silicon;Films;Heating;Microwave amplifiers;Data mining},

[2] R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," in IEEE Journal of Solid-State Circuits, vol. 9, no. 5, pp. 256-268, Oct. 1974, doi: 10.1109/JSSC.1974.1050511.
keywords: {Doping profiles;Semiconductor process modeling;Predictive models;Threshold voltage;Fabrication;Switching circuits;Digital integrated circuits;MOSFET circuits;Ion implantation;Length measurement},

[3] R. Brain, "Interconnect scaling: Challenges and opportunities," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2016, pp. 9.3.1-9.3.4, doi: 10.1109/IEDM.2016.7838381.
keywords: {Integrated circuit interconnections;Metals;Delays;Resistance;Transistors;Wires;Capacitance},

[4] P. Kapur, G. Chandra and K. C. Saraswat, "Power estimation in global interconnects and its reduction using a novel repeater optimization methodology," Proceedings 2002 Design Automation Conference (IEEE

Cat. No.02CH37324), New Orleans, LA, USA, 2002, pp. 461-466, doi: 10.1109/DAC.2002.1012669. keywords: {Repeaters;Integrated circuit interconnections;Power dissipation;Wires;Energy consumption;Delay;Computational Intelligence Society;Clocks;Permission;Optimization methods},

[5] C. H. Stapper, "On Murphy's yield integral (IC manufacture)," in IEEE Transactions on Semiconductor Manufacturing, vol. 4, no. 4, pp. 294-297, Nov. 1991, doi: 10.1109/66.97812.
keywords: {Gaussian distribution;Integrated circuit yield;Integrated circuit modeling;Integrated circuit manufacture;Semiconductor device manufacture;Yield estimation;Manufacturing industries;Statistical distributions;Manufacturing processes;Costs},

[6] S. Naffziger et al., "Pioneering Chiplet Technology and Design for the AMD EPYC™ and Ryzen™ Processor Families : Industrial Product," 2021 ACM/IEEE 48th Annual International Symposium on Computer Architecture (ISCA), Valencia, Spain, 2021, pp. 57-70, doi: 10.1109/ISCA52012.2021.00014. keywords: {Industries;Program processors;Computer architecture;Packaging;Routing;Silicon;System-on-chip;Chiplets;Moore's Law;Processors;Modular;Industry},

[7] H. Kim, J. Y. Hwang, S. E. Kim, Y. -C. Joo and H. Jang, "Thermomechanical Challenges of 2.5-D Packaging: A Review of Warpage and Interconnect Reliability," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 13, no. 10, pp. 1624-1641, Oct. 2023, doi: 10.1109/TCPMT.2023.3317383. keywords: {Packaging;Substrates;Silicon;Reliability;Three-dimensional displays;Thermomechanical processes;Temperature measurement;25-D packaging;board-level reliability;interposer;solder fatigue life;warpage},

[8] A. Mallik et al., "Economics of semiconductor scaling - a cost analysis for advanced technology node," 2019 Symposium on VLSI Technology, Kyoto, Japan, 2019, pp. T202-T203, doi: 10.23919/VLSIT.2019.8776521. keywords: {Computer architecture;Cost benefit analysis;Nanoscale devices;Microprocessors;Industries;Tools},