THE COUPLED NON-EQUILIBRIUM TRANSPORT WAVEGUIDE LAW

ARCHITECTURAL DESIGN RULES & FUNDAMENTAL SUBSTRATE SPECIFICATION

Inventor: **Nathan Allen** • Document Status: **Preprint Baseline (v1.0)** • Security Level: **Defensive Public Disclosure Window**

SOLE INVENTORSHIP & PRIORITY DECLARATION

All technical architectures, mathematical formulations, and material specifications contained herein were conceptualized and realized solely by the author. This document establishes an absolute defensive legal boundary regarding prior art and derivation law, freezing the priority timeline against subsequent trailing claims or administrative re-branding attempts under standard heterogeneous integration categories.

Abstract of the Disclosure

This specification outlines an invariant material-to-logic architectural law that decouples active logic shielding from passive environmental sensing operations across microelectronic semiconductor devices. Traditional carrier routing frameworks are bound by the classical Drude framework and Maxwellian electrodynamics, trapping high-frequency transient signals within an inescapable 1500-nanosecond relaxation lag envelope due to surface and lattice defect scattering. The Coupled Non-Equilibrium Transport Waveguide Law supersedes these limitations via quantum carrier confinement over a shared, selectively carved Scandium Tungstate negative thermal expansion foundation. Parallel Graphene-Copper (Gr-Cu) hybrid input and pre-biased ballistic conduction traces run side-by-side inside a dual-encapsulated hexagonal boron nitride (hBN) dielectric waveguide, achieving native propagation velocities equal to the Fermi velocity of the carrier ensemble (~1.0 million meters per second) with zero structural step-discontinuities.

1. Fundamental Substrate Mechanics & Structural Coordinates

The implementation of this parallel routing matrix over macroscopic distances without suffering carrier thermalization requires absolute potential invariance across the lateral transition boundaries. To resolve differing thickness profiles between neighboring domains, the shared Scandium Tungstate substrate foundation relies on a top-down vertical axis differential carving profile. The foundation base directly beneath the passive monitoring domain (Zone B) remains completely flat and unmodified. Conversely, the foundation base directly beneath the active channel domain (Zone A) features a top-down structural carve establishing a precise downward vertical offset.

This deep carve drops the active channel floor step to balance capacitive displacement currents and compensate for the ultra-thin total profile of the active transport layers (approximately 2.3 nm to 3.1 nm total). By lowering the stack floor of Zone A, the upper boundary interfaces of both operational domains are brought into a single, perfectly flush horizontal alignment plane prior to global topside passivation. This geometric alignment eliminates vertical phase steps and physical step-discontinuities, ensuring wave energy packets transition laterally across the pocket boundaries with zero impedance mismatch or localized field distortions.

2. Co-Planar Domain Profiles & Core Component Parameters

ZONE A: ACTIVE GFET CHANNEL DOMAIN PROFILE

> **SUBSTRATE CONFIGURATION**
>
> Deeply carved, downward vertical offset floor etched into the Scandium Tungstate base.

> **DIELECTRIC BED BASELINE**
>
> Localized primary hBN sub-layer blanket bed restricted to a strict 2 to 3 nanometer thickness window (6 to 9 atomic layers) nested exclusively within the carved floor.

> **ACTIVE CORE CHANNELS**
>
> Graphene-Copper (Gr-Cu) hybrid input and ballistic conduction traces. Standalone unlaminated 2D graphene monolayers are entirely omitted to prevent unconstrained wrinkling and delocalization.

> **CONTACT INTERFACES**
>
> Directional Nickel-Scandium (Ni-Sc) contact pads anchored straight to the exposed atomic edges of the Gr-Cu cores to establish a definitive Zero Schottky Barrier.

ZONE B: PASSIVE SENSING BIPOLAR DOMAIN PROFILE

> **SUBSTRATE CONFIGURATION**
>
> Direct positioning on the completely flat, unmodified Scandium Tungstate base plane.

> **CRYSTALLINE MEDIUM**
>
> Composition-graded Silicon-Germanium (SiGe) material sub-layer with a strict sub-10 nanometer vertical axis thickness ceiling. No graphene is deposited or transferred over these coordinates.

> **TOPOLOGICAL ARRAY LAYOUT**
>
> A distributed sequence of repeating 1.0-micron HBT nodes paired with 0.2-micron isolation gaps to align the structure natively with the material-defined mean free path.

> **NODE CONTACT PASSIVATION**
>
> Internal tracking junctions are hermetically sealed directly beneath the global topside hBN parallel cap to suppress parasitic edge-leakage paths.

3. Mathematical Derivations & Waveguide Transport Laws

ZERO-COLLISION TRANSPORT CRITERION

The structural mechanics and propagation dynamics of the waveguide are governed by the principles of non-equilibrium statistical mechanics. Laminating a high-mobility graphene surface skin layer natively onto the outer grain boundaries of the copper cores establishes a quantum waveguide channel where electrons behave as massless Dirac fermions. Because the continuous run of individual input trace segments is geometrically constrained to a sub-micron scale shorter than the electron-phonon scattering mean free path ($\lambda_{e\text{-}ph}$), traveling carriers move faster than the timeline required to undergo thermalization with the background crystal lattice. The statistical state of the carrier ensemble escapes local thermodynamic equilibrium, governed entirely by the collisionless Boltzmann Transport Equation:

$$\partial f/\partial t + (p/m^*)\bullet\nabla_r(f) + e(E + (p/(m^*\bullet c)) \times B)\bullet\nabla_p(f) = 0$$

For the distribution function to validate a true zero-collision transport state across room temperature operations (300 Kelvin), the physical length (L) of individual transport link blocks must satisfy the absolute architectural threshold:

$$L \leq \lambda_{e\text{-}ph} \leq 1.2\ \mu m$$

STRUCTURAL DYNAMIC CAPACITANCE CANCELLATION LAW

To counteract the legacy RC low-pass filter effect over wider trace routing scales, the 9-micron-wide input trace runs in strict horizontal parallel proximity to an actively pre-biased ballistic conduction trace. This layout forces mutual coupling capacitance to completely dominate the environment. The inter-trace mutual coupling capacitance per unit length ($C_{coupling}$) is explicitly computed as:

$$C_{coupling} = (\pi\bullet\varepsilon_{hBN}) / \ln(2d/w)$$

Where the spatial layout separation distance (d) is calibrated to exactly 50 microns to isolate inductive back-EMF spikes, and the line cross-section width (w) is locked to 9 microns. The total displacement current density (J_D) crossing the inter-trace boundary is defined by:

$$J_D = C_{coupling} \bullet [d(V_{input} - V_{ballistic}) / dt]$$

By applying an active, pre-biased, correlated electrical potential to the parallel ballistic conduction trace, the architecture enforces the continuous charging limit:

$$\lim_{(\Delta t \to 0)} [V_{input}(t + \Delta t) - V_{ballistic}(t)] / \Delta t = 0$$

This operational state suppresses the local displacement current density (J_D) to a net-zero field value, bypassing legacy substrate charging time constants and allowing analog wave edges to maintain a native propagation velocity equal to the Fermi velocity of the massless Dirac fermion ensemble (~1.0 million meters per second).

4. Chronometric Layering for Non-Security Sensing Integrations

Post heterojunction bipolar transistor uptake, where the signal wavefront energy profile has successfully transitioned through the composition-graded Silicon-Germanium (SiGe) HBT array nodes, the parallel waveguide configuration routes execution to a subsequent macro-scale chronometric layering matrix. This structural sub-matrix is specifically engineered for non-security type integrations, optimizing the co-planar layout for multi-spectral analytical extraction and disparate environmental sensing operations.

The chronometric layering matrix comprises a vertical stack of chronologically segmented delay lines structured natively over the substrate plane, separating incoming phase profile captures into clear, citable, time-correlated analytic channels. By delaying the processed signal profiles down distinct chronological paths post-bipolar uptake, the disparate sensing matrix executes cross-domain signal correlation to scan for external thermodynamic shifts, high-frequency electromagnetic noise spikes, and mechanical substrate deformations. Because these macro-environmental monitoring loops are isolated down chronometric pathways completely decoupled from primary logical execution, non-security analytical reporting runs concurrently without causing timing variations or parasitic charge crowding across the primary signal corridors.

5. Integrated Non-Monolayer Low-Pass Filter Windows

To enforce absolute deterministic signal propagation over long-scale ingestion paths, the total continuous run of the primary Graphene-Copper (Gr-Cu) input trace is geometrically constrained to a structural maximum length ceiling between 7.0 millimeters and 10.0 millimeters. Limiting the ingestion line to this macro-maximum caps the cumulative environmental phase degradation baseline, keeping propagation dynamics safely within the real-time processing capture envelope of the adjacent SiGe HBT matrix nodes.

Importantly, the integration configuration selectively bifurcates its structural layout rules based on domain operational profiles. Across the non-security type scientific architectures described in Section 4, the continuous run of the input trace retains its high-mobility graphene skin lamination uninterrupted up to the terminal boundary interface coordinates, enabling unfiltered multi-spectral analytical extraction and broadband sensing uptake post heterojunction bipolar transistor interception. Conversely, for hardware-level security applications, an inline low-pass filter window featuring a strict physical longitudinal dimension of exactly 5.0 microns is placed upstream from the waveguide interface. Within this 5.0-micron filter coordinate, the graphene skin lamination is entirely omitted, presenting a raw copper core segment that locally terminates non-equilibrium ballistic transport conditions to attenuate coherent Terahertz transients and block radiative data-harvesting vectors.

6. Cleanroom Manufacturing & Assembly Sequence

1. **Foundation Polish and Vacuum Bake:** A Scandium Tungstate negative thermal expansion base substrate is prepared, cleaned, and baked under high vacuum at 500 degrees Celsius to secure a net-zero moisture profile.
2. **Selective Deep Carving (Zone A Only):** While the substrate region under Zone B remains entirely flat and unmodified, a localized deep carve is dry-etched into the substrate surface directly over the Zone A coordinates, establishing a precise downward vertical axis offset.
3. **Passive HBT Array Epitaxy (Zone B):** Directly on the unmodified substrate base surface in Zone B, a composition-graded Silicon-Germanium (SiGe) material sub-layer is epitaxially grown and lithographically patterned as a distributed, multi-node topological array (1.0-μm HBT nodes paired with 0.2-μm isolation gaps), constraining the vertical thickness strictly to a sub-10 nanometer window.
4. **Localized Primary hBN Bed Assembly (Zone A Only):** Inside the deeply carved Zone A pocket, a primary hBN bed is grown via LPCVD (50 to 75 gas-pulse cycles at 450 to 520 degrees Celsius) to lock layer thickness to a strict 2 to 3 nanometer window. A selective dry etch restricts this layer exclusively to the carved Zone A floor.
5. **Gr-Cu Hybrid Interconnect Line Fabrication:** High-mobility Graphene-Copper (Gr-Cu) hybrid lines are lithographically defined and deposited onto the primary hBN bed to establish the input trace and the ballistic conduction trace, completely omitting standalone unlaminated 2D sheets and maintaining an exact 50-micron layout separation distance.
6. **Contact & Node Interconnect Lithography:** Anisotropic Reactive Ion Etching (RIE) slices contact windows to expose the Gr-Cu transport interfaces, where electron-beam evaporation deposits directional Nickel-Scandium (Ni-Sc) metal layers to form a Zero Schottky Barrier interface, while simultaneously evaporating active contact interfaces onto the Zone B HBT node terminals.
7. **Global Topside Atomic Sealing:** The entire parallel die is loaded into a PE-ALD loop operating at a low-temperature threshold of 150 degrees Celsius. The system executes exactly 75 automated gas-pulse cycles to grow a continuous topside hBN encapsulation layer to a strict thickness of 3 nanometers globally across the entire wafer. This completes the hBN-Gr/Cu-hBN dual-encapsulated quantum sandwich, hermetically sealing all underlying traces, contact pads, and active array contacts beneath a single, unbroken dielectric roof.