Fundamental Origin and Design Mitigation of Output-Capacitance Hysteresis in Vertical Charge-Balanced Power Devices

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Abstract

The output-capacitance hysteresis of charge-balanced vertical drift regions, commonly referred to as superjunctions, has attracted renewed attention because of its impact on switching losses in resonant and soft-switching power converters. Previous studies have linked this behaviour to stranded charge in the p/n semiconductor pillars and to the finite carrier velocity required for charge redistribution during voltage transients. In this work, the physical origin of this hysteresis is revisited by analysing the charge dynamics during charging and discharging. Finite-element simulations are used to assess the influence of charge-balance condition, temperature, partial dopant ionisation, cell pitch, voltage slew rate, and non-uniform doping, including graded pillar profiles. The results indicate that capacitance hysteresis is strongly governed by field-dependent carrier transport at the boundaries of the depletion regions, which controls the rate at which mobile carriers can be removed from, or replenished within, the charge-balanced structure. Based on these findings, design guidelines are proposed that reduce hysteresis-related energy loss by approximately 50% compared with a uniformly doped reference superjunction structure, while preserving a favourable specific on-state resistance, $R_{\mathrm{on,sp}}$, without substantially increasing process complexity.

Keywords: Superjunction, Output-capacitance hysteresis, Charge-balanced drift region, Dynamic capacitance, Finite-element modelling, Incomplete ionisation, Resonant converters, Zero-voltage switching

1. Introduction

The drive towards higher switching frequencies in power electronics is primarily motivated by the need to reduce passive component size and increase power density. This has accelerated both the development of advanced power device architectures, such as superjunction structures, and the transition from silicon towards wide-bandgap semiconductors, including SiC and GaN. Owing to their wider bandgaps and higher critical electric fields, these materials enable thinner and more highly doped drift regions, thereby reducing the specific on-state resistance for a fixed blocking voltage. However, as devices move towards lower conduction losses and faster voltage transients, the accurate treatment of switching losses becomes increasingly important, particularly in converter topologies based on hard-switching operation, where voltage and current overlap during the switching transition.

Soft-switching converters address this limitation by reducing, or ideally eliminating, the overlap between voltage and current during switching. In zero-voltage switching (ZVS) operation, the power semiconductor device is turned on only after the voltage across it has been reduced to zero, ideally eliminating turn-on loss. In resonant converters, the resonant tank and switching frequency are typically selected such that the magnetising or resonant current can discharge the device output capacitance, C_{oss}, during the dead time. The converter is therefore operated in a region where sufficient current is available to discharge C_{oss} before turn-on. In this context, any hysteresis in the output capacitance introduces an additional non-recoverable energy component, reducing the expected benefit of soft switching.

Since the introduction of silicon superjunction (SJ) devices, output-capacitance hysteresis has been recognised as an important limitation in soft-switching converters. It was first reported in devices fabricated using multi-epitaxy multi-implantation processes by Fedison *et al.* [1] and was later attributed by Roig *et al.* [2] to stranded charge in the p/n pillars during charging and discharging of the drift region. The effect was subsequently found to worsen as the cell pitch was reduced, despite pitch scaling being one of the main routes used in later silicon superjunction generations to reduce the on-state resistance [3, 4]. Later studies highlighted that, although the magnitude of the hysteresis is process dependent, it does not completely disappear in trench-refill superjunction structures. This indicates that process-induced stranded charge is only one contribution to the overall hysteresis behaviour [2, 3]. More recently, finite carrier velocity in the semiconductor has been identified by Lin [5] as a fundamental origin of output-capacitance hysteresis. Subsequent electrothermal analysis further highlighted the relevance of the charge–discharge energy loss in off-state superjunction MOSFET operation [6]. However, the influence of cell design and the physical conditions required to minimise the hysteresis remain insufficiently clarified.

In addition to the active drift region, the response of the edge termination can influence the behaviour of the device during fast voltage transients. This is particularly relevant for wide-bandgap semiconductors, where deep dopants, incomplete dopant ionisation, and bulk or surface traps may further affect charge redistribution and exacerbate capacitance hysteresis [7, 8].

In this work, the physical origin of output-capacitance hysteresis is revisited and linked to the relaxation time associated with carrier transport in the charge-balanced drift region. This mechanism leads to asymmetric charging and discharging trajectories of the dynamic output capacitance. Temperature-dependent finite-element simulations are used to verify the proposed interpretation and to analyse the dependence of the hysteresis on temperature, charge-balance condition, incomplete dopant ionisation, cell pitch, voltage slew rate, and non-uniform doping profiles. The results show that appropriate doping-profile engineering can reduce the asymmetry between charging and discharging. In particular, graded electric-field profiles that avoid low-field bottlenecks at the moving depletion boundaries provide lower hysteresis energy by improving charge removal and replenishment during voltage transients.

The effect of incomplete dopant ionisation is also investigated. Partial dopant ionisation can modify the effective charge balance and local conductivity, particularly in wide-bandgap superjunctions where deep dopant levels and temperature-dependent ionisation become important [9].

The central contribution of this work is to link the hysteresis energy directly to the local electric-field and conductivity conditions at the moving depletion boundaries of the charge-

balanced drift region. This interpretation shows that output-capacitance hysteresis is not only a consequence of residual or stranded charge, but also of the finite time required for carriers to be extracted from and reinjected into regions whose conductivity evolves dynamically during the voltage transient. This provides a practical basis for reducing hysteresis through charge-balance and doping-profile engineering.

The remainder of this paper is organised as follows. Section 2 presents the physical origin of output-capacitance hysteresis and the methodology used to extract the dynamic capacitance and hysteresis energy. Section 3 discusses the finite-element simulation results and the resulting device-level mitigation strategies. Section 4 summarises the main conclusions.

2. Physical Origin and Extraction of Dynamic Output-Capacitance Hysteresis

The essential features of output-capacitance hysteresis originate from the electrostatics and transport dynamics of charge-balanced drift regions. In a superjunction structure, alternating p-type and n-type semiconductor pillars are introduced in the drift region. Under charge-balance conditions, the net space charge is close to zero, enabling a nearly flat electric-field profile in the vertical direction. This allows the drift region to be more highly doped than in a conventional one-dimensional drift region, leading to a superior trade-off between specific on-state resistance, $R_{\mathrm{on,sp}}$, and breakdown voltage, BV.

In a conventional vertical drift region, as schematically shown in Fig. 1(a), depletion develops mainly from the main junction and extends vertically into the lightly doped drift layer as the reverse voltage increases. In this case, the expansion and contraction of the depleted region occur mainly along the vertical direction. Unless additional time-dependent effects associated with bulk traps are present, output-capacitance hysteresis is not expected to be significant. In contrast, in a correctly designed superjunction, as shown in Fig. 1(b)–(c), the depletion process initially occurs laterally between adjacent p- and n-type pillars. Charge redistribution therefore involves carrier motion along narrow p- and n-type pillars. This additional transport through narrow and partially depleted paths introduces a finite dynamic response, which can lead to different charging and discharging trajectories in the Q_{oss}–V_{DS} plane, where Q_{oss} is the output charge. The lateral electric field reduces the vertical electric-field gradient, consistent with the redistribution of space charge described by Poisson's equation. The voltage at which the pillars become fully depleted is referred to here as the pillar depletion voltage, or pinch-off voltage. This voltage depends on the charge contained in each pillar, the pillar width, the pillar doping concentration, and the superjunction cell pitch.

In a power MOSFET, this lateral depletion process produces a sharp reduction in both the gate-drain capacitance, C_{gd}, and the drain-source capacitance, C_{ds}, and therefore in the output capacitance, C_{oss}. This forms the basis of the strong nonlinearity of the superjunction output capacitance.

Roig *et al.* [2] attributed the hysteresis observed in silicon superjunction devices to stranded charge associated with the multi-epitaxy multi-implantation process. In such structures, local dopant fluctuations and non-uniform pillar profiles can make depletion and re-population of the pillars asymmetric during charging and discharging. Trench-filled superjunctions, which generally provide a more uniform doping profile, have been shown to exhibit reduced hysteresis. Further clarification was provided by Lin [5], who identified finite semiconductor carrier velocity as a key physical origin of dynamic charge hysteresis. However, clear design rules

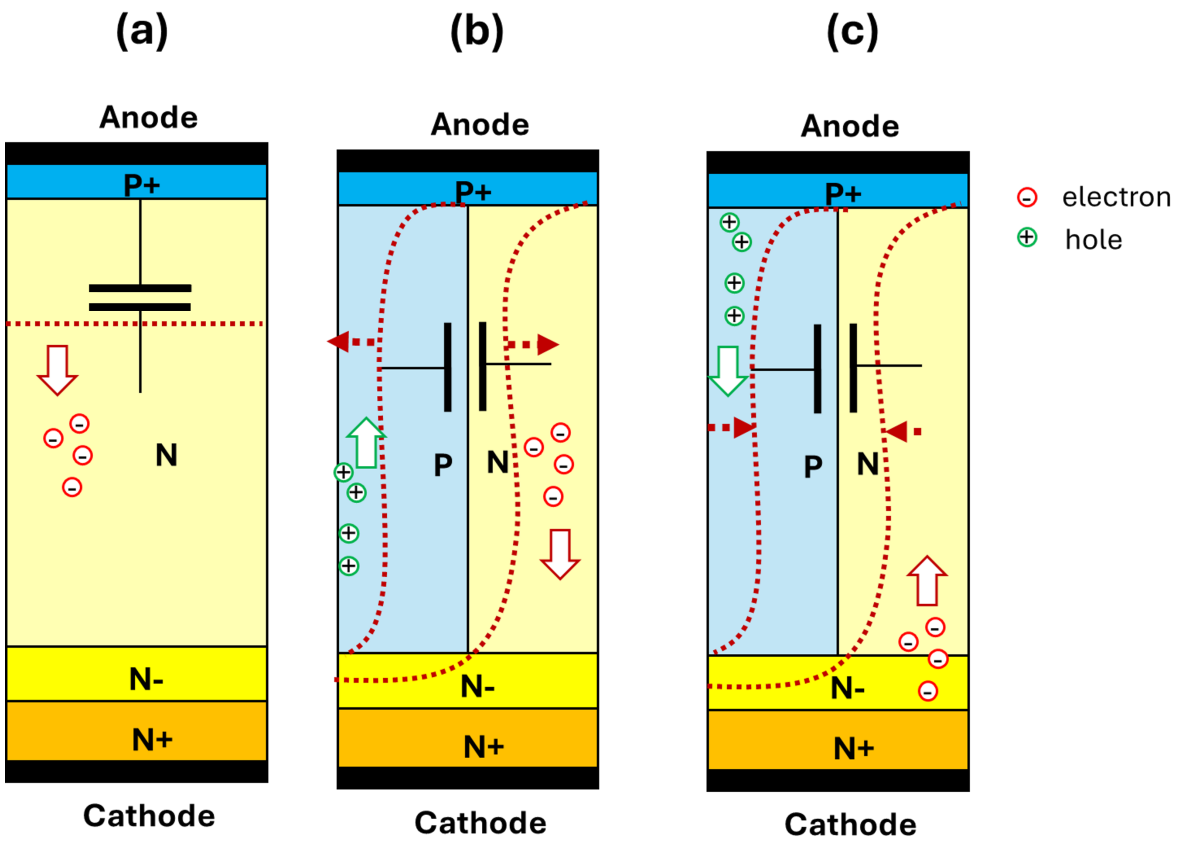

Figure 1: Schematic comparison between a conventional vertical drift region and a charge-balanced superjunction structure: (a) vertical depletion in a conventional drift region when the reverse voltage increases; (b) lateral depletion between adjacent p- and n-type pillars in a superjunction during the charging phase, i.e. when the reverse voltage increases; and (c) lateral depletion between adjacent p- and n-type pillars in a superjunction during the discharging phase, i.e. when the reverse voltage decreases. The arrows indicate carrier motion associated with removing or replenishing charge in the drift region. The dashed red line represents the depletion-region front.

for mitigating this effect remain limited, particularly for multi-epitaxy multi-implantation superjunctions and for future wide-bandgap implementations, where incomplete dopant ionisation may further modify the internal charge distribution. The temperature dependence of output-capacitance hysteresis also remains insufficiently clarified in the literature.

In this work, we therefore examine how the internal electric-field distribution of a charge-balanced drift region influences the dynamic charging and discharging trajectories of C_{oss}. Rather than treating capacitance hysteresis only as an unavoidable consequence of finite carrier transport, we show that the magnitude of the hysteresis-related energy loss can be reduced by engineering the superjunction design so that carrier extraction and reinjection occur more symmetrically during charging and discharging.

To analyse this behaviour, it is useful to consider the local dielectric relaxation time implied by the Drude conductivity. This description is not intended to replace the full two-dimensional electrostatic and transport solution. Instead, it provides a simplified physical interpretation of the local time scales that govern carrier redistribution. For a region with local conductivity σ, the characteristic charge-relaxation time can be interpreted using a local resistance $R = \rho L/A$ and capacitance $C = \varepsilon_s A/L$, where ρ is the resistivity, L is the characteristic transport length, A is the effective cross-sectional area, and ε_s is the

semiconductor permittivity. The corresponding RC time constant is therefore

$$\begin{aligned}\tau_{\mathrm{RC}} &= RC = \rho\varepsilon_s = \frac{\varepsilon_s}{\sigma} \\ &= \frac{\varepsilon_s}{q\left(\mu_n n + \mu_p p\right)}.\end{aligned} \tag{1}$$

Here, τ_{RC} is the characteristic charging/discharging time constant, σ is the local electrical conductivity, q is the elementary charge, μ_n and μ_p are the electron and hole mobilities, and n and p are the electron and hole concentrations, respectively. Equation (1) shows that the dynamic response in each pillar is directly controlled by the local carrier density and mobility. Regions with low conductivity, such as strongly depleted superjunction regions with high local electric fields, will therefore respond more slowly.

A superjunction diode, as represented schematically in Fig. 1(b)–(c), provides a useful approximation of a gate-source-shorted MOSFET during the charging and discharging of C_{oss}, as the channel is suppressed and the device response is dominated by the internal drift-region capacitance. During charging, holes are extracted from the source/anode side while electrons are extracted from the cathode/drain side, allowing the superjunction drift region to deplete. During discharging, carriers must be reinjected and redistributed into the depleted p- and n-type pillars. Once the superjunction is strongly depleted, the available mobile carrier density in the pillars is suppressed. Re-population during the discharging phase is therefore limited by finite carrier velocity in the long pillar regions and by the time required to re-establish conductive paths within the p- and n-type pillars. As a result, the discharging trajectory may become slower and, more generally, different from the charging trajectory, producing hysteresis in the Q_{oss}–V_{DS} characteristic.

The energy associated with the charging and discharging branches can be calculated from the corresponding large-signal Q_{oss}–V_{DS} curves as

$$\begin{aligned}E_{\mathrm{oss,ch}} &= \int_0^{Q_{\max}} V_{\mathrm{DS,ch}}\left(Q_{\mathrm{oss}}\right)\, dQ_{\mathrm{oss}}, \\ E_{\mathrm{oss,dis}} &= \int_0^{Q_{\max}} V_{\mathrm{DS,dis}}\left(Q_{\mathrm{oss}}\right)\, dQ_{\mathrm{oss}}, \\ E_{\mathrm{diss}} &= E_{\mathrm{oss,ch}} - E_{\mathrm{oss,dis}}.\end{aligned} \tag{2}$$

Here, $E_{\mathrm{oss,ch}}$ is the energy associated with the charging branch, $E_{\mathrm{oss,dis}}$ is the energy recovered during the discharging branch, $Q_{\max}$ is the maximum output charge reached during the cycle, and $V_{\mathrm{DS,ch}}$ and $V_{\mathrm{DS,dis}}$ are the drain-source voltages along the charging and discharging trajectories, respectively. The difference between the two energies, E_{diss}, represents the energy dissipated because of hysteresis. In resonant converters, the corresponding power loss can be estimated as $P_{\mathrm{diss}} = E_{\mathrm{diss}} f_{\mathrm{sw}}$, where f_{sw} is the switching frequency.

The dynamic output capacitance used in the remainder of this work is extracted from the transient current and voltage waveforms as

$$C_{\mathrm{oss,dyn}} = \left| \frac{I_D}{dV_{\mathrm{DS}}/dt} \right|. \tag{3}$$

Here, I_D is the displacement current associated with the charging or discharging of the output capacitance, and dV_{DS}/dt is the drain-source voltage slew rate, or cathode-anode voltage slew rate for the equivalent diode structure. This definition captures the large-signal transient capacitance of the device and is therefore more representative of resonant switching operation than a small-signal capacitance measured at a fixed bias point.

The electric-field distribution inside the superjunction is governed by Poisson's equation,

$$\nabla \cdot (\varepsilon_s \nabla \phi) = -q \left(p - n + N_D^+ - N_A^- \right). \tag{4}$$

Here, ϕ is the electrostatic potential, N_D^+ and N_A^- are the ionised donor and acceptor concentrations, respectively, and the remaining symbols have the same meaning as in Eq. (1). Equation (4) highlights the central role of pillar doping and charge balance in shaping the electric-field profile. Any deviation from ideal charge balance modifies the local space-charge distribution and can therefore alter both the depletion dynamics and the transient charging/discharging behaviour.

The electric-field shape inside the superjunction, particularly in the central region of the charge-balanced layer, is therefore critical for reducing charge hysteresis. While a flat vertical electric-field profile is desirable for optimising the conventional BV–$R_{\mathrm{on,sp}}$ trade-off under ideal charge-balance conditions, it is not necessarily optimal from a dynamic charging/discharging perspective. This is because the depletion and reinjection fronts near the anode and cathode sides may not evolve at the same rate during the two phases of the cycle. As discussed in Section 3, improved hysteresis behaviour can be achieved by engineering the internal field profile so that carrier extraction and reinjection occur more symmetrically. Equation (1) also indicates that higher carrier mobility, shorter superjunction lengths, wider conductive paths, and higher effective conductivity can reduce the characteristic response time and therefore mitigate the hysteresis effect.

2.1. Dynamic Capacitance Extraction Methodology

Figure 2(a) schematically illustrates the reduction in small-signal output capacitance and the corresponding large-signal charging–discharging hysteresis typically observed in charge-balanced devices. Experimentally, this behaviour can be extracted using variations of the Sawyer–Tower circuit, as previously reported in the literature [10, 11]. This method has been widely used to obtain Q_{oss}–V_{DS} characteristics in several power semiconductor technologies, including GaN HEMTs and silicon superjunction MOSFETs [3, 12–14].

The usefulness of the Sawyer–Tower approach lies in its ability to separately capture the large-signal charging and discharging trajectories of a nonlinear capacitor exhibiting hysteresis. In this configuration, the reference capacitor, C_{ref}, is used to integrate the displacement current and therefore determine the transferred charge [10].

The internal charging and discharging process can also be reproduced using a resonant half-bridge test circuit, as shown in Fig. 2(b). In this configuration, the DUT is placed in one branch of the half bridge with its gate shorted to the source contact. This suppresses channel conduction and ensures that the device response is mainly governed by the charging and discharging of its internal output capacitance during each switching cycle. Such circuit configurations have been used to observe capacitance hysteresis in silicon superjunction devices, including cases where the internal junction temperature increases over multiple

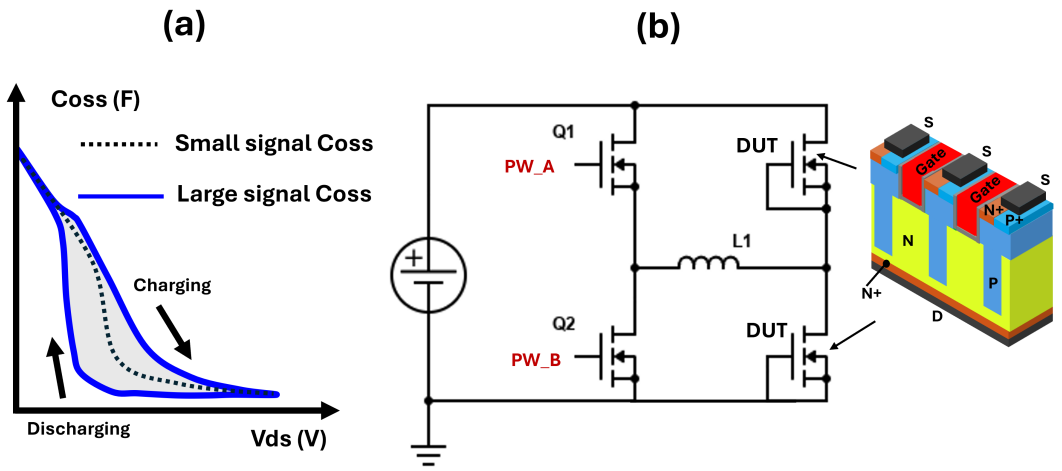

Figure 2: (a) Schematic representation of the reduction in small-signal output capacitance and the corresponding large-signal charging–discharging behaviour. (b) Resonant half-bridge circuit used to evaluate output-capacitance hysteresis, where the DUT is a charge-balanced silicon superjunction MOSFET operated in diode configuration by shorting the gate and source terminals.

resonant cycles because part of the output-capacitance energy is dissipated rather than recovered. The simulated bus voltage, V_{bus}, used for the circuit in Fig. 3 is 200 V, the resonant inductor is $L_1 = 90\,\mu\mathrm{H}$, and the switching frequency is $f_{\mathrm{sw}} = 400\,\mathrm{kHz}$. The device area is $1\,\mathrm{cm}^2$. The auxiliary switches, Q_1 and Q_2, are modelled as non-superjunction MOSFETs and are driven according to the modulation sequence described in [13, 15]. The switching-node voltage and current waveforms are also affected by the nonlinear voltage dependence of C_{oss}, as illustrated in Fig. 3.

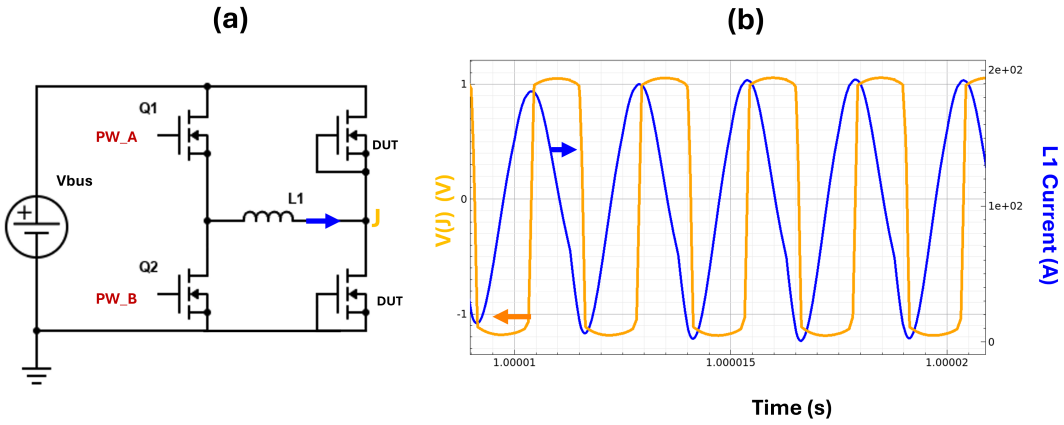

Figure 3: (a) Schematic simulation circuit in which the DUT is represented by a finite-element model of a superjunction diode/MOSFET structure. (b) Representative voltage and current waveforms at the switching node, highlighting the charging and discharging process of the DUT.

To reproduce the main features of output-capacitance hysteresis while isolating the internal device physics, a superjunction diode structure with a target blocking voltage of approximately 650 V is simulated, as shown in Fig. 4. Rather than modelling the full resonant converter of Fig. 2(b), the finite-element device model is driven by a simplified voltage pulse generator with a controlled dV_{DS}/dt. This approach removes the influence of external circuit parasitics and resonant-tank design, allowing the internal charge-redistribution dynamics of the superjunction structure to be examined directly.

The energy dissipated during one charging/discharging cycle is calculated from Eq. (2), which is equivalent to the energy loss obtained by integrating $I_D V_{\mathrm{DS}}$ over one full cycle. The dynamic output capacitance is extracted from the transient current and voltage waveforms using Eq. (3). During each charging and discharging transient, the internal electric-field distribution and other physically relevant quantities, including carrier velocity, carrier-density evolution, and the motion of the depletion-front boundaries, are monitored to correlate the extracted hysteresis energy with the underlying charge-redistribution dynamics.

The finite-element simulations include the relevant carrier transport, recombination, mobility, and ionisation models, with the detailed physical model settings consistent with previous finite-element studies of superjunction and incomplete-ionisation effects [4, 9]. Symmetric Neumann boundary conditions are applied to geometrical boundaries not connected to electrical contacts, while perfect Ohmic boundaries are assumed for the anode and cathode regions. The n^- layer represents a buffer region with a thickness fixed at $L/10$, included to provide a more gradual reverse-recovery behaviour in practical devices. The effects of the edge termination and gate-pad area are neglected at this stage. This approximation is reasonable for isolating the active-cell physics, although the termination contribution can become significant as the die area is reduced and should be considered in future full-device analyses. Unless otherwise specified, the voltage slew rate applied to the device is $1\,\mathrm{V/ns}$ and the superjunction design is assumed to be symmetric, i.e. $\epsilon = 0.5$. The discussion presented in this manuscript focuses on 650 V superjunction drift regions; however, the underlying physical mechanisms and design principles can be readily extended to both lower- and higher-voltage device classes.

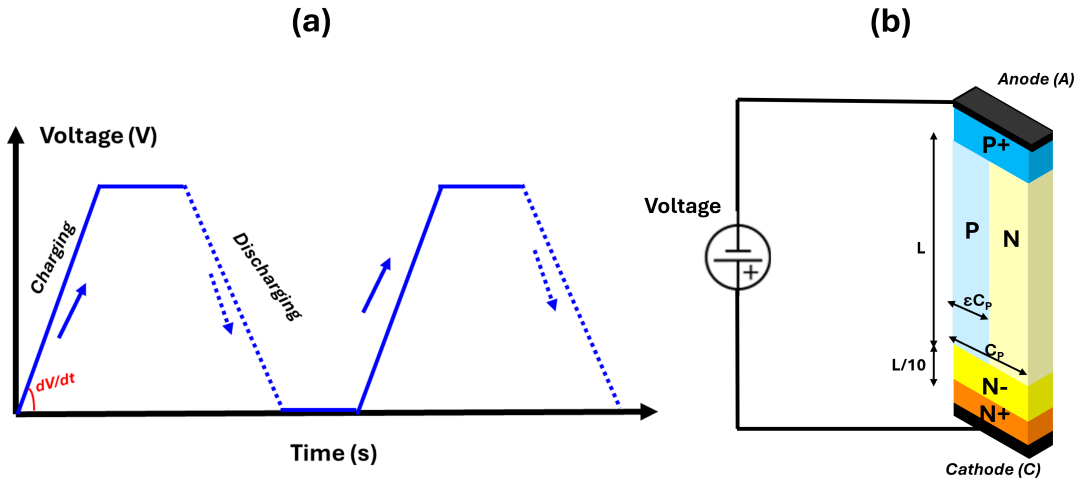

Figure 4: Finite-element simulation setup used to analyse dynamic output-capacitance hysteresis. (a) Voltage transient pulse sequence applied to emulate charging and discharging of the output capacitance. (b) Superjunction diode structure connected to the voltage pulse. For the silicon reference structure, the drift-region thickness is $L = 33\,\mu\mathrm{m}$, while the superjunction geometrical asymmetry parameter, ϵ, is varied from 0.2 to 0.8 to analyse the $R_{\mathrm{on,sp}}$–E_{diss} figure of merit. The parameter C_P denotes half of the superjunction cell pitch. For $\epsilon = 0.5$, the pillar doping concentration is fixed at 5×10^{15} cm^{-3}. When ϵ is varied, the pillar doping is adjusted to maintain equal total charge in the p- and n-pillars, i.e. $\epsilon C_P N_p = (1-\epsilon) C_P N_n$. Constant, flat doping profiles are assumed unless specified otherwise. The dynamic capacitance is extracted from the simulated current and voltage waveforms using Eq. (3).

3. Analysis and Results

3.1. Influence of Cell Pitch, Temperature, and Voltage Slew Rate

Using the simulation setup described in the previous section, the impact of output-capacitance hysteresis is analysed for a silicon-based superjunction device targeting 650 V. Figure 5(a) shows that the charging and discharging dynamics are a strong function of the voltage slew rate. Faster voltage transients increase the separation between the charging and discharging branches, thereby increasing the degree of hysteresis. This behaviour is consistent with the finite carrier-redistribution time described in Section 2. When the external voltage transient is faster than the characteristic response of the charge-balanced drift region, carrier extraction and replenishment cannot follow the applied bias instantaneously. It is worth noting that this setup with constant doping profiles in both pillars more closely reproduces a trench-refill process than a conventional multi-epitaxy multi-implantation process.

Figure 5(b) shows the temperature dependence of the large-signal capacitance. In the silicon superjunction case considered here, where no deep dopant species are included in the pillars, higher temperature leads to increased hysteresis. This is attributed primarily to the reduction in carrier mobility with temperature, which increases the local dielectric relaxation time described by Eq. (1). As a result, carrier removal and replenishment become slower, and the charging–discharging asymmetry becomes more pronounced. This also supports the experimental observations reported in [1], where continuous charging and discharging of the output capacitance can lead to device failure as the internal junction temperature rises.

Figure 6 clarifies the time evolution of the charging and discharging process by visualising the depletion-region boundary, electric field, and hole velocity. The asymmetry in the depletion boundaries during charging and discharging illustrates how the electric-field evolution and carrier-removal process are affected by the high average electric field across the superjunction structure. In this case, ideal charge-balance conditions are assumed, resulting in an approximately flat electric-field profile along a vertical cutline.

Figure 7(a) shows that hysteresis losses are exacerbated at higher temperatures for silicon-based superjunction devices, worsening the overall E_{diss}–$R_{\mathrm{on,sp}}$ figure of merit. Cell-pitch reduction, while keeping the same total pillar charge by increasing the doping concentration proportionally, also leads to a less favourable trade-off. This indicates that the dynamic depletion and re-population of narrower, more highly doped regions can become more challenging under fast voltage transients. To further support the relaxation-time interpretation, Fig. 7(b) shows that hysteresis losses are reduced by approximately 50% when both electron and hole mobilities are artificially increased by a factor of ten. These findings are consistent with experimental observations that some newer, more aggressively scaled superjunction MOSFETs can exacerbate the hysteresis problem. It is also worth noting that, for the selected cell pitch, the geometrical asymmetry of the superjunction, controlled by ϵ, is not the dominant contributor to the observed hysteresis. The results also suggest that longer, more lightly doped superjunction drift regions designed for higher blocking voltages may exhibit stronger hysteresis, provided that incomplete-ionisation effects are not dominant.

3.2. Influence of Charge-Balance Condition

Once the fundamental process leading to asymmetric charging and discharging has been clarified, design strategies can be applied to mitigate the hysteresis effect while maintaining a

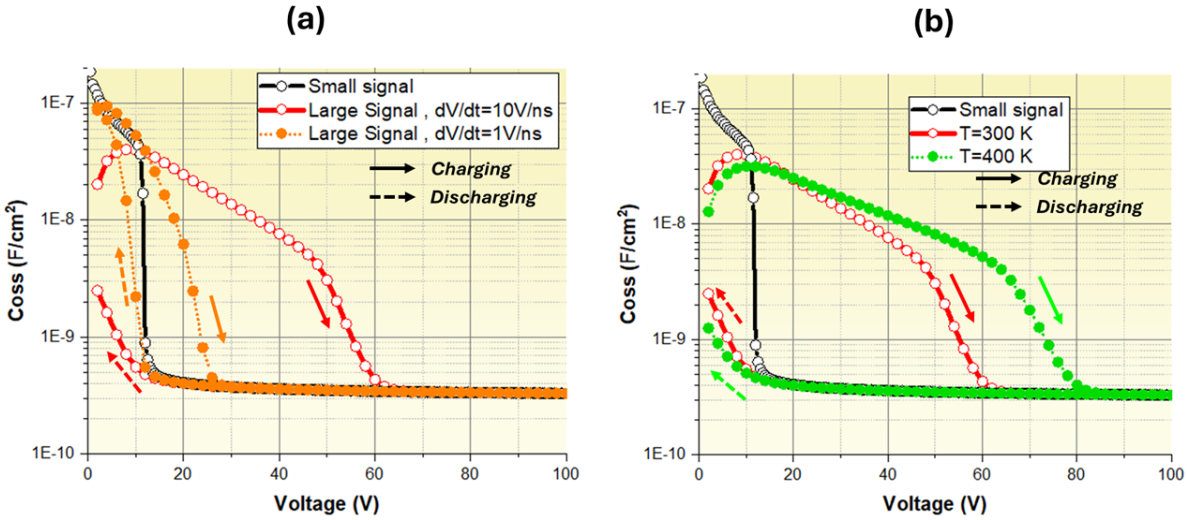

Figure 5: (a) Comparison between small-signal and large-signal output capacitance, highlighting the increase in hysteresis at faster voltage slew rates, obtained for $\epsilon = 0.5$, where the n- and p-pillars are geometrically symmetric. (b) Temperature dependence of the large-signal output capacitance.

favourable E_{diss}–$R_{\text{on,sp}}$ trade-off. Since the inception of superjunction devices, it has been recognised that a perfectly flat electric-field profile can be detrimental to reliability and robustness. Process variations that introduce charge imbalance can lead to electric-field crowding either near the device surface under n-rich conditions or near the bottom of the drift region under p-rich conditions. This makes the device sensitive to local charge perturbations, especially in n-rich conditions, particularly at the semiconductor/oxide interface and in the edge-termination region. On the other hand, a p-rich profile can shift the peak electric field towards the bottom of the superjunction layer, which may improve surface-charge robustness and reduce hysteresis. However, excessive p-rich imbalance can reduce the blocking-voltage margin and narrow the acceptable manufacturing window [16].

As shown in Fig. 8, a p-rich condition can reduce the degree of hysteresis, but this improvement comes at the expense of reduced blocking voltage. Such design choices must take into account the effect of charge imbalance, the edge-termination design, and the allowable charge-balance window during manufacturing. In these simulations, the unbalance ratio is defined as

$$\text{Unbalance ratio} = 100 \times \frac{N_p - N_n}{N_n}, \tag{5}$$

where N_n is the n-pillar doping concentration, which is kept constant, while the p-pillar doping concentration, N_p, is varied.

3.3. Influence of Non-Uniform and Graded Doping Profiles

Sloped or graded doping profiles, which can be obtained either in multi-epitaxy multi-implantation processes through dose engineering or in trench-refill structures through pillar tapering, provide a practical route to reshape the electric-field profile without necessarily compromising the overall charge-balance condition. In typical 600 V–650 V silicon superjunction

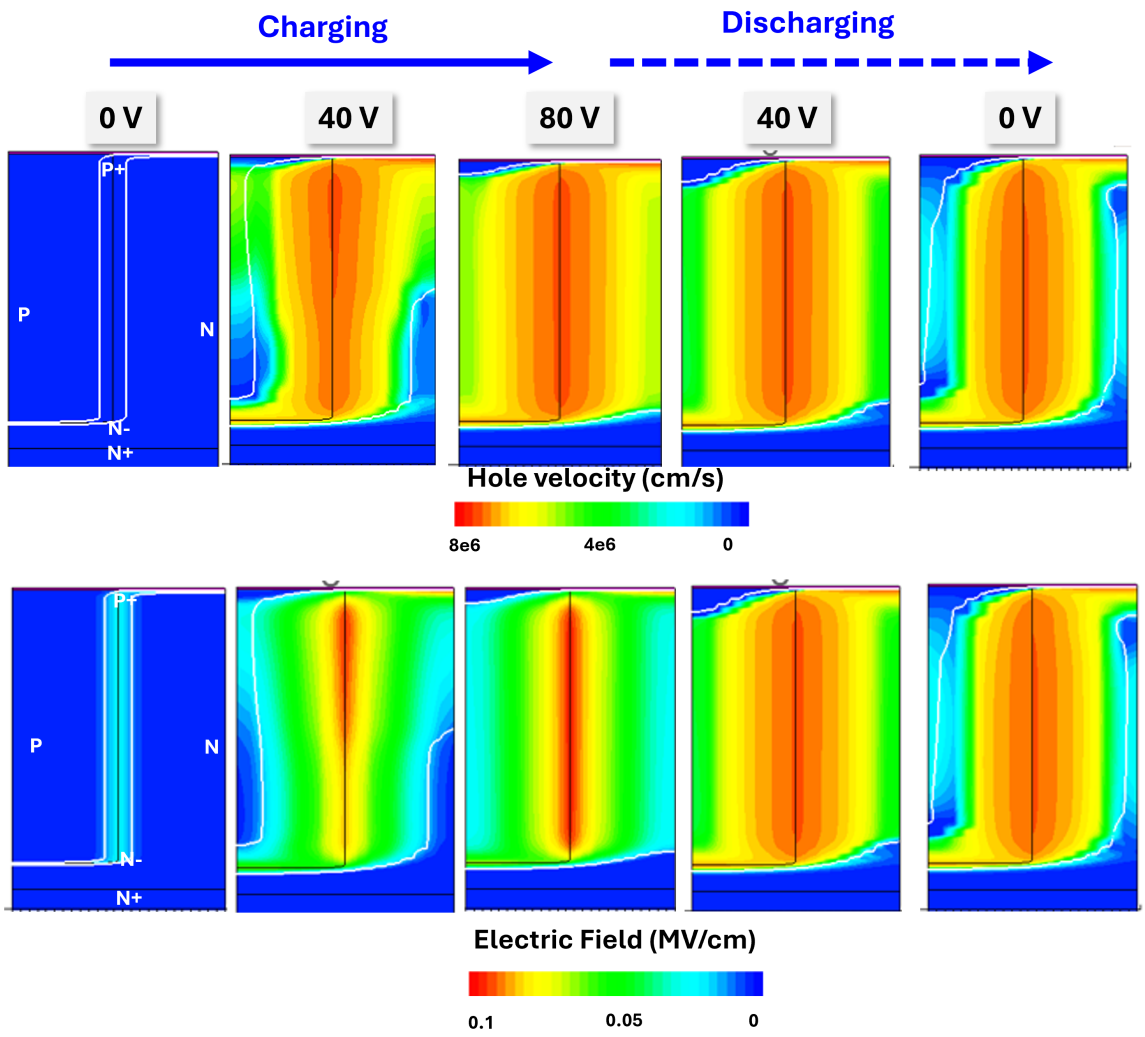

Figure 6: Finite-element modelling of the charging and discharging process in a silicon-based superjunction device without doping-profile engineering, i.e. with constant pillar doping, obtained for $\epsilon = 0.5$, where the n- and p-pillars are geometrically symmetric. The depletion-region boundary remains contracted during the discharge phase, leading to the observed hysteresis and lower discharging capacitance. The hole-velocity profile, which is field dependent, highlights the finite speed of the carrier removal and replenishment processes.

devices, this process may involve multiple epitaxial growth and implantation steps, typically around 10–13, allowing the vertical doping profile of the pillars to be engineered.

Figure 9 shows a strategy for engineering the doping profile inside the superjunction layer to reshape the electric field according to Poisson's equation. In this design, the structure is effectively n-rich near the top and p-rich near the bottom, leading to a positive electric-field slope in the upper region and a peak field closer to the centre of the charge-balanced layer. This produces a characteristic bell-shaped electric-field profile, which is known to improve robustness against charge imbalance because additional p- or n-type charge mainly shifts the position of the field peak rather than producing strong field crowding at one boundary.

Such a doping profile can be achieved by tuning the doping sequence in a multi-epitaxy multi-implantation process and by controlling dopant diffusion during subsequent thermal treatments. In principle, the vertical ripple of the p- and n-pillars can also be adjusted

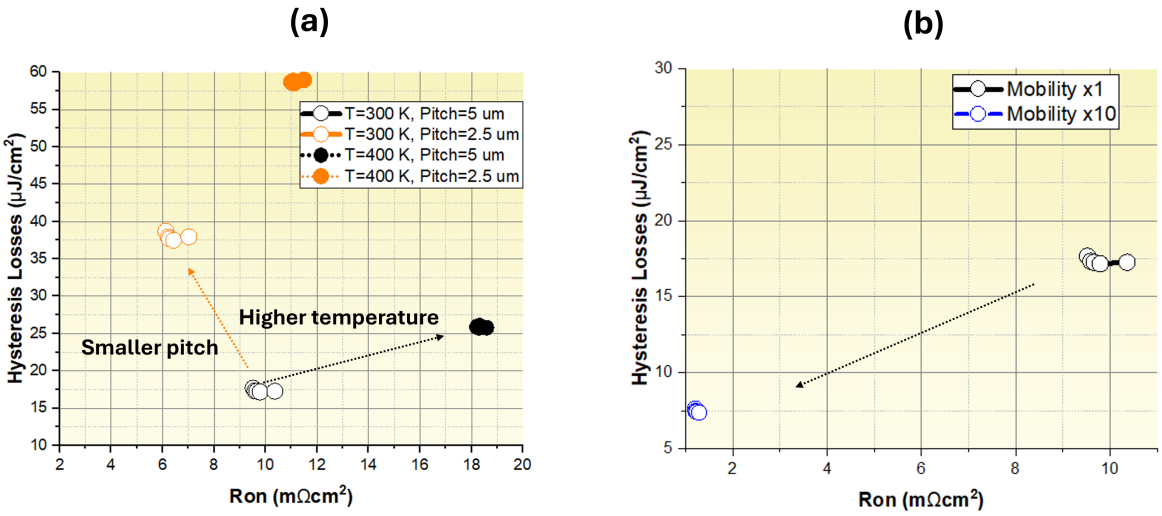

Figure 7: (a) E_{diss}–$R_{\mathrm{on,sp}}$ figure of merit for different cell pitches and junction temperatures. (b) Reduction in hysteresis losses when the carrier mobilities of both electrons and holes are increased by a factor of ten. Different data points for each technology curve correspond to different values of ϵ, which determines the superjunction symmetry. Perfect charge-balance conditions are assumed.

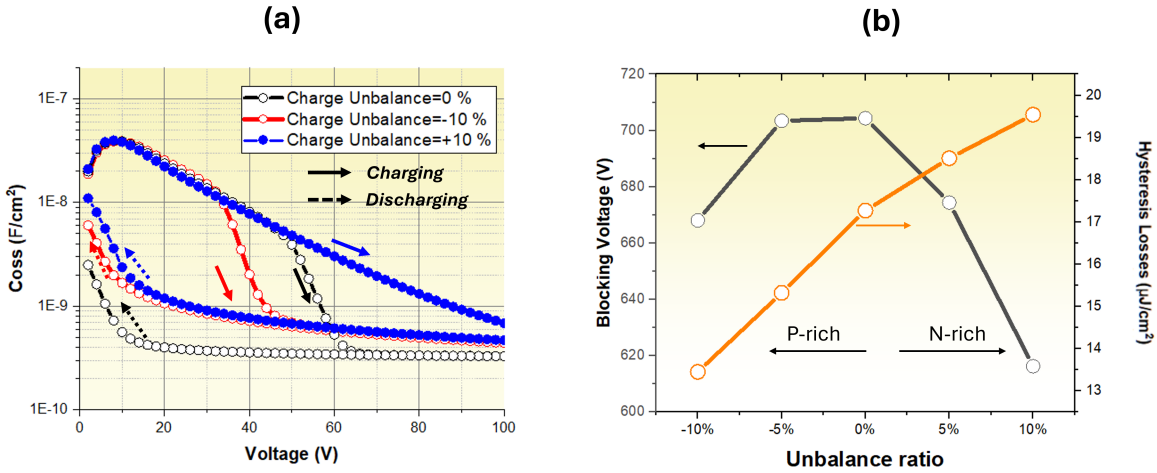

Figure 8: (a) Effect of charge-balance condition on dynamic output-capacitance hysteresis, obtained for $\epsilon = 0.5$, where the n- and p-pillars are geometrically symmetric. Positive charge imbalance indicates excess n-type charge in the superjunction. (b) Blocking voltage and hysteresis losses as a function of unbalance ratio. The imperfect symmetry of the BV–unbalance trend is attributed to the presence of the bottom n-type buffer layer, which also contributes to the overall charge balance of the device.

through the drive-in time after implantation. A drawback of this design is that the peak blocking voltage may be slightly reduced compared with an ideally balanced flat-field structure. However, this penalty can be offset by an enlarged charge-balance window and improved robustness. Similar concepts have also appeared in early patents on superjunction-based devices to improve device robustness under unclamped inductive switching conditions [17] or during short-circuit events. Under these conditions, the bell-shaped profile allows the hotspot caused by Joule heating to develop deeper inside the active area. Related pillar-profile engineering has also been used to tune the static and dynamic trade-offs of superjunction MOSFETs [4]. For processes that do not rely on multi-epitaxy multi-implantation, a tapered or graded profile may also be introduced through trench-refill engineering [2, 3].

The additional advantage of such a profile is the possibility of reducing charge hysteresis compared with the constant-doping case. Figure 10 shows that a positive p-pillar slope reduces the hysteresis-related energy loss and improves the E_{diss}–$R_{\mathrm{on,sp}}$ figure of merit. Figures 11 and 12 further illustrate the corresponding electric-field and hole-velocity evolution during charging and discharging. The positive p-pillar slope reduces the electric field near the regions where charging and discharging initially occur, while concentrating the peak field in a smaller central region. This improves the local relaxation dynamics at the moving depletion boundaries, allowing the depletion region to expand and contract more symmetrically and thereby reducing hysteresis losses. However, excessive dopant slopes or geometry tapers can affect the peak blocking voltage and should therefore be limited. The simulations shown here assume a slope of either $+10\%$ or -10%, meaning that the doping variation at the top and bottom of the superjunction differs by $\pm 10\%$ relative to the doping in the middle of the device. This limits the breakdown-voltage reduction at the balance point to approximately 30 V.

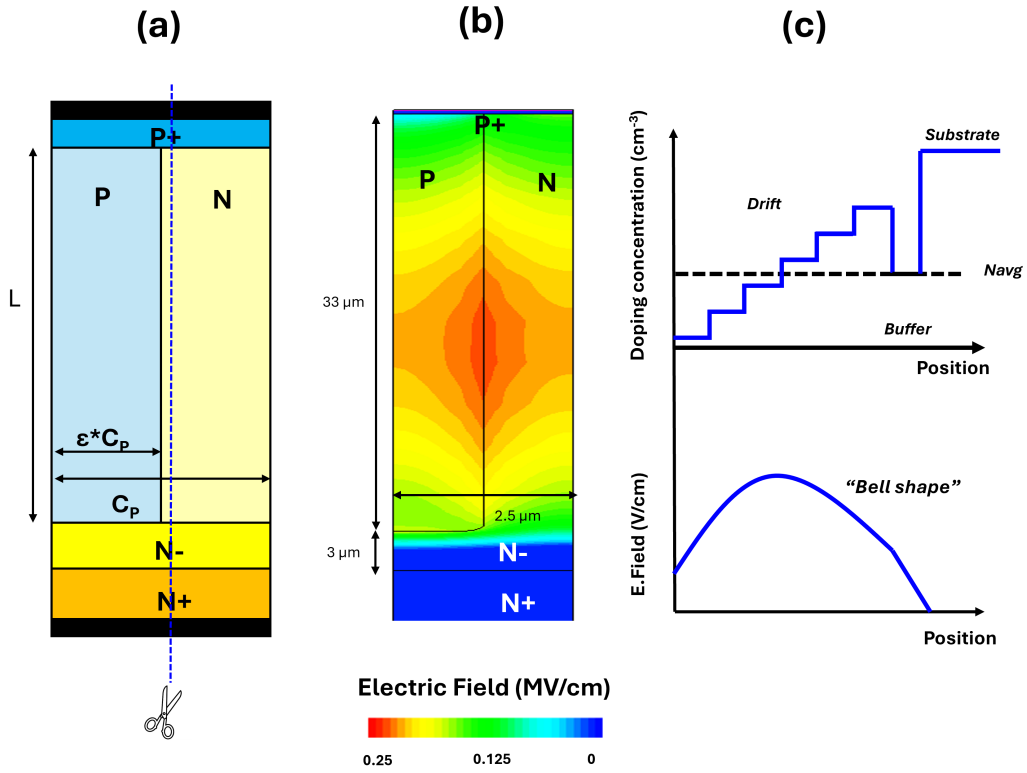

Figure 9: (a) Schematic cross-section, (b) resulting off-state electric-field profile at $V_{\mathrm{off}} = 600$ V, and (c) doping definition for a graded p-pillar profile. The structure produces a characteristic bell-shaped electric-field profile that peaks near the centre of the charge-balanced region. Perfect charge-balance conditions are assumed, with the average p-pillar doping, shown by the dashed line in (c), matching the constant n-pillar doping. The stepped profile can be approximately achieved with a multi-epitaxy multi-implantation process by controlling the dose of each implant and ensuring that the average dose corresponds to the level shown in the stepped profile. In a trench-refill process, the doping concentration can be controlled to achieve a sharper stepped profile, as shown schematically. The simulations assume 11 steps of 3 µm each.

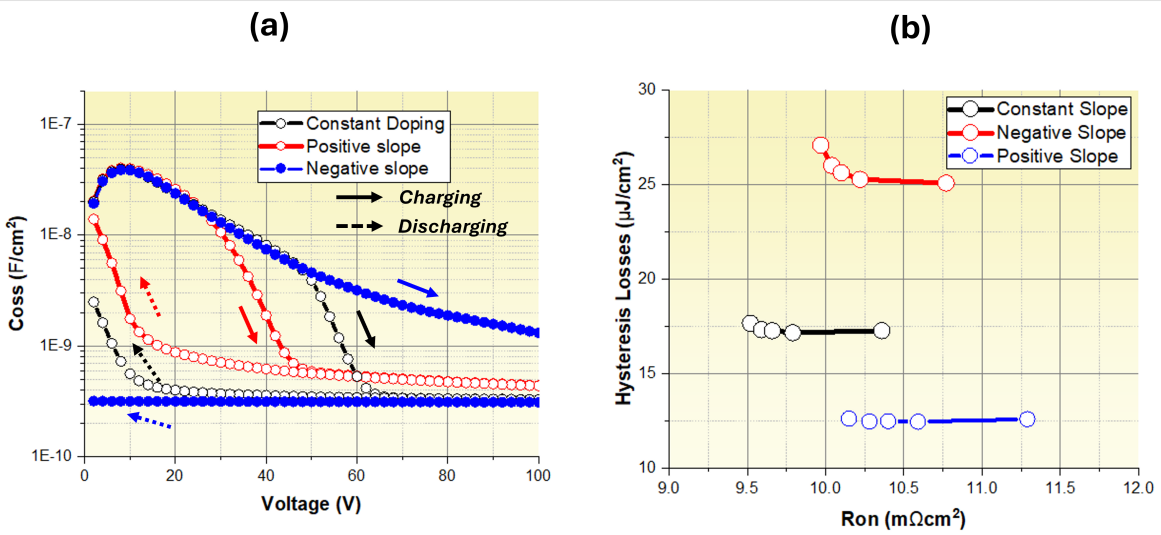

Figure 10: (a) C_{oss} hysteresis for positive and negative p-pillar doping slopes at 300 K, obtained for $\epsilon = 0.5$, where the n- and p-pillars are geometrically symmetric. (b) E_{diss}–$R_{\mathrm{on,sp}}$ figure of merit, highlighting the advantage of a positive p-pillar slope, corresponding to higher p-type doping towards the bottom of the superjunction layer.

3.4. Temperature Dependence and Partial Ionisation

Wide-bandgap semiconductors such as 4H-SiC are strongly affected by incomplete dopant ionisation, particularly in p-type regions where acceptor levels are relatively deep. In charge-balanced drift regions, incomplete ionisation modifies the effective ionised charge density and can therefore shift the device away from the intended charge-balance condition during transient operation. If the electrical excitation is faster than the characteristic response of the ionised dopant population, the superjunction may temporarily behave as an imbalanced structure. This can increase local electric-field crowding, leakage current, and junction temperature. Under repeated switching cycles, the increased temperature may partially mitigate the effect by increasing dopant ionisation, although it may also introduce additional electrothermal stress.

In 4H-SiC, the higher critical electric field allows a 650 V drift region to be realised with a much thinner layer than in silicon. In the structure considered here, the drift-region thickness is approximately 6 µm, compared with 33 µm for the silicon superjunction reference structure. The pillar doping concentration is approximately 1×10^{17} cm^{-3}, which is more than one order of magnitude higher than in the silicon case for the same voltage rating. The total pitch of the 4H-SiC structure is 0.8 µm, maintaining a similar aspect ratio to the silicon superjunction diode discussed above. The material parameters used for 4H-SiC are consistent with previous finite-element studies of incomplete ionisation and SiC device modelling [9, 19, 20]. Figures 13 and 14 show that partial ionisation of the p-type pillar, assuming an acceptor activation energy of approximately 0.265 eV, leads to charging and discharging dynamics that are markedly different from those observed in silicon under complete-ionisation assumptions.

The transient ionisation of dopants can be described using first-order carrier capture and emission kinetics [9, 18]. For donors and acceptors, the ionised dopant concentrations are

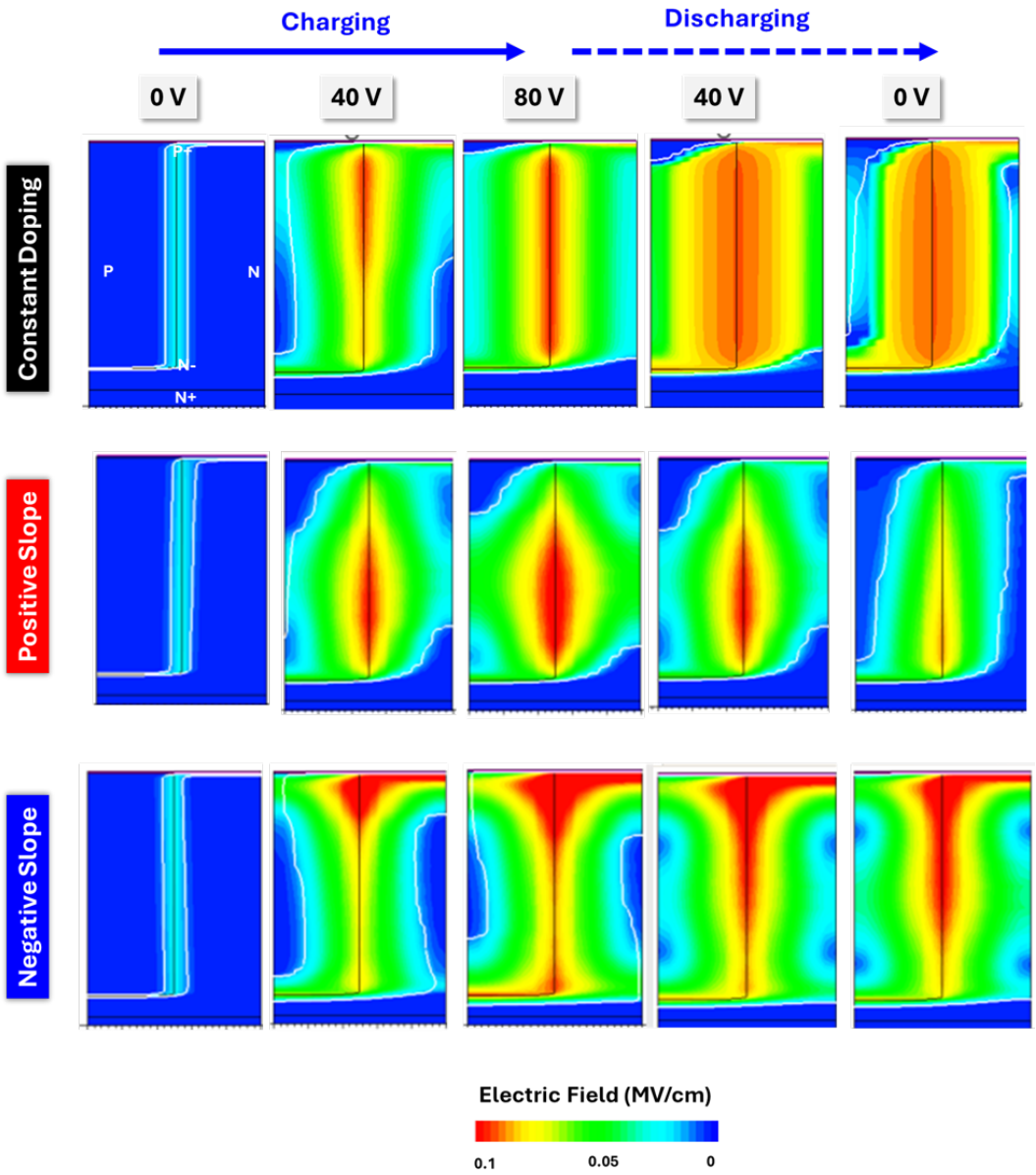

Figure 11: Electric-field profile during the charging and discharging dynamics corresponding to Fig. 10(a). The positive p-pillar slope, corresponding to lower p-type concentration near the anode and higher p-type concentration near the cathode, produces a lower electric field near the moving depletion boundaries. This simplifies carrier replenishment during the discharge phase and reduces hysteresis during the charging phase.

written as

$$\frac{\partial N_D^+}{\partial t} = v_{\mathrm{th},e}\sigma_D \left[\frac{n_1}{g_D}N_{D0} - \left(n + \frac{n_1}{g_D}\right)N_D^+\right], \tag{6a}$$

$$n_1 = N_C \exp\left[-\frac{E_C - E_D}{kT}\right], \tag{6b}$$

$$\frac{\partial N_A^-}{\partial t} = v_{\mathrm{th},h}\sigma_A \left[\frac{p_1}{g_A}N_{A0} - \left(p + \frac{p_1}{g_A}\right)N_A^-\right], \tag{6c}$$

$$p_1 = N_V \exp\left[-\frac{E_A - E_V}{kT}\right]. \tag{6d}$$

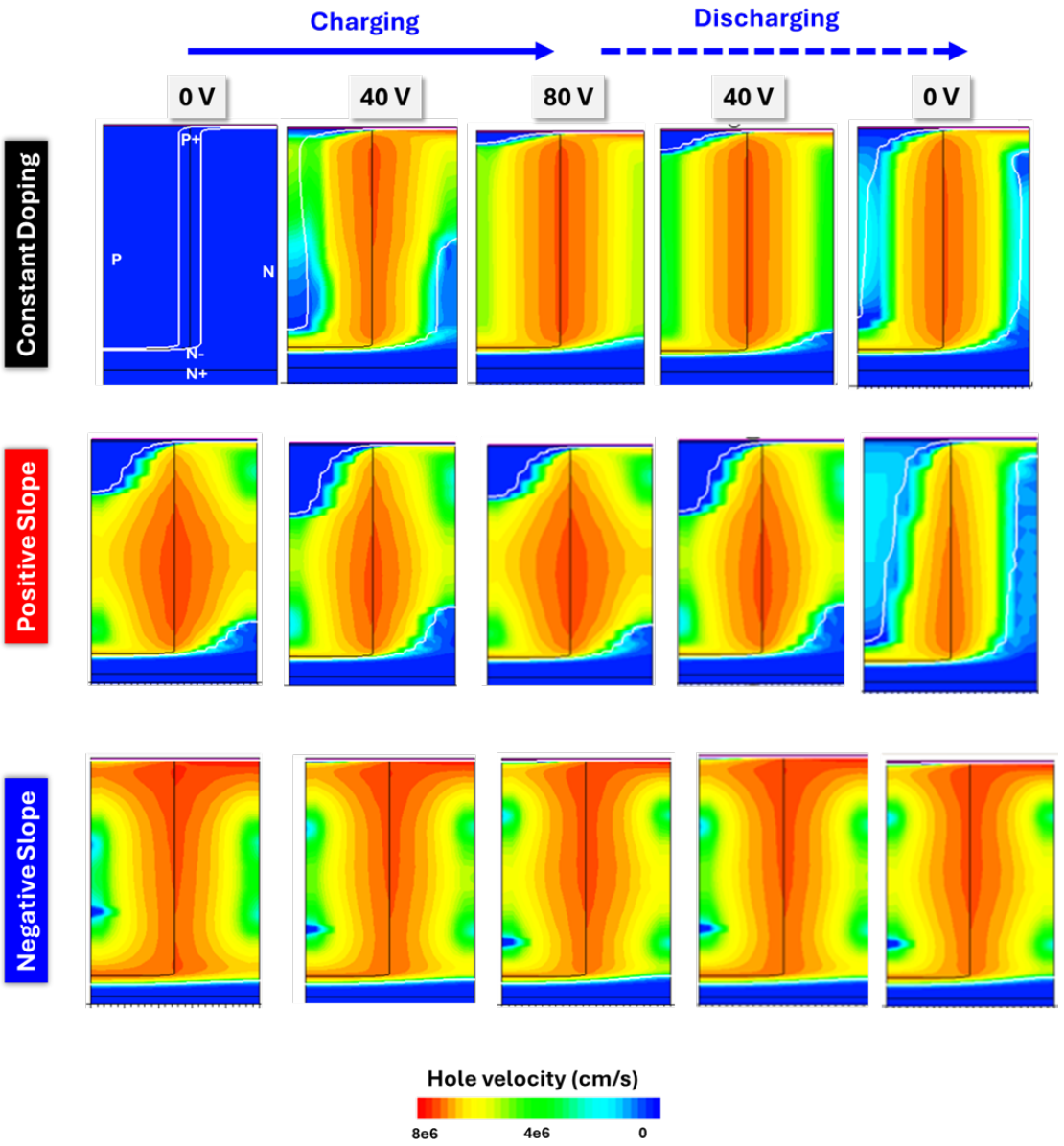

Figure 12: Hole-velocity profile during the charging and discharging dynamics corresponding to Fig. 10(a).

Here, N_D^+ and N_A^- are the ionised donor and acceptor concentrations, respectively, while N_{D0} and N_{A0} are the total donor and acceptor concentrations. The quantities $v_{\mathrm{th},e}$ and $v_{\mathrm{th},h}$ are the electron and hole thermal velocities, σ_D and σ_A are the donor and acceptor capture cross sections, and g_D and g_A are the corresponding degeneracy factors. The electron and hole concentrations are denoted by n and p, respectively. The quantities n_1 and p_1 are the effective carrier densities associated with emission from the donor and acceptor levels. N_C and N_V are the effective densities of states in the conduction and valence bands, E_C and E_V are the conduction- and valence-band edges, E_D and E_A are the donor and acceptor energy levels, k is the Boltzmann constant, and T is the absolute temperature. In the 4H-SiC simulations considered here, the acceptor equation is the most relevant because incomplete ionisation is dominated by the p-type pillar.

Figures 13–14 show that, during the charging and discharging transients, the partially

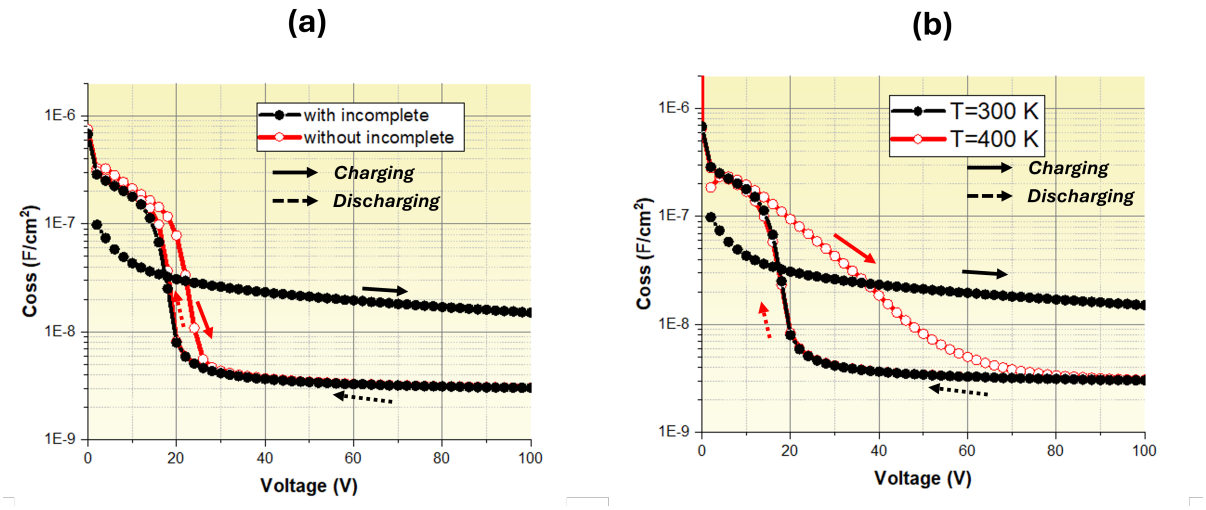

Figure 13: (a) Dynamic output-capacitance hysteresis for a 650 V 4H-SiC superjunction structure with and without incomplete ionisation model in the p-type pillar, obtained for $\epsilon = 0.5$, where the n- and p-pillars are geometrically symmetric. (b) Temperature dependence of the dynamic output capacitance.

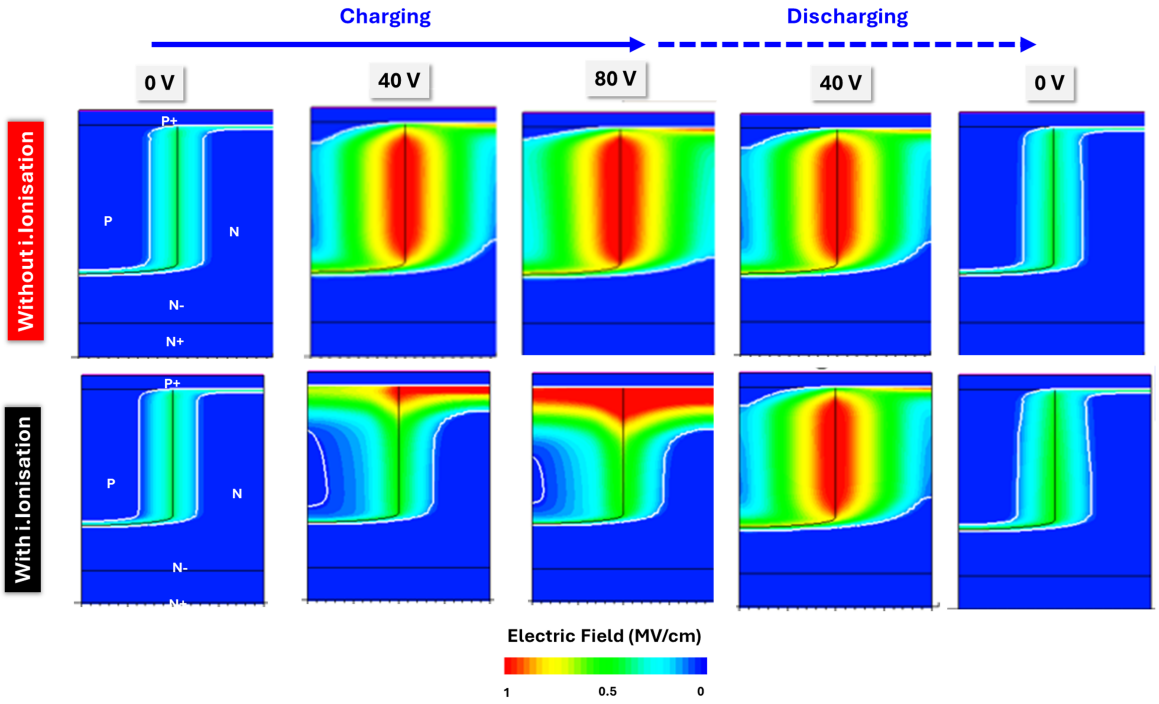

Figure 14: Electric-field evolution with and without incomplete ionisation during the charging and discharging phases corresponding to Fig. 13(a).

ionised p-type pillar causes the device to respond effectively as an n-rich structure when high voltage is applied during the charging phase. The discharging phase is less affected because the ionised dopant population and mobile carrier density begin to follow the applied voltage transient after the initial high-dV/dt excitation. This produces a strong asymmetry between the charging and discharging branches with and without incomplete ionisation. In some cases, the charging and discharging trajectories can intersect, leading to a substantial increase in hysteresis-related energy loss. In contrast to the silicon case considered in Section 3.1, higher temperature can reduce hysteresis in the 4H-SiC structure because it increases dopant ionisation and partially restores the intended charge-balance condition. This also implies that consecutive switching cycles can partially mitigate the hysteresis if the generated internal Joule heat increases the local junction temperature and improves acceptor ionisation.

These results indicate that hysteresis losses in wide-bandgap charge-balanced drift regions can be fundamentally stronger than in silicon if incomplete dopant ionisation is accounted for. This effect becomes particularly important when the capacitance contribution of the edge termination is comparable to that of the active area. In such cases, active-cell and termination dynamics should be analysed together. Graded profiles of the type discussed in Section 3.3 may provide a practical route to mitigate the effect by improving the robustness of the internal electric-field profile against dynamic charge imbalance.

3.5. Design Guidelines for Hysteresis Mitigation

The results presented above suggest several design guidelines for reducing output-capacitance hysteresis in charge-balanced drift regions.

First, the internal electric-field profile should be engineered not only for static breakdown-voltage capability, but also for dynamic charge redistribution. A perfectly flat electric-field profile is attractive from the perspective of the conventional BV–$R_{\mathrm{on,sp}}$ trade-off, but it can produce slow and asymmetric depletion-boundary motion during charging and discharging. Field profiles that avoid low-conductivity bottlenecks at the moving depletion boundaries can reduce the effective relaxation time and therefore lower the hysteresis energy.

Second, graded or sloped pillar doping can be used to improve charging–discharging symmetry. In the silicon superjunction structures considered here, a positive p-pillar slope, corresponding to higher p-type doping towards the bottom of the drift region, produces a bell-shaped electric-field profile and reduces hysteresis losses relative to the constant-doping case. This approach can also improve robustness against surface-charge perturbations and manufacturing-induced charge imbalance, although it must be co-optimised with the blocking-voltage margin.

Third, the cell pitch and doping concentration should not be scaled only according to static on-resistance requirements. Pitch reduction can improve $R_{\mathrm{on,sp}}$ up to the point where the JFET effect becomes dominant [4], but it also modifies the lateral depletion and carrier-reinjection dynamics. Even when the pillar doping is increased to maintain the total pillar charge, the resulting structure may exhibit larger hysteresis under fast voltage transients. Therefore, the E_{diss}–$R_{\mathrm{on,sp}}$ trade-off should be considered alongside the conventional BV–$R_{\mathrm{on,sp}}$ trade-off.

Fourth, wide-bandgap implementations require explicit treatment of the dynamic effect of dopant ionisation. In 4H-SiC superjunctions, partial ionisation of p-type pillars can shift the effective charge balance during transient operation and lead to stronger hysteresis than would be predicted under complete-ionisation assumptions. Temperature, dopant activation energy,

pillar doping, and edge-termination design should therefore be included in the optimisation of wide-bandgap charge-balanced devices.

Finally, the contribution of the edge termination should be included when translating active-cell design rules into practical devices. As the active die area is reduced, the termination capacitance and termination charge dynamics can become comparable to those of the active region. A hysteresis-robust design for a charge-balanced layer should therefore co-optimise the active superjunction cell, the graded pillar profile, and the edge termination to minimise hysteresis-related energy loss while maintaining adequate breakdown-voltage robustness.

4. Conclusions

The physical origin of output-capacitance hysteresis in vertical charge-balanced drift regions has been analysed using finite-element simulations of superjunction structures under fast charging and discharging transients. The results show that hysteresis is not solely a consequence of residual or stranded charge, but it is strongly influenced by the local electric field, carrier mobility, mobile carrier density, and conductivity at the moving depletion boundaries.

For silicon superjunction structures, the hysteresis energy increases with faster voltage transients and reduced carrier mobility, supporting the interpretation based on a local dielectric relaxation time. The simulations also show that charge-balance condition, cell pitch, and internal electric-field shape have a direct impact on the charging–discharging asymmetry. In particular, graded p-pillar profiles that produce a bell-shaped electric-field distribution can reduce hysteresis-related energy loss while maintaining a favourable $R_{\mathrm{on,sp}}$–BV trade-off.

For wide-bandgap charge-balanced structures, incomplete dopant ionisation introduces an additional source of dynamic charge imbalance. In the 4H-SiC case considered here, partial ionisation of the p-type pillar modifies the effective charge balance during the voltage transient and produces a substantially different hysteresis behaviour from that observed in silicon under complete-ionisation assumptions. This highlights the need to include incomplete ionisation, temperature dependence, and edge-termination capacitance when assessing hysteresis-related losses in wide-bandgap superjunction devices.

Overall, the analysis provides a physical framework for understanding and mitigating output-capacitance hysteresis in vertical charge-balanced power devices. The proposed design strategy is to engineer the internal electric-field and doping profiles so that carrier extraction and reinjection occur more symmetrically during charging and discharging. This approach can reduce hysteresis-related energy loss while preserving the advantages of charge-balanced drift regions for low on-state resistance and high blocking voltage.

References

[1] J. B. Fedison and M. J. Harrison, "C_{OSS} hysteresis in advanced superjunction MOSFETs," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 247–252, doi: 10.1109/APEC.2016.7467880.

[2] J. Roig and F. Bauwens, "Origin of anomalous C_{OSS} hysteresis in resonant converters with superjunction FETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 3092–3094, 2015, doi: 10.1109/TED.2015.2455072.

[3] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, "C_{OSS} measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 578–584, 2019, doi: 10.1109/TED.2018.2880952.

[4] H. Kang, N. Donato, and F. Udrea, "Effect of pillar ripple on static and dynamic trade-offs in superjunction MOSFETs," *IEEE Electron Device Letters*, vol. 41, no. 5, pp. 753–756, 2020, doi: 10.1109/LED.2020.2985203.

[5] Z. Lin, "Study on the intrinsic origin of output capacitor hysteresis in advanced superjunction MOSFETs," *IEEE Electron Device Letters*, vol. 40, no. 8, pp. 1297–1300, 2019, doi: 10.1109/LED.2019.2924512.

[6] Z. Lin, Z. Wang, W. Zeng, P. Li, S. Hu, J. Zhou, and F. Tang, "Electrothermal analysis of the charge–discharge related energy loss of the output capacitance in OFF-state superjunction MOSFETs," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4582–4586, 2021, doi: 10.1109/TED.2021.3099079.

[7] E. Van Brunt, G. Wang, J. Liu, V. Pala, B. Hull, J. Richmond, and J. Palmour, "Operation of 4H-SiC Schottky diodes at dV/dt values over 700 kV/μs," in *Proc. 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 67–70, doi: 10.1109/ISPSD.2016.7520779.

[8] M. Kah, N. Donato, and F. Udrea, "Dynamic effects of incomplete ionization in edge terminations of diamond power devices," *Diamond and Related Materials*, 2025, Art. no. 112994, doi: 10.1016/j.diamond.2025.112994.

[9] N. Donato and F. Udrea, "Static and dynamic effects of the incomplete ionization in superjunction devices," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4469–4475, 2018, doi: 10.1109/TED.2018.2867058.

[10] G. Samperi, A. Laudani, N. Salerno, A.Scuto, M. Ventimiglia, S. A. Rizzo "C_{OSS} losses in resonant converters," *Energies*, vol. 18, no. 13, Art. no. 3312, 2025, doi: 10.3390/en18133312.

[11] A. Raciti, S. A. Rizzo, N. Salerno, G. Susinni, R. Scollo, and A. Scuto, "Modeling the hysteresis power losses of the output parasitic capacitance in super junction MOSFETs," in *Proc. International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, 2018, pp. 527–532, doi: 10.1109/SPEEDAM.2018.8445347.

[12] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. M. Rivas-Davila, "An investigation into the causes of C_{OSS} losses in GaN-on-Si HEMTs," in *Proc. IEEE 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–7, doi: 10.1109/COMPEL.2019.8769661.

[13] N. Perera, A. Jafari, L. Nela, G. Kampitsis, M. S. Nikoo, and E. Matioli, "Output-capacitance hysteresis losses of field-effect transistors," in *Proc. IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, doi: 10.1109/COMPEL49091.2020.9265823.

[14] D. Bura, T. Plum, J. Baringhaus, and R. W. De Doncker, "Hysteresis losses in the output capacitance of wide bandgap and superjunction transistors," in *Proc. 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018.

[15] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "C_{OSS} related energy loss in power MOSFETs used in zero-voltage-switched applications," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 150–156, doi: 10.1109/APEC.2014.6803302.

[16] W. Saito, "Theoretical limits of superjunction considering with charge imbalance margin," in *Proc. IEEE 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2015, pp. 125–128, doi: 10.1109/ISPSD.2015.7123405.

[17] G. Deboy, D. Ahlers, H. Strack, M. Rueb, and H. Weber, "High-voltage semiconductor component," U.S. Patent US6630698B1, Oct. 7, 2003.

[18] M. Lades, W. Kaindl, N. Kaminski, E. Niemann, and G. Wachutka, "Dynamics of incomplete ionized dopants and their impact on 4H/6H-SiC devices," *IEEE Transactions on Electron Devices*, vol. 46, no. 3, pp. 598–604, 1999, doi: 10.1109/16.748884.

[19] K. Naydenov, N. Donato, and F. Udrea, "Operation and performance of the 4H-SiC junctionless FinFET," *Engineering Research Express*, vol. 3, no. 3, Art. no. 035008, 2021, doi: 10.1088/2631-8695/ac12bc.

[20] N. Donato, "Modelling and design of diamond power semiconductor devices," Ph.D. dissertation, University of Cambridge, Cambridge, U.K., 2019.