Physics-Based and Machine-Learning-Assisted Performance Mapping of Ultra-High-Voltage SiC IGBTs and MOSFETs Under Hard- and Soft-Switching Conditions

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***Abstract*— Ultra-high-voltage SiC IGBTs, SiC MOSFETs and series connection Si IGBT and SiC MOSFETs configurations are compared under hard- and soft-switching conditions using a self-consistent electrothermal framework combined with machine-learning-assisted device mapping. All electro-thermal input data are extracted from finite-element device simulations, so that the comparison is based on physics-derived models rather than simplified compact-model assumptions. Three different comparisons are considered. First, maximum-current capability maps are calculated to determine the highest current that each device technology can sustain before reaching the imposed thermal limit. Second, a deterministic electrothermal solver selects the minimum-loss feasible device at each operating point. Third, a machine-learning classifier trained from deterministic solutions is used to accelerate superior-device map generation, while deterministic correction is retained near device-transition boundaries. For the 20 kV voltage class considered here, the classifier-only stage reduces map-generation time by up to $3.8\times$ relative to the full deterministic map. When deterministic correction is applied near low-confidence and transition-boundary regions, the hybrid workflow achieves a $2.1\times$ speed-up excluding the one-time training cost.**

***Index Terms*—** Silicon carbide, SiC IGBT, SiC MOSFET, ultra-high-voltage power devices, electrothermal modelling, hard switching, soft switching, machine learning, surrogate modelling, power electronics, series connection, FEM modelling, ZVS.

I. Introduction

SiC IGBTs have been investigated for several decades, evolving from early 6H-SiC UMOS IGBTs and p-channel 4H-SiC IGBTs to later n-channel 4H-SiC devices based on planar, flip-type, free-standing, and waffle-substrate concepts [1]–[5]. Experimental demonstrations have extended SiC IGBTs and modules into the 10–27 kV voltage range, including 12 kV-class modules, 16 kV flip-type IE-IGBTs, 27 kV n-IGBTs, and 10 kV box-cell or waffle-substrate structures [6]–[9]. However, despite this progress, SiC IGBTs have not yet reached widespread commercial adoption, mainly due to challenges in carrier-lifetime engineering, backside processing, p-type contacts, bipolar degradation, edge termination, yield, and cost [10]. Furthermore, the transition from SiC MOSFETs to SiC IGBTs remains less clearly defined than the corresponding transition from Si MOSFETs to Si IGBTs. In principle, the conductivity modulation provided by a SiC IGBT can reduce conduction losses. However, this advantage is counterbalanced by the larger built-in voltage of 4H-SiC bipolar junctions (2.7 V at 300 K), which is substantially higher than that of silicon junctions (0.7 V at 300 K). As a result, the voltage class at which a SiC IGBT becomes favorable is expected to be higher than the voltage class at which a Si IGBT becomes superior to Si MOSFET.

The comparison is further complicated by the fact that ultra-high-voltage converter requirements can also be met using series-connected lower-voltage devices (also in modular configurations). Series-connected SiC MOSFETs may retain low switching losses and avoid bipolar charge storage, while series-connected Si IGBTs benefit from mature silicon processing and module technology. However, both approaches introduce additional active area, voltage-balancing requirements, and increased driving/control complexity. It is therefore not sufficient to compare only a monolithic SiC MOSFET and a monolithic SiC IGBT at a single current level.

Technology Computer-Aided Design (TCAD) simulations have also been used to optimise SiC IGBT cell designs by balancing on-state voltage, breakdown voltage, and switching loss across different topologies and design parameters [11]. However, converter-oriented comparisons between ultra-high-voltage SiC MOSFETs, SiC IGBTs, series-connected SiC MOSFETs, and series-connected Si IGBTs remain limited across broad switching-frequency, temperature, and current ranges. In this context, physics-based FEM modelling is essential because incomplete ionisation, anisotropic transport properties, oxide/semiconductor interface scattering, carrier recombination, and carrier-lifetime effects can all affect both the static and dynamic characteristics of SiC devices [12]–[17]. These effects are usually difficult to retain in compact, SPICE-type device models without extensive calibration over current, voltage, temperature, and switching conditions.

Machine-learning methods have recently been introduced in TCAD and power-electronics workflows to accelerate optimisation, prediction, and calibration tasks. Several recent examples include TCAD-trained models for SiC breakdown-voltage prediction, GaN HEMT current–voltage prediction, FinFET transfer-characteristic prediction, process-profile prediction, IGBT design optimisation from design-of-experiments datasets and SPICE-augmented parameter extraction [18]–[24]. ML methods have also been applied at converter level, for example to predict the efficiency of SiC- and GaN-based converters [25]. These approaches can be effective, but their efficacy depends strongly on the training data, the underlying physical models, and the range over which the model is used. In this paper, machine learning is therefore not used to replace the electrothermal solver, but to accelerate the generation of the device-selection map, with deterministic re-evaluation retained in low-confidence and transition regions.

The present study addresses this comparison using a physics-based, machine-learning-assisted workflow for ultra-

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TABLE I

DRIFT-REGION PARAMETERS USED FOR THE CONSIDERED DEVICE VOLTAGE CLASSES (1.2 KV-20 KV) BASED ON THE IMPACT IONISATION INTEGRAL.

Device	BV **(kV)**	**Drift thickness** (μ**m**)	**Doping** (cm^{-3})
Silicon IGBT	6.5	500	8.5×10^{12}
4H-SiC MOSFET/IGBT	1.2	10	1.0×10^{16}
4H-SiC MOSFET/IGBT	3.3	30	7.0×10^{15}
4H-SiC MOSFET/IGBT	6.5	60	3.0×10^{15}
4H-SiC MOSFET/IGBT	10	100	1.0×10^{15}
4H-SiC MOSFET/IGBT	15	120	8.0×10^{14}
4H-SiC MOSFET/IGBT	20	150	5.0×10^{14}

high-voltage SiC MOSFETs and SiC IGBTs under equivalent converter-level constraints. Hard- and soft-switching operation, thermal limits, maximum-current capability, deterministic loss minimisation, and series-connected alternatives are treated within the same modelling approach. Section II describes the device geometries and finite-element simulation setup. Section III presents the electrothermal and ML-assisted mapping methods. Section IV discusses the current-capability maps, superior-device maps, and comparison with a compact-model-based workflow. Section V concludes the paper.

II. TCAD MODELLING

A. Finite-Element Simulation Framework

Mixed-mode finite-element simulations were performed in TCAD to extract both the static and dynamic characteristics of the investigated devices. Switching losses were obtained using a double-pulse-test (DPT) circuit, while the output characteristics were extracted using a slow voltage-ramp transient with a ramp rate of approximately $1\ \mathrm{V/s}$, such that the resulting characteristics are representative of quasi-static operation. The DPT circuit and the relevant simulation parameters are shown in Fig. 1.

The device structures (modeled just with their active cell) considered in this work are shown in Fig. 2. The drift-region parameters for each device configuration are summarised in Table I. The SiC MOSFET (Fig. 2(a)) and SiC IGBT (Fig. 2(b)) cells use the same cell pitch of $14\ \mu\mathrm{m}$ to ensure a consistent geometrical comparison. A uniformly doped epi-type JFET region with a thickness of $2\ \mu\mathrm{m}$ and a donor concentration of $2 \times 10^{16}\ \mathrm{cm}^{-3}$ is used in both SiC unipolar and bipolar structures. For the SiC MOSFET, the n-buffer layer is $1\ \mu\mathrm{m}$ thick and doped at $1 \times 10^{18}\ \mathrm{cm}^{-3}$, whereas for the SiC IGBT the buffer layer is $2\ \mu\mathrm{m}$ thick and doped at $1 \times 10^{17}\ \mathrm{cm}^{-3}$. The SiC IGBT further includes a $2\ \mu\mathrm{m}$ p-anode doped at $5 \times 10^{17}\ \mathrm{cm}^{-3}$ and a $1\ \mu\mathrm{m}$ p^+ collector doped at $1 \times 10^{19}\ \mathrm{cm}^{-3}$.

A $30\ \mathrm{nm}$ $\mathrm{SiO_2}$ layer is used as the gate oxide for the SiC devices. The gate electrode is represented by n-type polysilicon with a donor concentration of $1 \times 10^{19}\ \mathrm{cm}^{-3}$. The lateral dimensions of the n^+ source and p^+ body-contact regions are both set to $1\ \mu\mathrm{m}$. Uniform doping profiles are assumed throughout the device structures, except near the front-side p-body and channel regions, where implanted profiles are used based on calibrated 4H-SiC process- and device-modelling assumptions [12]–[16].

For the Si IGBT structure shown in Fig. 2(c), the same $14\ \mu\mathrm{m}$ cell pitch is assumed. The cell design includes multiple dummy-emitter trenches, representative of recent-generation $6.5\ \mathrm{kV}$ trench Si IGBT technologies. An enhancement layer, which improves carrier confinement and plays a role analogous to the JFET region in the SiC devices, is included with a thickness of $2\ \mu\mathrm{m}$ and a doping concentration of $3 \times 10^{15}\ \mathrm{cm}^{-3}$. The trench depth is $4\ \mu\mathrm{m}$ and the gate oxide thickness is $75\ \mathrm{nm}$. The backside n-buffer and p-anode regions are obtained from process simulations.

The resulting output characteristics are shown in Fig. 3 and Fig. 4, highlighting the voltage-class dependence of the MOSFET–IGBT crossover and the 20 kV comparison used in the subsequent loss analysis.

Incomplete ionisation is included for the 4H-SiC devices in order to account for the deep dopant levels associated with donor and acceptor species [12], [13]. This is implemented using a trap-based dopant model, which also accounts for the corresponding recombination level. Carrier lifetime is modelled using a combination of Auger, radiative, and Shockley–Read–Hall (SRH) recombination mechanisms [16], [17]. In 4H-SiC, the peak SRH lifetime τ is treated as a variable parameter and is assumed to be identical for electrons and holes. Its temperature dependence is represented as

$$\tau_m(T) = \tau_{0,m} \left(\frac{T}{300\ \mathrm{K}} \right)^{\alpha_{\tau,m}}, \tag{1}$$

where m denotes the semiconductor material. For 4H-SiC, $\alpha_{\tau,\mathrm{4H\text{-}SiC}} = 1.7$, consistent with the experimentally reported increase of carrier lifetime with temperature in 4H-SiC epitaxial layers [17]. For Si, $\alpha_{\tau,\mathrm{Si}} = 1.5$ is used. In the Si IGBT, the peak electron and hole SRH lifetimes, $\tau_{0,n}$ and $\tau_{0,p}$, are set to $30\ \mu\mathrm{s}$ and $10\ \mu\mathrm{s}$, respectively, together with standard material parameters for silicon and benchmark 6.5 kV Si IGBT structures [26], [27]. The SiC channel mobility model follows [14] and includes the combined contributions of Coulomb scattering, surface acoustic phonon scattering, surface roughness scattering, and bulk mobility. Other standard 4H-SiC material parameters, including the bandgap, effective density of states, anisotropic transport parameters, capture cross sections, bandgap narrowing, and impact-ionisation coefficients, are taken from established 4H-SiC modelling references [12], [13], [16]. The drift-region thickness and doping concentration are scaled by assuming avalanche impact ionisation as the dominant breakdown mechanism. Anisotropic impact-ionisation parameters are used for 4H-SiC. Edge termination regions and gate pads are not included in the simulated structures. All single-device configurations are normalised to an active area of $1\ \mathrm{cm}^2$. The device classes considered in this work are summarised in Table I. For the $20\ \mathrm{kV}$ class comparison, both the series-connected Si IGBT and the series-connected SiC MOSFET configurations are modelled as three 6.5 kV devices connected in series. The total active area of these series-connected configurations is therefore assumed to be three times larger than that of a single-device configuration.

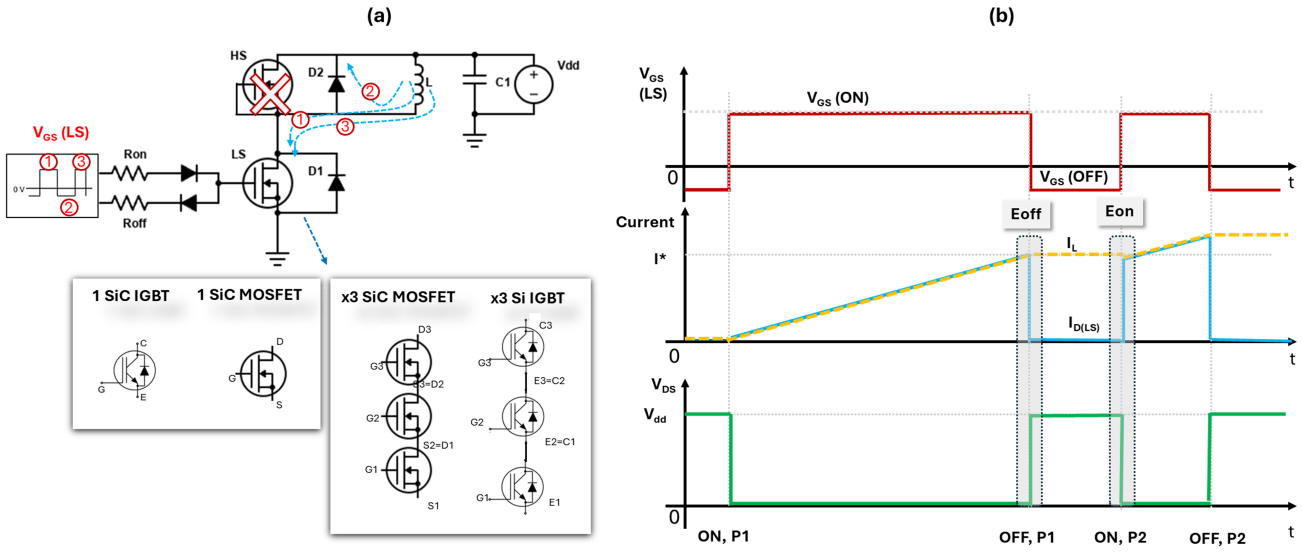

Fig. 1. (a) Double-pulse-test circuit used for the mixed-mode finite-element simulations. The high-side switch is replaced by an ideal diode so that the extracted switching losses correspond only to the low-side device under test. The four device configurations analysed in this work are used as the low-side switch. (b) Representative DPT waveforms indicating the time intervals used for the extraction of turn-on and turn-off switching energies. The simulation parameters are $R_{\mathrm{on}} = 10\ \Omega$, $R_{\mathrm{off}} = 1\ \Omega$, $C_1 = 10\ \mathrm{pF}$, $V_{\mathrm{DD}} = BV/1.6$, $V_{\mathrm{GS,on}} = 15\ \mathrm{V}$, and $V_{\mathrm{GS,off}} = -5\ \mathrm{V}$. Diode D2 is modelled as ideal. D1 represents the internal body diode of the MOSFET and is absent in the IGBT case.

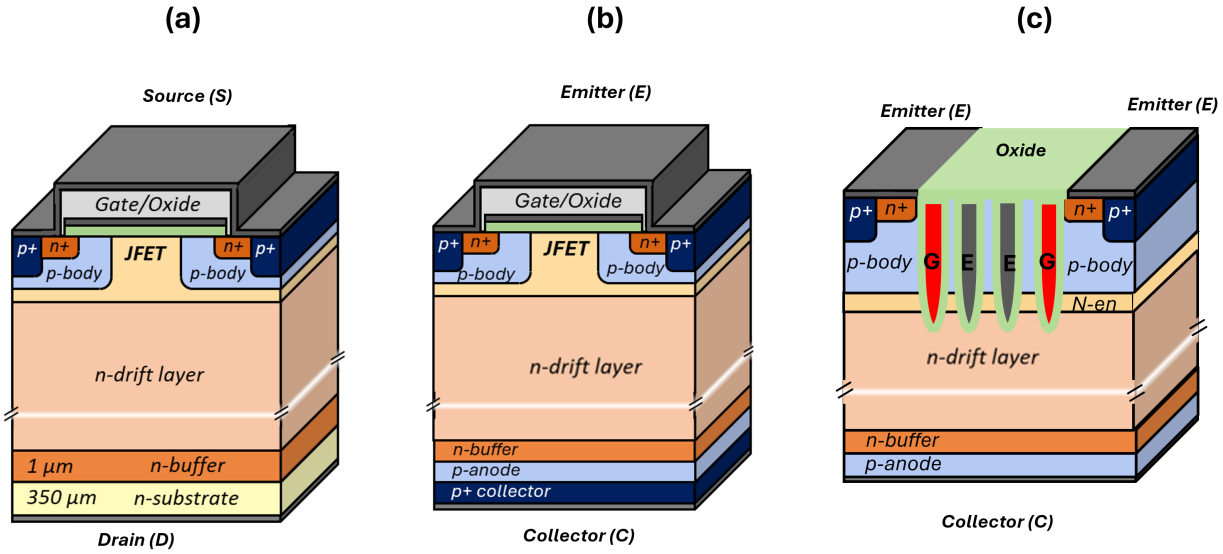

Fig. 2. (a) Schematic active-cell view of the SiC MOSFET, (b) SiC IGBT, and (c) Si IGBT used in this work.

In total, more than 2000 mixed-mode finite-element simulations were performed to generate the training dataset used in this work. The extracted quantities include the on-state voltage V_{on}, turn-on energy E_{on}, and turn-off energy E_{off} over the investigated current range and for junction temperatures between 300 K and 448 K. Switching energies are extracted by integrating the instantaneous switching power over the interval in which the drain/collector voltage and current transition between 10% and 90% of their steady-state values, following standard JEDEC-standard loss-extraction convention and recent wide-bandgap switching-loss methodologies [16], [28]. While the actual switching losses depend on the selected circuit topology, so it can vary for different gate resistors and parasitic inductances, the objective here is to provide a broad technology comparison under consistent (and identical) parasitic assumptions.

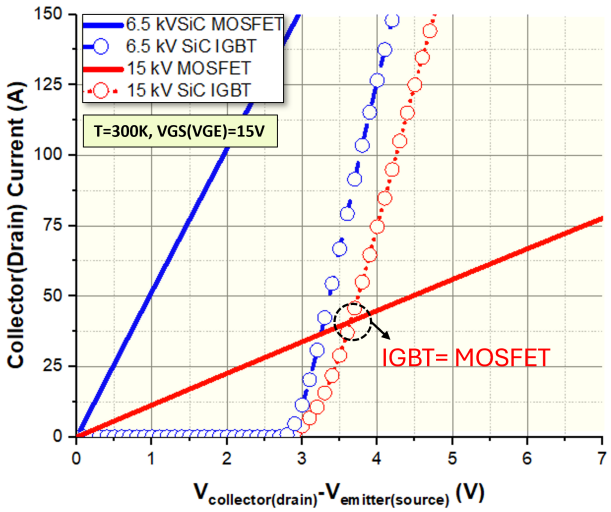

Fig. 3. Output characteristics at $T = 300$ K for the SiC IGBT and SiC MOSFET, highlighting the shift of the crossover point towards lower current at higher voltage classes. τ_0 for SiC IGBT is $1\ \mu$s

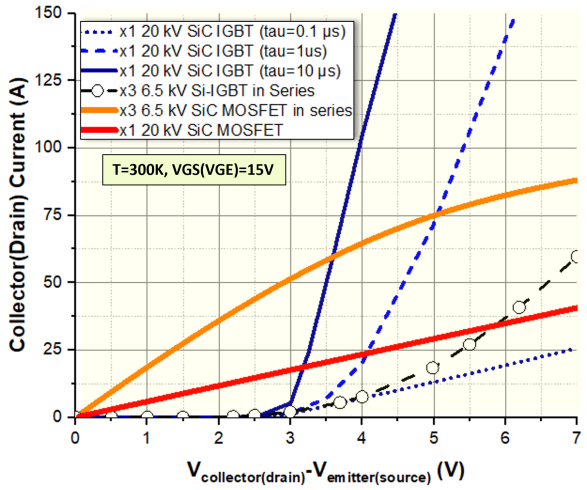

Fig. 4. Comparison of output characteristics at $T = 300$ K for the 20 kV voltage class.

III. Physics-Based and ML-Surrogate Loss Modelling

Three complementary calculations are used for the device comparison. The first extracts a maximum-current capability surface, denoted as I^*, for each technology and identifies the highest current that can be thermally sustained at a selected junction-temperature limit. The second performs a deterministic self-consistent electrothermal comparison and selects the feasible device with the lowest total loss. The third uses a machine-learning classifier, implemented as a bagged decision-tree ensemble, trained from deterministic electrothermal solutions to accelerate the generation of superior-device maps over dense operating grids.

The candidate device set can be written as

$$\mathcal{K} = \{k_1, k_2, \ldots, k_N\}, \tag{2}$$

where each candidate k represents one device architecture, such as a single SiC MOSFET, a SiC IGBT with a given carrier lifetime, a series connection of SiC MOSFETs, or a series connection of Si IGBTs.

Each device candidate is described by tabulated electrical data:

$$V_{\mathrm{on},k}(I,T), \qquad E_{\mathrm{on},k}(I,T), \qquad E_{\mathrm{off},k}(I,T), \tag{3}$$

where I is the device current and T is the temperature at which the electrical data are evaluated.

The main operating variables are the device current I, switching frequency f_{sw}, duty cycle D, heatsink temperature T_{sink}, ambient temperature T_{amb}, voltage class, and device thermal resistance $R_{\mathrm{th},k}$.

For all approaches, the total device loss is decomposed as

$$P_{\mathrm{tot},k} = P_{\mathrm{cond},k} + P_{\mathrm{sw},k}. \tag{4}$$

The conduction loss is calculated from the on-state output characteristics:

$$P_{\mathrm{cond},k} = D\, V_{\mathrm{on},k}(I,T)\, I. \tag{5}$$

The switching loss is calculated from the switching energy per pulse:

$$P_{\mathrm{sw},k} = f_{\mathrm{sw}} E_{\mathrm{tot},k}(I,T). \tag{6}$$

Two switching-energy definitions are considered. For hard-switching operation,

$$E^{\mathrm{hard}}_{\mathrm{tot},k} = E_{\mathrm{on},k} + E_{\mathrm{off},k}, \tag{7}$$

while for the soft-switching case considered here(i.e., zero voltage switching (ZVS)), the turn-on energy is assumed to be strongly reduced, and the switching energy is approximated by

$$E^{\mathrm{soft}}_{\mathrm{tot},k} = E_{\mathrm{off},k}. \tag{8}$$

Therefore, the total loss can be written as

$$P_{\mathrm{tot},k} = D\, V_{\mathrm{on},k}(I,T)\, I + f_{\mathrm{sw}} E_{\mathrm{tot},k}(I,T). \tag{9}$$

The same loss expression is used in the maximum-current calculation, the deterministic electrothermal solver, and the machine-learning class-assignment algorithm. The difference between the approaches lies in how the temperature is treated and in whether the device comparison is performed by direct deterministic evaluation or by a trained surrogate model.

A. Thermal Resistance and Device Stack

Each device candidate is assigned a steady-state thermal resistance using a simplified multilayer package model with lateral heat spreading. The model assumes single-side cooling and a two-dimensional heat source originating from the active semiconductor region, following chip-size and thermal-limit treatments typically used for wide- and ultra-wide-bandgap power devices, as shown in [29]. The package includes the semiconductor(semi), die attach (attach), DBC top copper

(Cu,top), AlN ceramic isolation (cer), DBC bottom copper (Cu,bottom), copper baseplate(bp), and the external cooling (conv).

The total thermal resistance of device candidate k is

$$R_{\mathrm{th},k} = R_{\mathrm{semi},k}+R_{\mathrm{attach}}+R_{\mathrm{Cu,top}}+R_{\mathrm{cer}}+R_{\mathrm{Cu,bot}}+R_{\mathrm{bp}}+R_{\mathrm{conv}}. \tag{10}$$

For each conductive layer, the thermal resistance is calculated using a 45° heat-spreading approximation as

$$R_i = \frac{t_i}{k_i A_i}, \qquad A_i = \frac{A_{\mathrm{in}} + \left(\sqrt{A_{\mathrm{in}}} + 2t_i\right)^2}{2}, \tag{11}$$

where t_i and k_i are the thickness and thermal conductivity of layer i, respectively, and A_i is the layer-averaged spreading area. The input footprint A_{in} is the active-device area for the first layer and the expanded output footprint of the previous layer for all subsequent layers.

The convective resistance at the external cooling boundary is

$$R_{\mathrm{conv}} = \frac{1}{hA_{\mathrm{plate}}}, \tag{12}$$

where h is the heat-transfer coefficient and A_{plate} is the final heat-spreading area at the cooling boundary.

The semiconductor thickness is device dependent. For the SiC MOSFET, the semiconductor thickness is taken as the sum of the SiC drift-region thickness and the SiC substrate thickness. For the SiC IGBT, only the voltage-supporting SiC region is included. For the series-connected Si IGBT case, the semiconductor thickness is taken as the total Si die thickness.

The AlN ceramic thickness is scaled with the representative blocking voltage:

$$t_{\mathrm{AlN}} = \frac{S_{\mathrm{F}} BV}{E_{\mathrm{AlN}}}, \tag{13}$$

where $S_{\mathrm{F}} = 1.2$ is the insulation safety factor and $E_{\mathrm{AlN}} = 20\ \mathrm{kV/mm}$ is the assumed AlN dielectric strength. For the 20 kV case, this gives $t_{\mathrm{AlN}} = 1.2\ \mathrm{mm}$.

The main thermal-stack parameters used in the comparison are summarised in Table II. These values define a consistent reference package and cooling condition for comparing the relative electrothermal behaviour of the candidate technologies. They are not intended to represent a fully optimised module design. It is worth noting that the thermal impedance is used as a first order approximation.

The resulting device-specific thermal resistance $R_{\mathrm{th},k}$ is used in both the deterministic electrothermal solver and the maximum-current capability calculation. In the steady-state comparisons, duty-cycle dependence is introduced through the average conduction-loss term; any effective thermal scaling used for the I^* envelope methodology is applied only within that calculation and is not double counted in the overall loss estimation.

TABLE II

MAIN THERMAL-STACK PARAMETERS USED IN THE ELECTROTHERMAL COMPARISON. VALUES FOR THE 20 KV VOLTAGE CLASS ARE SHOWN.

Parameter	Symbol	Value
Cooling configuration	–	Single-side cooled
Heat-spreading model	–	45° spreading
Representative SiC voltage class	BV	20 kV
SiC drift thickness	$t_{\mathrm{drift,SiC}}$	150 μm
SiC substrate thickness	$t_{\mathrm{sub,SiC}}$	200 μm
Series Si IGBT die thickness	$t_{\mathrm{die,Si}}$	650 μm
SiC thermal conductivity	k_{SiC}	300 $\mathrm{W\,m^{-1}K^{-1}}$
Si thermal conductivity	k_{Si}	148 $\mathrm{W\,m^{-1}K^{-1}}$
Die-attach thermal conductivity	k_{attach}	60 $\mathrm{W\,m^{-1}K^{-1}}$
DBC copper thickness	t_{Cu}	0.3 mm
Copper thermal conductivity	k_{Cu}	400 $\mathrm{W\,m^{-1}K^{-1}}$
AlN thermal conductivity	k_{AlN}	150 $\mathrm{W\,m^{-1}K^{-1}}$
AlN dielectric strength	E_{AlN}	20 kV/mm
AlN safety factor	S_{F}	1.2
AlN ceramic thickness	t_{AlN}	1.2 mm
Copper baseplate thickness	t_{base}	10 mm
Heat-transfer coefficient	h	5000 $\mathrm{W\,m^{-2}K^{-1}}$
Thermal reference temperature	T_{sink}	300 K
Maximum junction temperature	$T_{\mathrm{j,max}}$	448 K

B. Maximum-Current Capability Calculation

The first comparison metric is the maximum thermally sustainable current, denoted as I^*. For each device candidate k, switching frequency f_{sw}, and duty cycle D, I^* is defined as the highest current for which the device remains below the imposed junction-temperature limit. The calculation therefore solves

$$I_k^* = \max_I \left\{ I : T_{\mathrm{j},k}\left(I, f_{\mathrm{sw}}, D\right) \le T_{\mathrm{j,max}} \right\}. \tag{14}$$

For a given current estimate, the total loss is calculated as

$$P_{\mathrm{tot},k} = D\,V_{\mathrm{on},k}(I,T)\,I + f_{\mathrm{sw}} E_{\mathrm{tot},k}(I,T), \tag{15}$$

where $E_{\mathrm{tot},k} = E_{\mathrm{on},k} + E_{\mathrm{off},k}$ for hard switching and $E_{\mathrm{tot},k} = E_{\mathrm{off},k}$ for the ZVS approximation. The electrical quantities in this calculation are evaluated at the junction-temperature estimate used in the thermal balance, using the same temperature interpolation procedure described in Section III-C. The corresponding junction temperature is obtained from

$$T_{\mathrm{j},k} = T_{\mathrm{sink}} + R_{\mathrm{th},k} P_{\mathrm{tot},k}. \tag{16}$$

The limiting current I_k^* is then found by increasing or solving for the current at which

$$T_{\mathrm{j},k} = T_{\mathrm{j,max}}. \tag{17}$$

Repeating this calculation over the f_{sw}–D grid gives the maximum-current capability surface for each device technology. Unlike the deterministic superior-device map, which ranks all feasible devices at a prescribed operating current, the I^* map identifies the thermal current envelope of each individual candidate with ultra-low computational cost.

C. Deterministic Self-Consistent Electrothermal Loss Comparison

The deterministic electrothermal calculation is used as the reference method for device ranking. In contrast to the I^* capability calculation, all device candidates are evaluated at the

same prescribed operating point, defined by current, switching frequency, duty cycle, and heatsink temperature.

For each device k, the on-state voltage and switching energies are evaluated at the instantaneous estimate of junction temperature. The tabulated electrical data are first interpolated over current using shape-preserving piecewise cubic interpolation. A linear temperature interpolation is then applied between two consecutive available temperature data, T_1 and T_2, according to

$$X_k(I,T_j) = X_k(I,T_1) + \frac{T_j - T_1}{T_2 - T_1}\left[X_k(I,T_2) - X_k(I,T_1)\right], \tag{18}$$

where $X_k \in \{V_{\mathrm{on},k}, E_{\mathrm{on},k}, E_{\mathrm{off},k}\}$.

The self-consistent junction temperature is obtained from the fixed-point condition

$$T_{\mathrm{j},k} = T_{\mathrm{sink}} + R_{\mathrm{th},k} P_{\mathrm{tot},k}\left(I, f_{\mathrm{sw}}, D, T_{\mathrm{j},k}\right). \tag{19}$$

At iteration n, the total loss is evaluated as

$$P_{\mathrm{tot},k}^{(n)} = D V_{\mathrm{on},k}\left(I, T_{\mathrm{j},k}^{(n)}\right) I + f_{\mathrm{sw}} E_{\mathrm{tot},k}\left(I, T_{\mathrm{j},k}^{(n)}\right), \tag{20}$$

where $E_{\mathrm{tot},k}$ is selected according to the hard- or soft-switching case.

The junction temperature is then updated using relaxed fixed-point iteration:

$$T_{\mathrm{j},k}^{(n+1)} = (1-\alpha) T_{\mathrm{j},k}^{(n)} + \alpha\left[T_{\mathrm{sink}} + R_{\mathrm{th},k} P_{\mathrm{tot},k}^{(n)}\right]. \tag{21}$$

In this work, $\alpha = 0.45$ is used. The iteration is stopped when the change in junction temperature is below $\varepsilon_T = 10^{-3}$ K.

After convergence, the conduction, switching, and total losses are

$$\begin{aligned} P_{\mathrm{cond},k} &= D\, V_{\mathrm{on},k}(I, T_{\mathrm{j},k})\, I, \\ P_{\mathrm{sw},k} &= f_{\mathrm{sw}} E_{\mathrm{tot},k}(I, T_{\mathrm{j},k}), \\ P_{\mathrm{tot},k} &= P_{\mathrm{cond},k} + P_{\mathrm{sw},k}. \end{aligned} \tag{22}$$

A device is considered feasible only if the electrothermal iteration converges, the required current lies within the valid interpolation range, and the final junction temperature remains below the imposed limit $T_{\mathrm{j,max}}$. The deterministic superior device is then selected from the feasible set as

$$k_{\mathrm{opt}} = \arg\min_{k \in \mathcal{K}_{\mathrm{feas}}} P_{\mathrm{tot},k}. \tag{23}$$

The loss margin between the best and second-best feasible devices is also stored:

$$\Delta P = P_{\mathrm{tot,second}} - P_{\mathrm{tot,best}}. \tag{24}$$

Large ΔP indicates that the selected device is robustly superior, whereas small ΔP identifies transition regions where small changes in duty cycle, switching frequency, thermal resistance, or electrical data could alter the winner.

The deterministic calculation is repeated over the full I–D–f_{sw} operating grid. At each grid point, the stored outputs include the winning device, the winning-device loss, the converged junction temperature, the loss margin, and the feasibility status of every candidate.

D. ML-Assisted Superior-Device Mapping

The reference device selection is obtained from the deterministic electrothermal calculation at each operating point. For a prescribed sink temperature and SiC IGBT carrier-lifetime setting, all candidate devices are evaluated and the feasible device with the lowest total loss is selected. A full deterministic sweep of the operating space is costly, since each device requires a self-consistent solution of electrical loss and junction temperature. The total number of deterministic candidate-device evaluations is

$$N_{\mathrm{eval}} = N_I N_D N_f N_{\mathrm{dev}}, \tag{25}$$

where N_I, N_D, and N_f are the numbers of current, duty-cycle, and switching-frequency points, respectively, and N_{dev} is the number of candidate devices.

The electrical quantities used in the electrothermal calculation are extracted from a TCAD-derived database sampled on a coarser current grid. This reduced sampling is necessary because transient TCAD simulations become expensive when repeated across several blocking-voltage classes, temperature conditions, and SiC IGBT carrier-lifetime values. The extracted $V_{\mathrm{on}}(I,T)$, $E_{\mathrm{on}}(I,T)$, and $E_{\mathrm{off}}(I,T)$ characteristics are therefore interpolated inside the electrothermal solver and evaluated on a denser grid for system-level mapping and classifier training. In this work, the dense mapping grid is defined by

$$N_I = 45, \qquad N_D = 25, \qquad N_f = 55. \tag{26}$$

This gives

$$N_{\mathrm{op}} = N_I N_D N_f = 61\,875 \tag{27}$$

operating points for each temperature and lifetime condition. The increased map resolution should therefore be interpreted as a denser system-level evaluation of interpolated TCAD-derived characteristics, not as an increase in the number of independent TCAD simulations. This resolution is useful near device-transition regions, where the preferred technology can change with current, duty cycle, switching frequency, temperature, or SiC IGBT carrier lifetime.

In the ML-assisted workflow, the full dense deterministic map is not computed first. Instead, the electrothermal solver is run only at a sampled subset of the operating space to provide reference device labels. These labels are then used to train a classifier for the dense map, while deterministic re-evaluation is retained for low-confidence points and regions close to device transitions.

For each prescribed temperature and lifetime condition, the classifier input vector is

$$\mathbf{x} = \left[I,\, \log_{10}(f_{\mathrm{sw}}),\, D\right], \tag{28}$$

where $\log_{10}(f_{\mathrm{sw}})$ is used because the switching-frequency range spans several decades. The supervised-learning target is the deterministic optimum device class,

$$y = k_{\mathrm{opt}}, \tag{29}$$

where k_{opt} is the feasible candidate device with the lowest total loss from the deterministic electrothermal calculation. The class $y = 0$ is reserved for points at which no candidate satisfies the imposed thermal constraint.

Training samples are drawn uniformly in current and duty cycle, and uniformly in $\log_{10}(f_{\mathrm{sw}})$. At each sampled point, all candidate devices are evaluated and the feasible minimum-loss device is assigned as the reference class. A bagged decision-tree ensemble classifier is then trained to approximate this selection rule,

$$\hat{k}_{\mathrm{opt}} = g(\mathbf{x}). \tag{30}$$

A classifier-only map can misplace narrow transition regions between competing devices, especially where the loss difference between the best and second-best candidates is small. For this reason, deterministic correction is applied where the classifier is less reliable. The classifier confidence is defined as

$$C(\mathbf{x}) = \max_k p_k, \tag{31}$$

where p_k is the classifier score associated with class k. Points satisfying

$$C(\mathbf{x}) < C_{\mathrm{th}}, \qquad C_{\mathrm{th}} = 0.88, \tag{32}$$

are re-evaluated deterministically. Additional correction points are selected near predicted device-transition boundaries, identified from changes in the predicted superior-device class between neighbouring grid points. To preserve most of the computational benefit, the corrected fraction is capped as

$$\frac{|\mathcal{C}|}{N_{\mathrm{op}}} \le f_{\mathrm{corr,max}}, \qquad f_{\mathrm{corr,max}} = 0.25, \tag{33}$$

where $\mathcal{C}$ is the set of operating points selected for deterministic correction. The final hybrid superior-device map uses deterministic labels in the correction set and classifier predictions elsewhere,

$$k_{\mathrm{hyb}}(\mathbf{x}) = \begin{cases} k_{\mathrm{det}}(\mathbf{x}), & \mathbf{x} \in \mathcal{C}, \\ \hat{k}_{\mathrm{opt}}(\mathbf{x}), & \mathbf{x} \notin \mathcal{C}, \end{cases} \tag{34}$$

where $k_{\mathrm{det}}(\mathbf{x})$ is the deterministic electrothermal selection and $\hat{k}_{\mathrm{opt}}(\mathbf{x})$ is the classifier-predicted optimum device class.

The deterministic part of the hybrid workflow requires

$$N_{\mathrm{det,hyb}} = N_{\mathrm{train}} + N_{\mathrm{val}} + |\mathcal{C}|, \tag{35}$$

operating points to be solved deterministically, where N_{train}, N_{val}, and $|\mathcal{C}|$ are the numbers of training, validation, and correction points, respectively. Since all candidate devices are evaluated at each such point, the common factor N_{dev} cancels in the approximate speed-up estimate. Treating the classifier prediction time separately, the reduction in deterministic evaluations is estimated as

$$S_{\mathrm{hyb}} \approx \frac{N_{\mathrm{op}}}{N_{\mathrm{train}} + N_{\mathrm{val}} + |\mathcal{C}|}. \tag{36}$$

The hybrid map therefore keeps the electrothermal calculation as the reference for training and correction, but avoids running the full self-consistent device comparison at every point of the dense grid.

IV. Results

A. Maximum-Current I^* Capability Map

Figures 5 and 6 summarise the maximum-current capability maps for the 20 kV voltage class. Figure 5(a) shows the three-dimensional map of the maximum allowable current, I^*, as a function of switching frequency and duty cycle for a selected carrier lifetime, while Fig. 5(b) reports the corresponding cutline at $D = 0.5$. In this case, zero-voltage-switching (ZVS) operation is assumed, so that turn-on losses are minimised and the comparison is mainly governed by conduction and turn-off losses.

Under ZVS conditions, the advantage of the SiC IGBT is evident, primarily because of its lower conduction loss in the low- and medium-frequency ranges (¡ 10 kHz). This advantage becomes less pronounced at low duty cycle and low current, where the SiC MOSFET, for the same active area, becomes increasingly competitive. Over a wide frequency range, approximately from 100 Hz to 20 kHz, the maximum allowable current of the SiC IGBT is nearly twice that of the SiC MOSFET. When turn-on losses are included, as shown in Fig. 6, the crossover point between the two device architectures shifts below 1 kHz. For the $D = 0.5$ cutline, an additional crossover is observed between the SiC IGBT cases with carrier lifetimes of 1 μs and 0.1 μs.

The inclusion of turn-on losses reduces the peak value of I^* from approximately 100 A to below 90 A. In contrast to the ZVS case, the SiC IGBT curves no longer exhibit an extended plateau; instead, I^* decreases markedly from tens of hertz to a few kilohertz. The 0.1 μs SiC IGBT case (where conductivity modulation is weak) exhibits a performance close to that of the SiC MOSFET over most of the investigated frequency range. The advantage of the SiC IGBT also becomes less significant at lower voltage classes, such as 6.5 kV (lower voltage classes are not shown here). In this case, the SiC MOSFET achieves a substantially higher maximum current, reaching approximately 120 A in both the full hard-switching and ZVS scenarios. By contrast, the SiC IGBT remains below the SiC MOSFET over the entire frequency range, as shown in Fig. 7.

A further comparison is performed at the 20 kV voltage class between the monolithic SiC MOSFET, the SiC IGBT, a series connection of three 6.5 kV SiC MOSFETs, and a series connection of three 6.5 kV Si IGBTs, as described in Section III. Under ZVS conditions, the SiC IGBT outperforms the other technologies over a broad operating range. The series-connected Si IGBT solution shows the poorest performance, with a maximum allowable current below 30 A over the entire frequency range. Conversely, the series-connected SiC MOSFET solution offers improved performance at higher switching frequencies and lower current levels. These ZVS and hard-switching comparisons are shown in Figs. 8 and 9, respectively.

It should be noted that series-connected devices generally require additional voltage margin, which is not included in

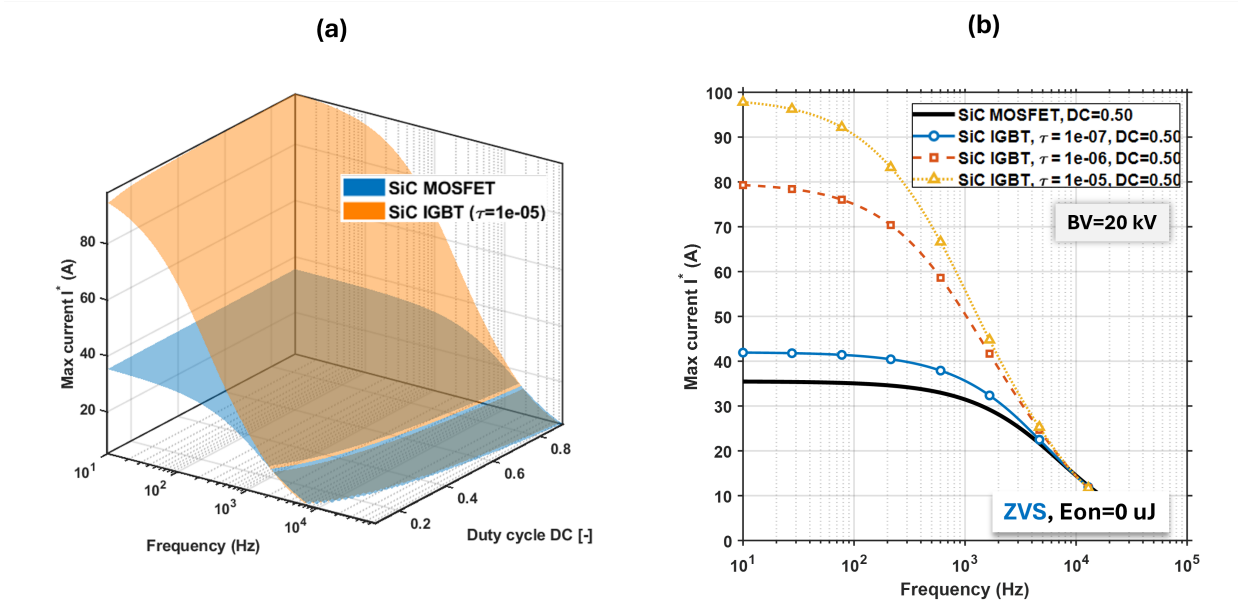

Fig. 5. (a) Three-dimensional maximum-current map for the 20 kV SiC MOSFET and SiC IGBT comparison. (b) Cutline at a fixed duty cycle of $D = 0.5$. ZVS operation is assumed for this calculation.

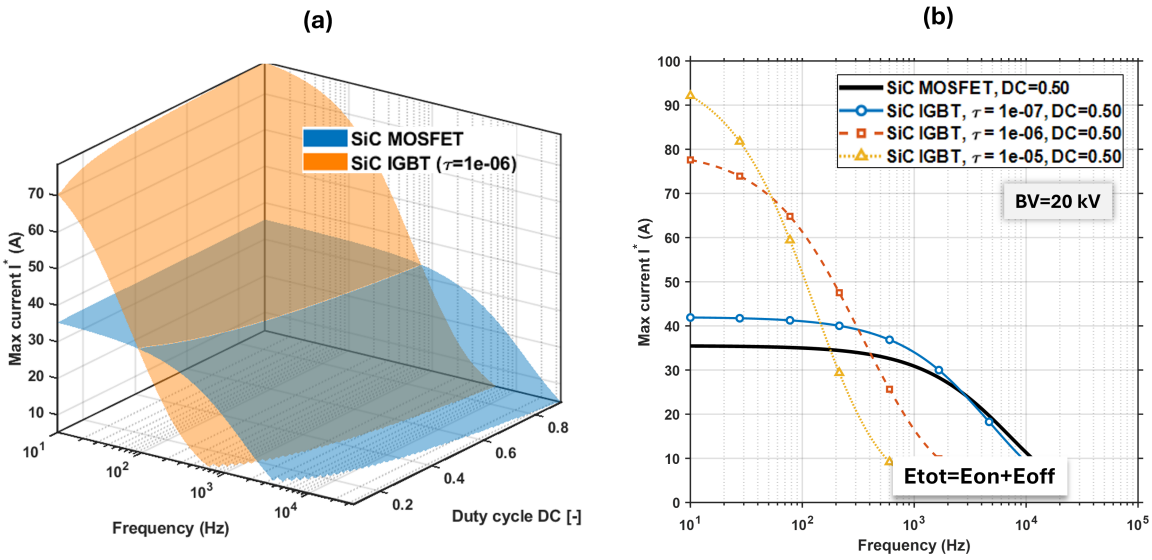

Fig. 6. (a) Three-dimensional maximum-current map for the 20 kV SiC MOSFET and SiC IGBT comparison. (b) Cutline at a fixed duty cycle of $D = 0.5$. Full hard-switching losses are included in this calculation.

the present study. Furthermore, voltage imbalance and unequal switching-energy sharing among series-connected devices can increase the effective switching losses in practical converter operation. These effects could be incorporated into the present modelling framework through an additional correction factor, although such results are not reported here.

B. Deterministic and ML-Assisted Superior-Device Maps

As an initial test, ML regressors were trained directly on the electrical quantities used in the electrothermal calculation: V_{on}, E_{on}, and E_{off}. The corresponding parity plots are shown in Fig. 10. Although the regressors captured the main trends in the TCAD-derived data, the approach did not reduce the overall calculation time. The overhead of training and evaluating separate surrogates gave an effective speed factor of about $0.5\times$, making it slower than the deterministic interpolation-based calculation. This direct electrical-surrogate route was therefore retained only as a benchmark, not as the final acceleration method.

Figure 11 shows the deterministic three-dimensional

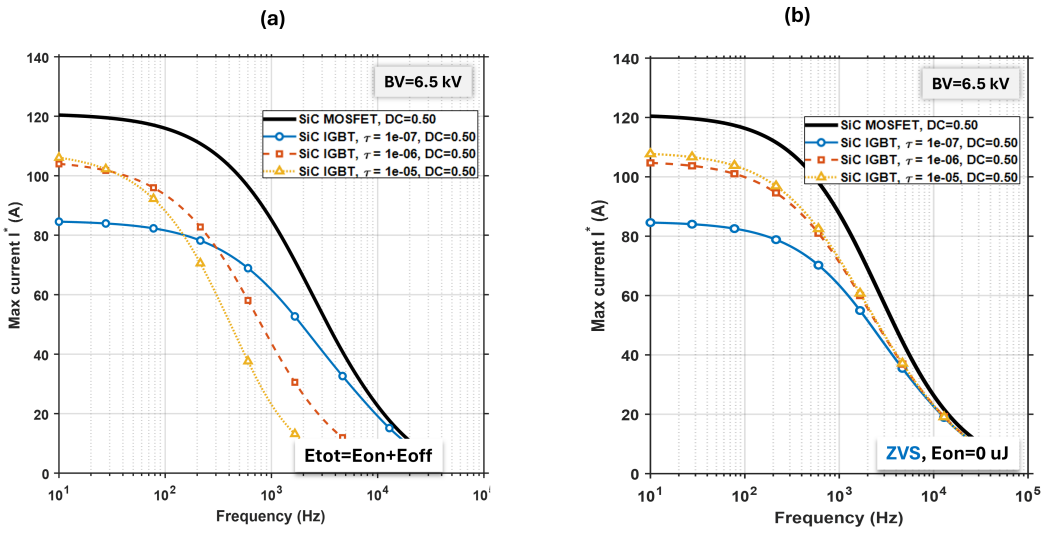

Fig. 7. Maximum-current comparison for the 6.5 kV class assuming (a) hard-switching losses and (b) a ZVS loss scenario. The duty cycle is fixed at $D = 0.5$.

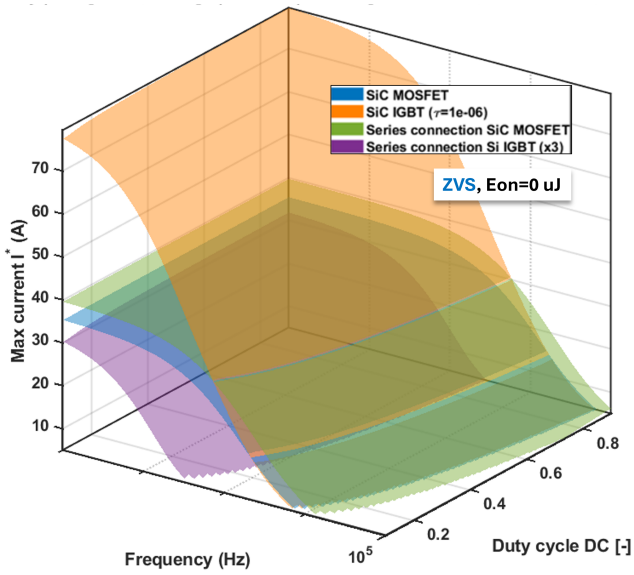

Fig. 8. Maximum-current map for the 20 kV comparison between the SiC MOSFET, SiC IGBT, series-connected Si IGBTs, and series-connected SiC MOSFETs under the ZVS approximation.

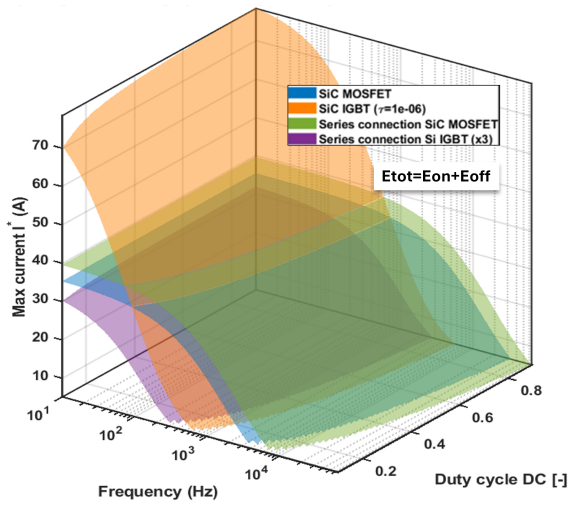

Fig. 9. Maximum-current map for the 20 kV comparison between the SiC MOSFET, SiC IGBT, series-connected Si IGBTs, and series-connected SiC MOSFETs under full hard-switching conditions.

superior-device map obtained from the full self-consistent electrothermal solver. Under the ZVS approximation, the SiC IGBT is favoured over a broad low- to medium-frequency region because of its lower conduction loss. At lower load current and higher switching frequency, the series-connected SiC MOSFET solution becomes increasingly competitive and can outperform the SiC IGBT. Compared with the I^* envelope, this map provides a more complete description of the operating space, since each point stores the selected device, total loss, converged junction temperature, loss margin to the second-best feasible device, and feasibility status of all candidates.

The main drawback of the deterministic approach is its computational cost. For each prescribed sink-temperature and SiC IGBT carrier-lifetime condition, the full operating grid contains

$$N_{\mathrm{op}} = 45 \times 25 \times 55 = 61875. \tag{37}$$

Benchmarking 500 deterministic operating points required 1.448 s, giving an estimated full-map runtime of 179.2 s. To reduce this cost, the hybrid superior-device classifier described in Section III-D was used. The classifier is trained from a subset of deterministic electrothermal evaluations, predicts the superior-device class over the dense grid, and then applies deterministic correction only at low-confidence and predicted-boundary points.

The resulting hybrid map, shown in Fig. 12, preserves the

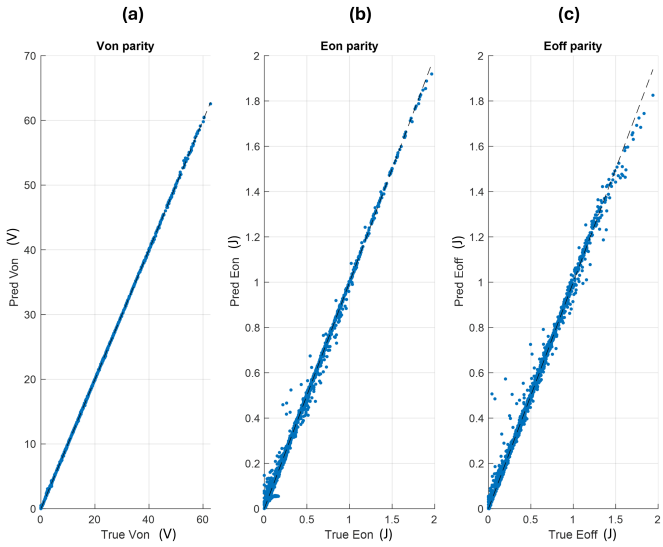

Fig. 10. Training summary for the direct ML electrical surrogate: (a) $\boldsymbol{V_{on}}$, (b) $\boldsymbol{E_{on}}$, and (c) $\boldsymbol{E_{off}}$ prediction.

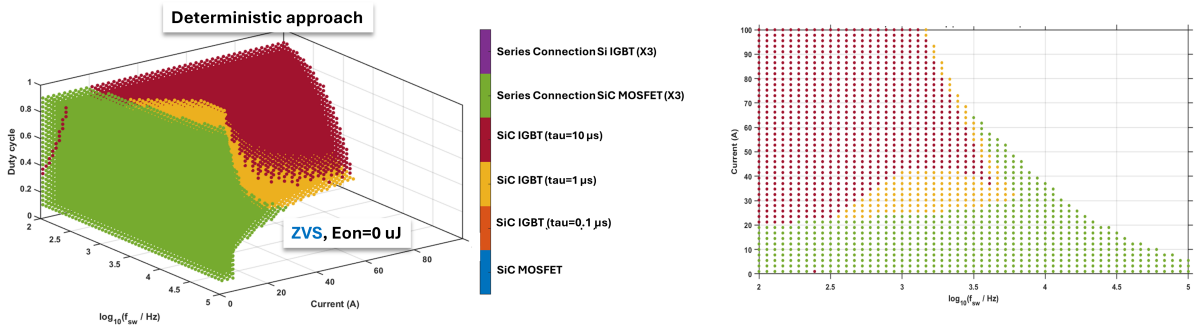

Fig. 11. (a) Power-loss superior-device maps obtained with the full deterministic self-consistent electrothermal approach. (b) Slice of the three-dimensional map at $\boldsymbol{D = 0.9}$.

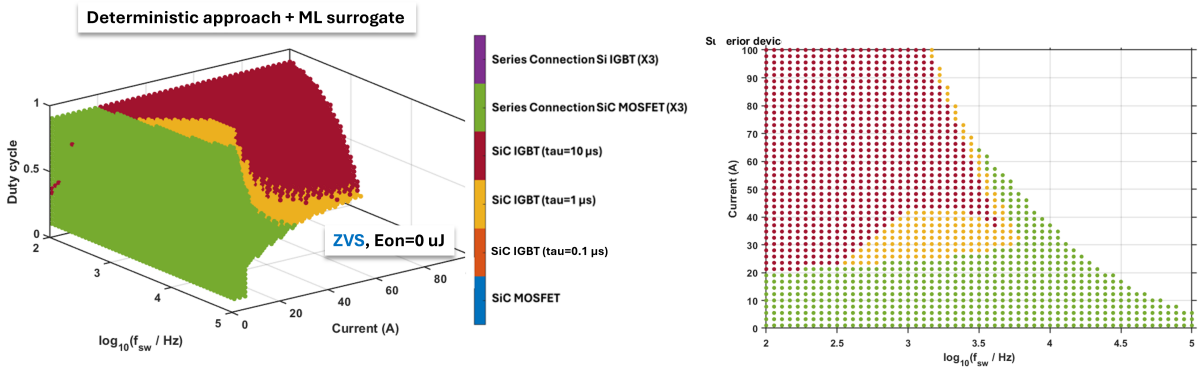

Fig. 12. (a) Power-loss superior-device map obtained with the hybrid deterministic–machine-learning approach. (b) Slice of the three-dimensional map at $\boldsymbol{D = 0.9}$.

main device-selection regions of the full deterministic solution while reducing the number of deterministic electrothermal evaluations. Prediction of the superior-device class over the full grid required 46.7 s (on a standard laptop with an Intel i7 multicore CPU), corresponding to a potential speed-up of approximately $3.8\times$ relative to the full deterministic map if no deterministic correction is applied. This value represents the classifier-only mapping stage and shows that, when deterministic correction is not required, the ML-assisted workflow can generate the superior-device map up to $3.8\times$ faster than

the full deterministic approach. In the present implementation, correction was retained near low-confidence and transition-boundary regions to improve reliability. This stage required a further 38.3 s, with 9786 corrected points,

$$\frac{9786}{61875} \approx 15.8\%, \tag{38}$$

below the imposed correction cap of 25%. The prediction and (subsequent) correction workflow therefore required 85.0 s, giving an effective speed-up of approximately $2.1\times$ excluding the one-time training cost. Including training, the first-run time was 103.9 s, corresponding to a speed-up of approximately $1.7\times$.

The ML stage therefore acts as an accelerator rather than a replacement for the deterministic electrothermal model. It reduces the number of full deterministic evaluations required for dense superior-device maps, while preserving deterministic calculations in regions where classification errors are most likely. The acceleration remains moderate here because the interpolation-based solver is already fast, but the benefit should increase for larger device libraries, denser operating grids, voltage-class sweeps, carrier-lifetime variations, or additional converter parasitic configurations.

C. Comparison with a SPICE Compact-Model Workflow and Model Extension

In 4H-SiC, incomplete ionisation in phosphorus-doped n-type regions and aluminium-doped p-type regions can affect carrier injection and the dynamic switching response. Related issues also arise from oxide/semiconductor trapped charge, whose occupancy can evolve during operation and modify the transient behaviour. As a result, SPICE compact-model extraction is not straightforward, particularly when stored charge, temperature dependence, dynamic capacitances, anisotropic transport, and switching behaviour must all be represented consistently.

The analytical and ML-assisted workflow used in this work avoids this intermediate compact-model extraction step. Well-calibrated SPICE models remain essential for fast circuit-level verification, but their extraction for ultra-high-voltage devices can introduce assumptions that affect loss prediction if charge storage, recombination, temperature-dependent transport, or dynamic capacitance effects are not described accurately. Here, device performance is therefore evaluated directly from physics-informed electrical and thermal characteristics. The same approach can be extended to other circuit conditions, including variations in gate resistance, stray inductance, parasitic capacitance, converter topology, and hybrid parallel- or series-connected device arrangements.

V. Conclusion

A physics-based electrothermal workflow has been developed to compare ultra-high-voltage SiC MOSFETs, SiC IGBTs, and series-connected alternatives under hard- and soft-switching assumptions. The method combines maximum-current capability extraction, deterministic self-consistent loss calculation, and a hybrid machine-learning mapping step for faster identification of the preferred device over large operating spaces.

The results show that three design questions must be treated separately: how much current each device can sustain thermally, which device gives the lowest loss at a given operating point, and how accurately a trained classifier can reproduce the deterministic device-selection map. This distinction is important because the preferred technology is not fixed, but depends on current, switching frequency, duty cycle, thermal boundary condition, and the assumed SiC IGBT carrier lifetime.

For this reason, the I^* maps and the superior-device maps should not be interpreted in the same way. The I^* maps define a thermal current envelope for a prescribed junction-temperature limit. By contrast, the deterministic and ML-assisted maps compare devices at fixed operating points after solving for the self-consistent junction temperature. A device with the highest allowable current is therefore not necessarily the lowest-loss option across the full operating range.

Compared with a compact-model-based SPICE screening approach, the present workflow is more suitable for early-stage technology comparison over wide parameter ranges. SPICE remains essential for final circuit verification once the converter topology and compact models have been fixed. However, by using TCAD-derived electrical characteristics directly, the proposed approach avoids the need to extract a separate compact model for every candidate before assessing loss, thermal feasibility, and current capability. This is especially useful when the device response depends on carrier lifetime, conductivity modulation, incomplete ionisation, temperature-dependent transport, or stored-charge effects, all of which can require substantial compact-model calibration.

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