Frequency-Dependent Distortion in Class II Ceramic Capacitors: Physics and Simulation Traps

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***Abstract*—Class II ceramic capacitors (e.g., X7R, X5R) exhibit a voltage-dependent capacitance that introduces harmonic distortion into analog signal chains. Counterintuitively, the maximum Total Harmonic Distortion (THD) does not occur at the highest frequencies, but rather near the cutoff frequency of the RC filter. This article explains the physical mechanism behind this frequency-dependent distortion peak. Furthermore, it demonstrates that non-physical harmonic content can appear when a voltage-dependent capacitor is implemented as an instantaneous $C(V)$ behavioral element rather than as a charge-defined device $Q(V)$, especially in simplified fixed-step transient solvers or poorly formulated macromodels.**

I. Introduction

Engineers frequently encounter signal degradation when designing analog low-pass filters or AC coupling circuits subject to strict PCB size constraints. Although related effects may appear in AC coupling circuits, the analysis below is limited to the RC low-pass topology shown in Fig. 1. Compact Class II ceramic capacitors (such as X7R or X5R) are often utilized, but their capacitance strongly depends on the applied voltage [1].

At low frequencies, the circuit may operate with minimal distortion. However, as the input signal frequency increases toward the filter's cutoff frequency, the second and third harmonics rise significantly. This article details the origin of this THD peak. Furthermore, it separates the physical distortion mechanisms inherent to the dielectric from numerical artifacts introduced by incorrect transient simulation practices.

II. Voltage-Dependent Capacitance in Class II Ceramics

High-K dielectrics exhibit a Voltage Coefficient of Capacitance (VCC) effect. Applying a DC or low-frequency AC voltage reduces the effective capacitance of the component. Manufacturers such as Murata and TDK document this bias-dependent behavior extensively in their application notes [4].

For circuit simulation purposes, the differential capacitance $C_{diff}(V)$ is often approximated by a heuristic modified Lorentzian function:

$$C_{diff}(V) = \frac{C_0}{1 + k|V|^n} \tag{1}$$

Where C_0 is the base capacitance at zero bias, k is a nonlinearity coefficient dependent on package size and material, and n is a fitting exponent. In this article, $C_{diff}(V)$ denotes the differential capacitance dQ/dV, not the large-signal ratio Q/V. The absolute value $|V|$ ensures symmetry for unpolarized ceramic capacitors. While $|V|$ introduces a point of non-differentiability at zero, it serves as an effective engineering approximation for large-signal behavior without altering the fundamental harmonic generation mechanism analyzed herein.

III. RC Low-Pass Filter with Nonlinear Capacitance

Consider a simple integrating RC circuit (Fig. 1) where the capacitor C utilizes a nonlinear X7R dielectric.

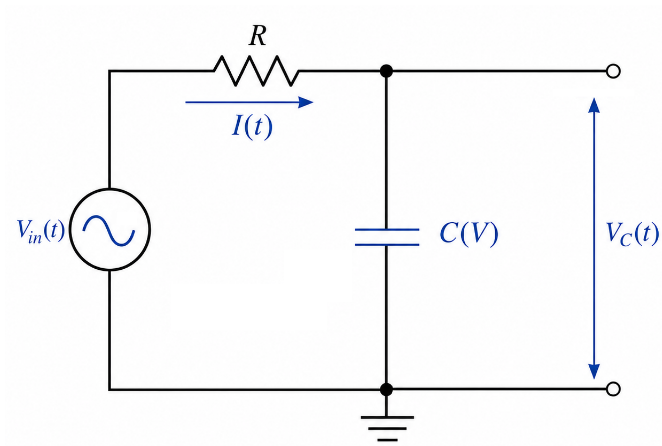

Fig. 1. Schematic of the integrating RC low-pass filter. The signal source $V_{in}(t)$, current-limiting resistor R, nonlinear capacitor $C(V)$, and output voltage across the capacitor $V_C(t)$ are indicated.

The source $V_{in}(t)$ drives the circuit, generating a current $i(t)$. The output is taken across the nonlinear capacitor, denoted as $V_C(t)$. If a nonlinear element is present, one might assume distortion grows monotonically with frequency. However, measurements and physical models dictate a distinct frequency-dependent peak.

IV. Why THD Peaks Near Cutoff Frequency

The presence of a THD peak near the cutoff frequency f_c is a direct consequence of the interaction between the voltage-dependent component and the network's impedance. The behavior is consistent with the frequency dependence expected from nonlinear system analysis, including Volterra-series formulations [3]. We can explain this via fundamental circuit analysis:

At low frequencies ($f \ll f_c$), the capacitor's impedance is exceedingly high. The current $i(t)$ is negligible, and almost the entire input voltage $V_{in}(t)$ appears across the capacitor. Because the current is minute, the nonlinear voltage drop across the resistor R is negligible. The output voltage $V_C(t)$ linearly follows the input, resulting in low THD.

Near the cutoff frequency ($f \approx f_c$), both the current flowing through the circuit and the voltage across the nonlinear capacitor are substantial. The varying capacitance modulates the current waveform. This distorted current produces a highly nonlinear voltage drop across the resistor R. Because $V_C(t) = V_{in}(t) - i(t)R$, the output voltage acquires significant harmonic components. The maximum distortion occurs near this transition band.

At high frequencies ($f \gg f_c$), the current $i(t)$ is large, but the low-pass nature of the filter suppresses the voltage swing across the capacitor. While the nonlinear capacitor continues to produce significant harmonic current components at integer multiples of the fundamental frequency, these harmonics fall deep into the stopband of the low-pass filter. The capacitor effectively shorts these higher-frequency components to ground, reducing the measurable THD in the output voltage $V_C(t)$.

V. Charge-Based Modeling of Nonlinear Capacitors

To correctly simulate such circuits, it is critical to formulate the component mathematically. Current is the derivative of charge:

$$i(t) = \frac{dQ(V)}{dt} \tag{2}$$

Where the total charge $Q(V)$ is the integral of the differential capacitance:

$$Q(V) = \int C_{diff}(V) dV \tag{3}$$

Physical modeling requires using $Q(V)$ as the primary state variable to evaluate the current.

VI. Numerical Artifact in Naive C(V) Transient Solvers

Non-physical harmonic content can appear when a voltage-dependent capacitor is implemented as an instantaneous $C_{diff}(V)$ behavioral element rather than as a charge-defined device $Q(V)$. The issue is not the use of SPICE itself, but an incorrect behavioral implementation of a nonlinear capacitor that updates voltage using a locally frozen capacitance instead of preserving charge.

If a simplified numerical algorithm (e.g., a semi-implicit Euler method) solves the circuit using the capacitance formulation $i = C\frac{dV}{dt}$, the discrete voltage update at step n becomes:

$$V_n = V_{n-1} + \frac{\Delta t}{C_{diff}(V_{n-1})} \cdot i_n \tag{4}$$

In this naive approach, the solver locally "freezes" the capacitance value at $C_{diff}(V_{n-1})$ for the duration of the time step Δt. Because the voltage changes during the step, the charge increment does not equal the physical requirement. Charge is not conserved, leading to continuous mathematical "charge pumping" [2]. This non-physical artifact accumulates and manifests in the spectrum as severe spurious harmonics, causing the simulation to become dominated by numerical artifacts rather than physical reality.

Charge conservation is enforced by using $Q(V)$ as the state relation. The numerical integration method then solves the charge-based differential equation rather than updating voltage from a locally frozen capacitance value.

VII. Simulation Setup

To evaluate the distinction between the physical distortion and the numerical artifact, a Python-based frequency sweep was performed. Total Harmonic Distortion (THD) is calculated at the capacitor voltage $V_C(t)$, summing harmonics up to the 5th order:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \tag{5}$$

The experimental parameters are detailed in Table I. The Python simulation script used to generate Figures 2 and 3 is provided in the open-source repository [5].

TABLE I
Simulation Parameters

Parameter	Value
Circuit Type	RC low-pass, output at V_C
Resistance (R)	1 kΩ
Base Capacitance (C_0)	1 μF
Cutoff Frequency (f_c)	159.15 Hz
Input Waveform	Sinusoidal, 0 V DC bias
Amplitude (V_{peak})	5 V
$C_{diff}(V)$ Nonlin. factor (k)	0.5 V^{-2}
$C_{diff}(V)$ Exponent (n)	2.0
Harmonics for THD	H_2 to H_5
FFT Window	Blackman-Harris
FFT Evaluation	Over 10 steady-state periods
Time Step	$\Delta t = 1/(30f)$ (30 pts/period)
Initial Conditions	$V_C(0) = 0$ V

The simulation procedure is outlined in Algorithm 1.

Algorithm 1 Frequency Sweep Procedure

for each f in logspace(f_{start}, f_{end}) **do**
  Generate $V_{in}(t)$
  Simulate transient response using $Q(V)$ solver (M2)
  Simulate transient response using $C(V)$ solver (M1)
  Discard initial 5 transient periods
  Compute FFT of steady-state $V_C(t)$
  Extract $V_1, V_2, \ldots, V_5$
  Compute THD
end for

VIII. Results

The sweep results comparing the strict charge-conserving model (M2) and the naive variable-capacitance model (M1) are presented in Figure 2.

As predicted by the physical model, THD peaks near the cutoff frequency f_c and then naturally decays. However, the naive model (M1) diverges drastically at high frequencies.

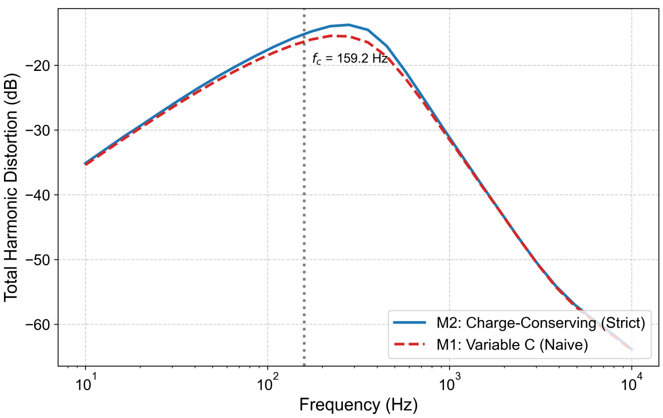

Fig. 2. THD vs. Frequency. Model parameters: $R = 1$ kΩ, $C_0 = 1$ μF, $V_{peak} = 5$ V. The strict charge-conserving model M2 (solid line) shows the physical THD peak. The naive model M1 (dashed line) exhibits divergence at high frequencies.

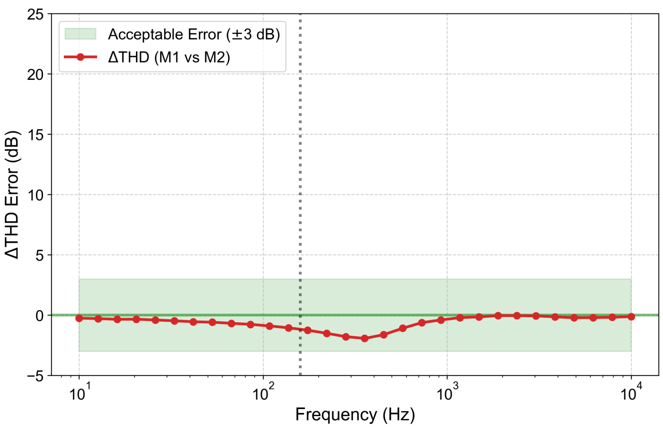

Fig. 3. Simulation Error (ΔTHD). Variable time step corresponding to 30 points per signal period. The error heavily breaches the acceptable ± 3 dB corridor at higher frequencies due to charge non-conservation.

Figure 3 plots the simulation error ($\Delta THD = M1 - M2$). While M1 remains accurate at low frequencies for a given step size, it rapidly breaches the acceptable engineering error margin as frequency increases, attempting to mitigate artifacts introduced by the model.

IX. Engineering Implications

Circuit designers must note the following: 1) **Transition Band Danger:** The maximum physical distortion occurs near the transition band of the RC circuit, not at infinite frequencies. 2) **Amplitude Dependence of Distortion:** Distortion is heavily amplitude-dependent. Small-signal applications may utilize X7R capacitors without significant penalty. 3) **Simulation Fidelity:** When modeling nonlinear circuits with behavioral elements, designers must ensure the simulator employs a strictly charge-based formulation $Q(V)$ to prevent spurious numerical harmonics.

X. Limitations

The models and results presented possess specific engineering limitations. The employed $C(V)$ formulation is a heuristic approximation that simplifies the complex dielectric physics of X7R materials. Crucially, the model does not account for temperature dependencies, frequency dispersion, or dielectric absorption. Furthermore, the analysis restricts itself to symmetrical signals without a DC bias offset. Finally, the exact magnitude of the THD peak is highly dependent on the signal amplitude and the specific package characteristics of the capacitor used.

References

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[2] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 5, pp. 703-708, Oct. 1978.

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[4] Murata Manufacturing Co., Ltd., "Voltage Characteristics of Capacitors," Application Note. [Online].

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