Mixedmode Circuit Simulation of Silicon and Germanium Nanowire MOSFETs
- A Comparative Study

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***Abstract*— Nanowire MOSFETs have been recognized as one of the possible choices to continue the scaling of CMOS beyond conventional scaling limits. In present study we study various aspects of device characteristics and Mixedmode circuit behavior of Silicon and Germanium Nanowire MOSFETs. The various parameters determining the behavior of device in the analog/digital circuits is studied and compared for Nanowire MOSFET with Si and Ge as channel material. Important parameters such as transconductance, output conductance, Ion/Ioff ratio and short channel parameters have been extracted and compared for Silicon and Germanium. The Mixed mode circuit simulation has been done for Inverter (VTC and transient analysis) and 3 stage Ring Oscillator (transient analysis). Results of these simulations give insights into the in-circuit behavior of these future generation devices.**

***Keywords*- Nanowire MOSFETs, short-channel effect (SCE), Mixed-Mode Simulation, Channel Material**

I. INTRODUCTION

According to ITRS [1], continuous scaling down of the traditional single-gate (SG) bulk Complementary Metal Oxide Semiconductor (CMOS) will soon hit its limit. As Semiconductor devices are scaled into the deep sub-micron regime, short-channel effects and poor sub threshold characteristics begin to deteriorate the performance of traditional planar transistors. A decrease in channel length leads to short channel effects, whereas reduction in channel width causes a reduction in current drive and reliability degradation due to high electric field edges. These problems lead to scaling limitations on conventional planar single and double gate MOSFETs. Various nonplanar device structures [2]-[3] have been proposed in recent years to improve the electrostatic control of the channel potential. Among them, the Nanowire-MOSFET (NW-MOS) demonstrates the best control of short-channel effects and can be scaled to the shortest channel length possible for a given gate oxide thickness [4]-[6]. In addition to the effective suppression of short channel effects, the NW-MOS has also shown excellent current drive and are also compatible with conventional CMOS processes [7].

The channel doping is crucial factor to be considered to evaluate the performance of NW-MOS. Along with Silicon, Germanium [8]-[12] is also promising materials for NW-MOS applications due to higher carrier mobility. Various analytical models [13]-[15] for NW-MOS have been proposed recently giving more insight into the device physics. Recent study has given more insights into the in-circuit behavior of NW-MOS [16]-[17]. In the present study we focus on the performance of NW-MOS devices in the circuit. The important parameters for analog circuit design such as threshold voltage, intrinsic gain and various short channel effects have been simulated and results are compared for SI and Ge based NW-MOS. The digital circuit behavior has been simulated by analyzing the performance of CMOS inverter and Ring Oscillator. Section II gives a detailed analysis of potential, current, transconductance, output conductance, Ion/Ioff, threshold voltage and various short channel parameters for the Si and Ge NW-MOS. Section III explores the mixed mode circuit behavior of Si and Ge NW-MOS. The dc, ac and transient analysis of the circuits with Si and Ge based NW-MOS devices have been done and analysis of the results have been done.

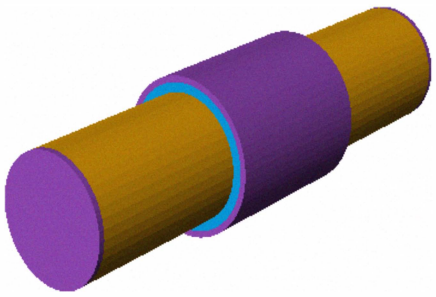

Fig.1 3-D view of Nanowire MOSFET

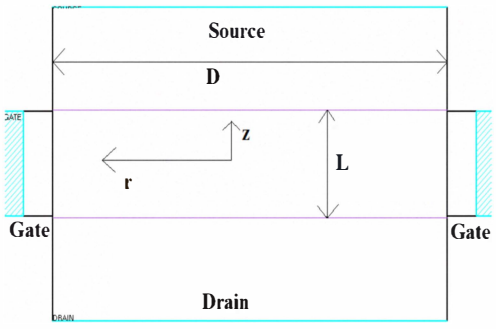

Fig.2 2-D Cross sectional view of Nanowire MOSFET

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II. DEVICE CHARACTERISTICS

Fig.1 shows the cylindrical Nanowire MOSFET and Fig.2 shows the two dimensional view of the Nanowire MOSFET. The material used for the channel region along with their parameters [18] is listed in the Table1. All the simulations are done at room temperature (300K). The values of these parameters are in their default units. The Concentration-Dependent Mobility has been used to model mobility of carriers inside the channel. Shockley-Read-Hall (SRH) Concentration-Dependent Lifetime Model is used to model Carrier generation-recombination in the semiconductor. Boltzmann statistics are used for the carrier statistics. NW-MOS has been simulated for a nearly undoped channel with doping concentration of 1e15 cm^{-3}. NW-MOS of radius=10nm has been simulated for channel lengths of 30nm, 50nm and 70nm. For higher doping concentrations and smaller dimensions the quantum and tunneling effects should also be considered while modeling, although the present study mainly focuses on the effect of channel material on NW-MOS performance.

To prevent direct gate tunneling in very thin oxides, SiN has been used as gate material in place of SiO2 because of its higher permittivity. In this work, gate dielectric thickness is set to a minimum value of 1.5 nm to maintain the gate leakage current to a negligible level with respect to Ioff as suggested by [19]. The channel potential and current distribution for the Si and Ge NW-MOS are shown in Fig.3 and Fig.4

TABLE1

Material	*Epsilon*	E_g	*Chi*	n_i*(per cc)*	*Nc*	*Nv*
Si	11.8	1.08	4.17	1.45e+10	2.8e+19	1.04e+19
Ge	16	0.663	4	1.73e+13	1.05e+19	3.95e+18

For same device dimensions and doping, Ge NW-MOS has higher threshold voltage (Vt) than SI NW-MOS (table2, 3). Thus the sub threshold current in the Ge NW-MOS is smaller than Si NW-MOS because of its inherently larger Vt. In saturation the Ge NW-MOS has higher current due to its higher mobility. Si NW-MOS has shown higher Ion/Ioff ratio than its Ge counterpart.

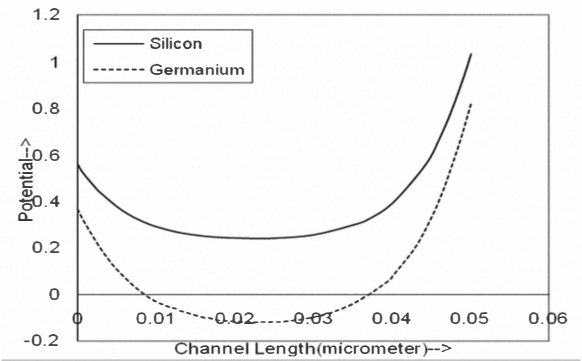

Fig.3 Potential distribution of Si and Ge NW-MOS, Leff=50nm,radius(r)=10nm , VG=0V, VD=0.5V.A midgap workfunction of 4.5 eV is used..

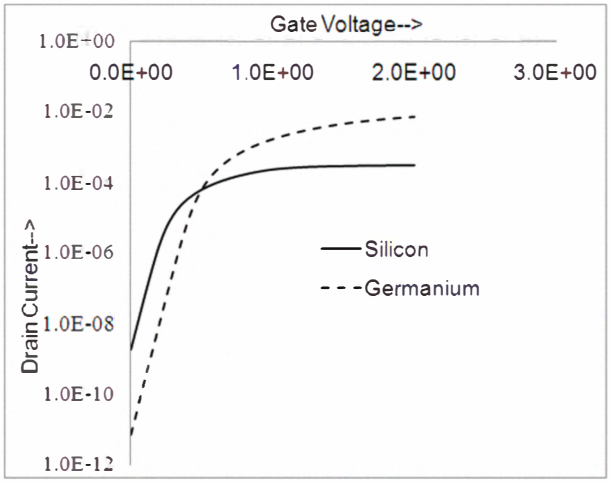

Fig.4 ID-VG results of Si and Ge NW-MOS, Leff=50nm, radius(r) =10nm, VG=0V, VD=0.5V.A midgap workfunction of 4.5 eV is used.

It shows Si NW-MOS may have a better performance in the circuits in which the device on-off transitions is critical. Subthreshold Slope(SS) has shown little variation with channel material and is mainly dependent on device dimensions for NW-MOS. Drain induced barrier lowering (DIBL) has been calculated as ($Vt(V_D=0.05)-Vt(V_D=1)$). Ge NW-MOS has shown better tolerance to drain voltage than its Si counterpart, thus Ge NW-MOS will perform better than Si NW-MOS in circuits having large fluctuations at drain node.

The intrinsic gain of a MOS is a function of its transconductance and output conductance. Fig.5 shows the variation of output conductance for Si and Ge NW-MOS with drain voltage for a V_G=0.5V. The trend is same as drain current for the similar V_{GS}, Ge due to its higher mobility shows much larger conductance in the saturation region corresponding transconductance values. Fig.6 shows the transconductance variation with respect to gate voltage for a drain voltage of 0.05V. For same dimensions and channel doping and silicon has shown greater transconductance because it has lower Vt, so higher overdrive voltage.

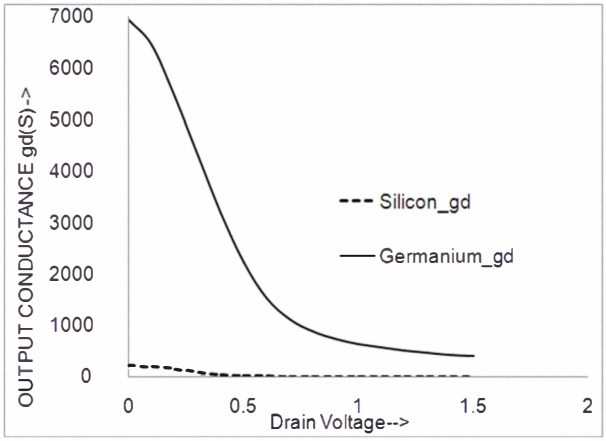

Fig.5 Output Conductance of Si and Ge NW-MOS, Leff=50nm,radius(r)=10nm , VG=0.5V.A midgap workfunction of 4.5 eV is used.

But if overdrive voltage is made same Ge NW-MOS shows higher transconductance than its Si counterpart. Also to gain further insight into the transconductance of NW-MOS , it has been plotted for various channel lengths as shown in Fig.7.From the graph it can be inferred that the gate bias for maximum transconductance is independent of channel length. Present simulations are not valid for further lower channel lengths due to excessive short channel effects at those device dimensions.

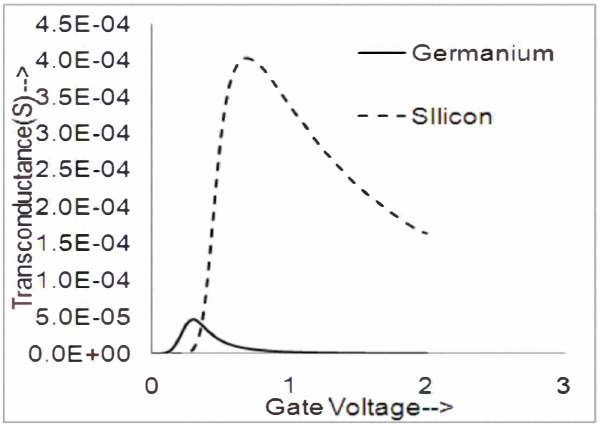

Fig.6 I_D-V_G results of Si and Ge NW-MOS, L_{eff}=50nm,radius(r)=10nm , V_G=0V, VD=0.5V.A midgap workfunction of 4.5 eV is used.

Table2 Silicon NW-MOS Properties

L(nm)	*Vt*	*SS*	*DIBL*	*Ion*	*Ioff*	*Ion/Ioff*
30	0.1509	77.46	0.3812	2.65E-05	1.17E-08	2.92E+06
50	0.1735	63.73	0.3350	1.60E-05	8.79E-10	3.98E+06
70	0.1882	61.42	0.3033	1.57E-05	3.57E-10	3.91E+06

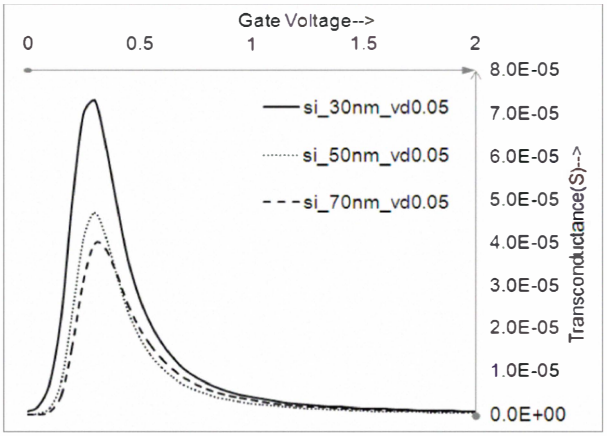

Fig.7 Output Conductance of Si and Ge NW-MOS, Leff=50nm,radius(r)=10nm , VD=0.05V

Table2 Germanium NW-MOS Properties

L(nm)	*Vt*	*SS*	*DIBL*	*Ion*	*Ioff*	*Ion/Ioff*
30	0.4106	78.26	0.2539	7.41E-04	2.06E-10	1.06E+05
50	0.4299	63.71	0.1856	4.48E-04	2.97E-12	1.42E+05
70	0.4439	61.24	0.1370	3.69E-04	7.95E-13	1.66E+05

III. MIXED MODE SIMULATION

The mixed mode circuit simulation for the Si and Ge NW-MOS devices is being done using Silvaco tools. The dc ,transient and ac behavior of the circuits with these devices are reported and conclusions regarding the factors effecting ciruit performance of these devices have been drawn. To check the CMOS compatibility of Si and Ge NW-MOS, CMOS inverter and 3 stage ring oscillator as shown in Fig,8 is simulated. Ntype NW-MOS (NNW-MOS) has been simulated for getting the transient frequency, thus giving the comparison of its intrinsic speed. In case of planar CMOS inverters, to achieve symmetry in rise and fall times in voltage transfer characteristics (VTC), with fixed gate length L, the width W for the p-MOS is kept typically nearly 2× higher than that of n-MOS [20]. As diameters or circumferences of the NW-MOS (corresponding to the *W* in standard CMOS) are the same for both n- and p-transistors, we need to adjust the channel length of NW-MOS transistors to get a symmetric VTC. The aspect ratio of silicon nanowire transistors could be larger than 0.5 or 1 due to different device specification [21]. In the present study the ascept ratio is taken more than 1 to for maintaining acceptable dc characteristics. For both Si and Ge, NNW-MOS of channel length 40nm and PNW-MOS of channel length 20 nm has been simulated. The CMOS inverter is being simulated for a Vdd of 0.5V.

With decreasing gate oxide thickness, the capacitance associated with the depleted layer in polysilicon gate becomes significant, making it necessary to consider alternative gate electrodes. A metal gate technology can overcome these issues provided the appropriate gate work functions can be achieved. In present simulation we use a dual work function CMOS gate technology [22] for simulating the characteristics of CMOS circuits using the NW-MOS. For Si CMOS inverter the NNW-MOS gate work function (Nφ) of 4.45eV and PNW-MOS work function (Pφ) of 4.9 eV has been used to simulate the inverter characteristics as shown in Fig. 9. For Ge the similar work function gives very poor characteristics due to weak NNW-MOS of Ge[23], so to get a better VTC characteristic as in Fig.9, NNW-MOS with gate work function of 4.0eV and PNW-MOS with gate work function of 4.9 eV has been used. This work function can be realized using Molybdenum as shown in [24].

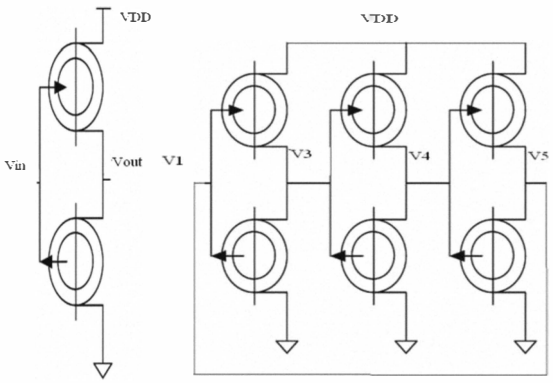

Fig.8 Circuit of CMOS Inverter and 3 Stage Ring Oscillator

The transient analysis has been done for the single inverter for Si and Ge based Inverter is shown in Fig.10.The results clearly show that the Ge based inverter give poor characteristics as it does not give rail to rail swing while its Si counterpart provides rail to rail swing of the output for the same variation of the input. The ring oscillator output for the variation of input is shown in Fig.11 and Fig.12 respectively. The results show a poor behavior in terms of propagation delay and cascading of stages for Ge based circuit.

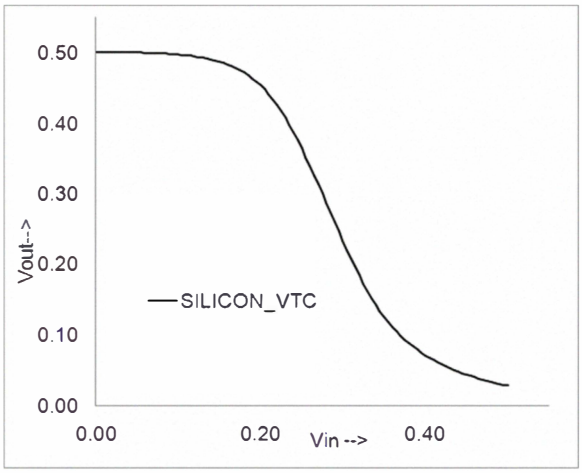

Fig.9 Voltage Transfer Characteristics for Si NW-MOS

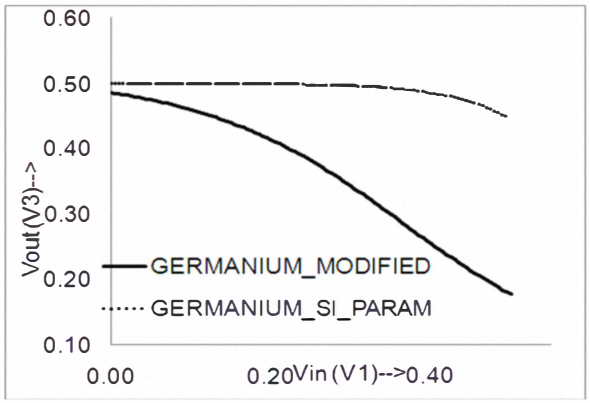

Fig.10 Voltage Transfer Characteristics for Ge NW-MOS

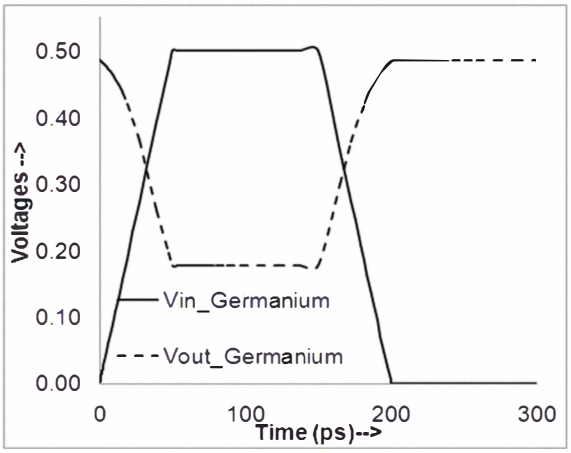

Fig.11 Transient Analysis of Si and Ge NW-MOS

Intrinsic frequency response of MOSFET has been simulated to get the transit frequency. The transit frequency is defined as the frequency at which the small signal current gain of the device drops to unity while source and drain terminals are held at ac ground.[25] Transit Frequency is simulated because it is related to the transit time from source to drain which determines max speed of MOSFET device. The transit frequency for Ge NNW-MOS was found as 6.31E+16 and for Si NNW-MOS, the transit frequency was found to be1.78E+15.

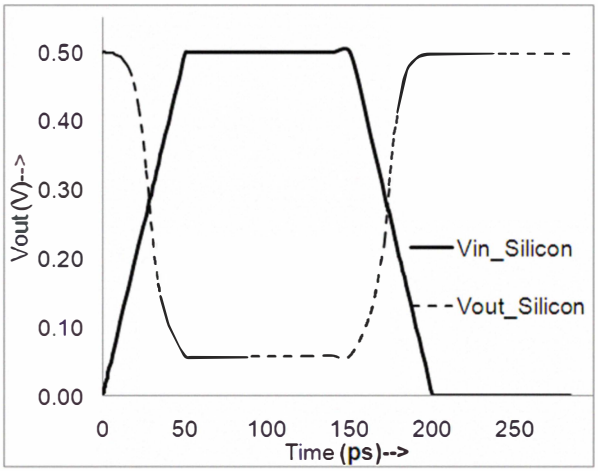

Fig.12 Ring Oscillaotor output for Si NW-MOS

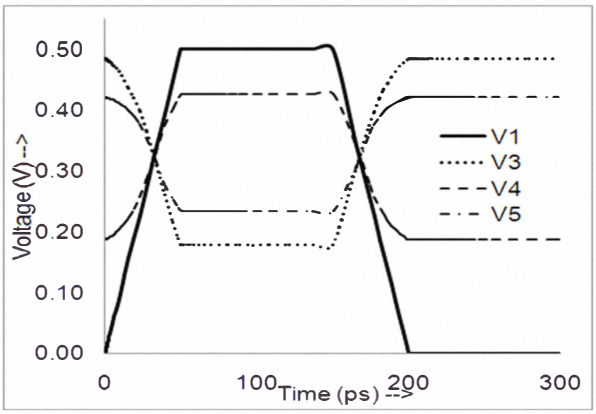

Fig.13 Ring Oscillator output for Ge NW-MOS

IV. CONCLUSION

The mixed mode simulation of dc, ac and transient behavior of Si and Ge based NW-MOS was carried out. The device characteristics of Si and Ge based NW-MOS have been reported and compared. The dual work function CMOS gate technology was used for simulating the circuit characteristics. Ge devices when simulated in standalone mode promises faster and better performance in many aspects, but the devices need to be optimized further so that to use these benefits offered by Ge based NW-MOS for a better circuit performance. On the other hand Si based NW-MOS have shown excellent circuit performance. This further confirms the Nanowire MOSFETs as next generation technology for further scaling and enhanced performance than the planar counterparts of similar dimensions. Future work includes

the study of III-V compounds as channel material for the NW-MOS.

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