Radiation-Hardened FPGA Architectures and Design Techniques for Space Applications: A Comprehensive Review.

Keerthanaa Karthikeyan
Power Electronics and Simulation Engineer, Independent Researcher
Keerthanaak131@gmail.com

Abstract

Field-Programmable Gate Arrays (FPGAs) have become an important technology in modern space systems because of their flexibility, reconfigurability, high processing power, and shorter development time. They are commonly used in satellite payloads, onboard data processing, communication systems, autonomous navigation, and scientific tools. However, the extreme radiation conditions found in space create significant reliability issues for FPGA-based systems. Radiation-related problems such as Total Ionizing Dose (TID), Single Event Upsets (SEUs), Single Event Transients (SETs), Single Event Latchups (SELs), and Single Event Functional Interrupts (SEFIs) can reduce performance, damage data, and lead to mission failures.To tackle these issues, various radiation-hardening methods have been developed at the device, circuit, architecture, and system levels. This review offers a detailed survey of radiation effects in FPGAs and looks at the latest methods used to reduce radiation impact in space applications. The paper covers radiation-hardened FPGA technologies, circuit-level hardening techniques, fault-tolerant design strategies like Triple Modular Redundancy (TMR) and configuration scrubbing, along with their use in actual space missions. It also discusses new trends such as adaptive fault tolerance, artificial intelligence-based onboard processing, and next-generation radiation-tolerant FPGA designs. By gathering recent developments and pointing out existing research gaps, this review gives researchers and engineers a clear understanding of radiation-hardened FPGA design practices and future paths for reliable reconfigurable computing in space settings.

Keywords— Field-Programmable Gate Arrays (FPGAs), radiation hardening, space applications, space radiation effects, Single Event Upsets (SEUs), Single Event Effects (SEEs), Total Ionizing Dose (TID), Triple Modular Redundancy (TMR), configuration scrubbing, fault-tolerant design, radiation-hardened by design (RHBD), radiation-hardened by process (RHBP).

Introduction

The increasing complexity of modern space missions has raised the need for high-performance, flexible, and reliable onboard computing systems. Satellites, deep-space probes, planetary rovers, Earth observation platforms, and scientific payloads need advanced data processing abilities while facing strict limits on power use, weight, and development costs. Among the digital processing options available, Field-Programmable Gate Arrays (FPGAs) have become a popular choice due to their ability to be reconfigured, process data in parallel, allow quick prototyping, and support mission-specific adjustments.

Unlike Application-Specific Integrated Circuits (ASICs), FPGAs can be reprogrammed after deployment, allowing for hardware updates, changes to algorithms, and improvements in functionality throughout a mission's duration. These benefits have led to their widespread use in spacecraft subsystems, including onboard data handling, image processing, communication systems, software-defined radios, guidance and navigation systems, and platforms for autonomous decision-making.

Despite these benefits, using FPGAs in space comes with significant reliability challenges. Spacecraft function in harsh radiation environments, which consist of energetic particles from solar events, galactic cosmic rays, and trapped radiation belts. These particles can

interact with semiconductor devices, leading to various radiation effects, including Total Ionizing Dose (TID) degradation and Single Event Effects (SEEs). Such issues can cause temporary faults, memory problems, logic errors, reduced performance, or permanent device failure. As semiconductor technologies continue to shrink, the risk of radiation-induced failures is becoming an increasingly important issue.

To ensure reliability during missions, extensive research has focused on radiation-hardening methods at different levels of FPGA design. These methods include radiation-hardened-by-process (RHBP) manufacturing, radiation-hardened-by-design (RHBD) circuit techniques, fault-tolerant designs, redundancy systems, error correction methods, and dynamic recovery approaches like configuration scrubbing. Modern space-grade FPGA families combine many of these techniques to provide better durability while keeping the flexibility that makes FPGAs appealing for space uses.

Over the last decade, many studies have looked into radiation effects and suggested ways to reduce risks for FPGA-based space systems. However, the existing literature is often scattered across various levels of complexity, from device physics to system-level fault tolerance. A unified review that connects these viewpoints would be beneficial for both researchers and engineers in the field of space electronics.

This paper offers a thorough review of radiation-hardened FPGA architectures and design methods for space applications. It starts by looking at the space radiation environment and its effects on FPGA technologies. Next, it discusses radiation-hardened FPGA devices, circuit-level mitigation techniques, and design-level fault tolerance approaches. It also analyzes case studies from real space missions to showcase practical strategies and lessons learned. Finally, it explores new trends, research hurdles, and future paths for radiation-resilient reconfigurable computing.

The main contributions of this review are:

1. A detailed overview of radiation-induced effects on FPGA reliability in space settings.

2. A systematic survey of radiation-hardened FPGA technologies and device structures.

3. A comparison of circuit-level and design-level fault tolerance methods.

4. An exploration of practical applications in space missions and aerospace systems.

5. Identification of current challenges, gaps in research, and future opportunities in radiation-resilient FPGA design.

2. Radiation Environment and Effects on FPGAs

2.1 Space Radiation Environment

Table 1: Comparison of Major Radiation Effects

Effect	Cause	Impact	Severity
TID	Long-term ionizing radiation	Parameter degradation	Medium-High
SEU	Particle-induced bit flip	Functional errors	High
SET	Transient pulse	Temporary errors	Medium
SEFI	Device control upset	Device interruption	High
SEL	Parasitic thyristor activation	Permanent damage possible	Very High

Electronic systems used in space constantly face a harsh radiation environment that can greatly impact the reliability and functionality of semiconductor devices. The main sources of radiation include Galactic Cosmic Rays (GCRs), Solar Particle Events (SPEs), and trapped particles in the Earth's radiation belts. These high-energy particles interact with semiconductor materials, causing various radiation-related effects that can change device behavior and reduce long-term reliability.

The level of radiation exposure strongly depends on the mission's orbit and duration. Satellites in Low Earth Orbit (LEO), Medium Earth Orbit (MEO), Geostationary Earth Orbit (GEO), and deep-space missions encounter different particle fluxes and radiation types. Besides direct interactions with particles, secondary particles created through nuclear reactions in spacecraft materials can also lead to radiation-induced failures. As FPGA-based systems are increasingly used for onboard processing, communication, image processing, and autonomous spacecraft operations, understanding the space radiation environment is vital for creating reliable

mitigation strategies.

Radiation effects in semiconductor devices are mainly divided into cumulative effects and single-event effects. Cumulative effects result from long-term radiation exposure and are represented by Total Ionizing Dose (TID). In contrast, single-event effects come from individual particle hits and include instances like Single Event Upsets (SEUs), Single Event Transients (SETs), Single Event Functional Interrupts (SEFIs), and Single Event Latchups (SELs).

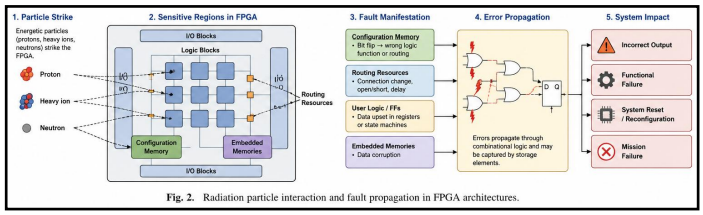

Fig. 2. Radiation particle interaction and fault propagation in FPGA architectures.

2.2 Total Ionizing Dose (TID)

Total Ionizing Dose (TID) refers to the total energy deposited by ionizing radiation in semiconductor materials over time. TID effects are especially important in CMOS technologies because ionizing radiation creates electron-hole pairs in gate oxides and isolation oxides. While electrons are quickly removed by electric fields, holes can get trapped in oxide layers and at oxide-silicon interfaces, leading to permanent degradation of device characteristics.

Trapped charge buildup results in threshold voltage shifts, higher leakage currents, timing issues, increased power use, and eventual functional failure. As radiation dose grows, these effects become more obvious and can seriously reduce device lifespan.

Studies on Xilinx FPGAs showed that TID can cause measurable declines in device performance due to charge accumulation in MOS structures. Research on Flash-based and anti-fuse FPGA technologies indicated that, while these devices have better resistance compared to SRAM-based devices, they are still susceptible to long-term ionizing radiation exposure. Experiments also found that dose rate has a significant effect on FPGA degradation. Lower dose rates often raise failure thresholds because charge annealing processes occur during prolonged irradiation.

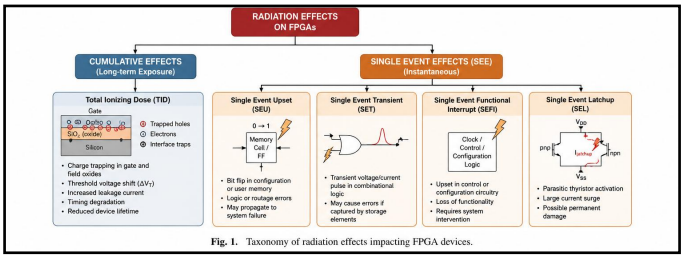

Fig. 1. Taxonomy of radiation effects impacting FPGA devices.

The increasing use of Commercial-Off-The-Shelf (COTS) FPGAs in space systems has driven research efforts to understand TID vulnerability and develop effective mitigation strategies. Therefore, TID characterization is a crucial part of radiation qualification for FPGA-based space electronics.

2.3 Single Event Effects (SEEs)

Unlike TID, which builds up gradually, Single Event Effects (SEEs) happen when a single energetic particle deposits enough charge in a sensitive area of a semiconductor device. The location and amount of charge deposition can trigger various failure mechanisms.

Modern FPGA technologies are particularly prone to SEEs because of their high integration density, smaller transistor dimensions, and heavy reliance on configuration memory. SEEs can impact configuration bits, user logic, routing resources, embedded memories, and control circuits, potentially causing temporary or permanent functional failures.

2.3.1 Single Event Upsets (SEUs)

Single Event Upsets (SEUs) are a major reliability concern for FPGA-based systems in space. An SEU occurs when a high-energy particle deposits enough charge to change the logic state of a storage element, leading to a bit flip.

In SRAM-based FPGAs, SEUs can affect configuration memory cells, user registers, flip-flops, embedded memories, and routing resources. Since configuration memory defines the hardware functionality, a single bit upset can change logic behavior, alter routing paths, or disconnect critical signals. This means SEUs can produce incorrect outputs even if the user circuit itself is physically intact.

Research has shown that FPGA interconnect resources are a primary source of SEU vulnerability. Upsets in routing configuration bits can introduce unexpected

delays, create unintended connections, or disconnect existing signal paths. These issues can lead to timing violations and functional failures, which can be hard to detect during operation.

The increasing use of SRAM-based FPGAs in space applications has spurred substantial research into SEU mitigation techniques, such as Triple Modular Redundancy (TMR), configuration scrubbing, error correction codes, and fault injection methods. These strategies aim to improve system reliability while maintaining the flexibility advantages of reconfigurable hardware.

2.3.2 Single Event Transients (SETs)

Single Event Transients (SETs) occur when a high-energy particle strike causes a temporary voltage pulse in a combinational logic path. Unlike SEUs, which change stored data, SETs create transient disturbances that can spread through the circuit.

If the transient pulse reaches a storage element during its sampling window, it can be captured as erroneous data, appearing as an SEU-like fault at the system level. As operating frequencies increase and technology nodes scale down, the risk of SET propagation becomes more important for assessing FPGA reliability.

SETs are particularly challenging because they do not always leave obvious signs of their occurrence, making detection and diagnosis harder than traditional configuration errors.

2.3.3 Single Event Functional Interrupts (SEFIs)

Single Event Functional Interrupts (SEFIs) are a type of radiation-induced failure that disrupts the normal operation of an entire subsystem or device. Unlike localized SEUs that affect individual memory cells, SEFIs can impact configuration controllers, clock management circuits, communication interfaces, or internal control logic.

A SEFI can cause a device to stop normal operation until corrective action, such as reset, reconfiguration, or power cycling, is taken. Although SEFIs occur less often than SEUs, their consequences can be more severe because they can affect the entire FPGA functionality.

For long space missions where physical intervention is not possible, robust recovery mechanisms are necessary to ensure continued system operation after SEFI events.

2.3.4 Single Event Latchup (SEL)

Single Event Latchup (SEL) is one of the most damaging radiation-induced failure mechanisms for CMOS technologies. SEL happens when a particle strike activates parasitic bipolar transistor structures within CMOS devices, forming a low-resistance current path between power and ground.

This surge of current can greatly increase power consumption and cause localized heating. If not quickly detected and addressed, SEL can permanently damage the device through thermal runaway processes.

Research on latchup mechanisms shows that susceptibility depends on process technology, device design, substrate layout, and operating conditions. Various hardening methods, including guard rings, Silicon-On-Insulator (SOI) technologies, and triple-well structures, have been developed to reduce SEL sensitivity.

Since SEL can lead to severe device failure, latchup protection circuits are often included in radiation-tolerant electronic systems.

Table 2: Radiation Sources in Space

Source	Origin	Typical Impact
Galactic Cosmic Rays	Outside solar system	SEUs, SELs
Solar Particle Events	Sun	SEUs, SEFIs
Trapped Radiation Belts	Van Allen Belts	TID accumulation

2.4 Impact of Radiation on FPGA Architectures

The effect of radiation varies widely among FPGA technologies. SRAM-based FPGAs are usually the most susceptible because configuration information is stored in volatile memory cells that can be directly affected by SEUs. Flash-based FPGAs show better resistance to configuration errors due to their non-volatile storage elements, though user logic and peripheral circuits are still at risk for radiation-induced disruptions. Anti-fuse FPGAs offer the best inherent protection against configuration errors because configuration connections are permanently set during device configuration.

Despite these differences, all FPGA technologies are vulnerable to some mix of TID effects and Single Event Effects. Therefore, choosing FPGA technology for space applications requires careful thought about mission duration, radiation environment, performance needs, power limits, and reliability goals.

Understanding the radiation mechanisms affecting FPGA architectures is key to developing effective hardening strategies. The next sections will review radiation-hardened FPGA technologies and mitigation methods proposed to enhance the reliability of reconfigurable computing systems in space environments.

3. Radiation-Hardened FPGA Technologies and Design Approaches

The increasing use of FPGAs in spacecraft has brought remarkable improvements in onboard computing capability. Their reconfigurability, parallel processing capability, and relatively short development cycle make them an attractive alternative to Application-Specific Integrated Circuits (ASICs) for many space missions. However, these benefits come with a significant challenge: conventional FPGA devices are highly susceptible to radiation-induced failures. As mission complexity increases and spacecraft are expected to operate autonomously for longer durations, ensuring the reliability of FPGA-based systems has become a fundamental requirement rather than an optional design consideration.

To address these challenges, researchers have developed two complementary approaches to improve FPGA reliability. The first focuses on manufacturing devices that are intrinsically resistant to radiation through specialized semiconductor processes. The second enhances reliability through architectural and design techniques without fundamentally altering the fabrication process. These approaches are commonly referred to as Radiation-Hardened by Process (RHBP) and Radiation-Hardened by Design (RHBD). Modern space systems often employ a combination of both strategies to achieve the level of reliability required for long-duration missions.

3.1 Radiation-Hardened by Process (RHBP)

Radiation-Hardened by Process (RHBP) refers to modifications introduced during semiconductor fabrication to improve a device's intrinsic resistance to radiation. Instead of correcting faults after they occur, RHBP aims to reduce the likelihood of radiation-induced failures at the transistor level.

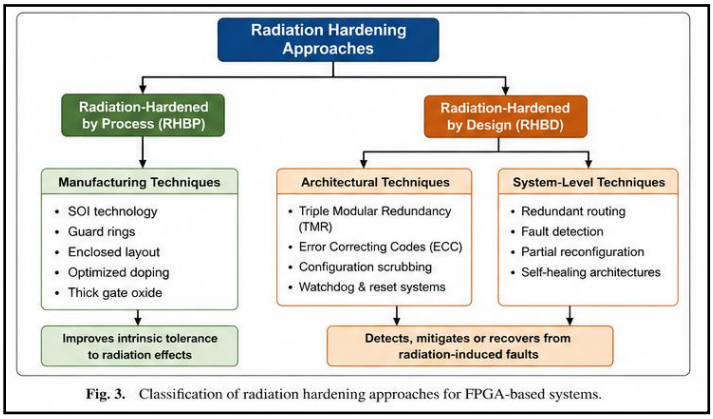

Fig. 3. Classification of radiation hardening approaches for FPGA-based systems.

Typical RHBP techniques include Silicon-on-Insulator (SOI) technologies, optimized doping profiles, guard-ring structures, enclosed-layout transistors, and specialized oxide fabrication processes. These manufacturing techniques reduce charge collection during energetic particle strikes and improve resistance against both cumulative radiation damage and single-event effects. As a result, RHBP devices generally exhibit lower upset rates and improved long-term reliability in harsh radiation environments.

Despite these advantages, RHBP devices present several limitations. They are considerably more expensive than

commercial devices, are often manufactured using older technology nodes, and typically provide lower logic density and computational performance than modern commercial FPGAs. Consequently, they are usually reserved for missions where reliability is the primary design objective, such as deep-space exploration, military spacecraft, and scientific missions with long operational lifetimes.

3.2 Radiation-Hardened by Design (RHBD)

Unlike RHBP, Radiation-Hardened by Design improves reliability through circuit architecture and system-level techniques rather than changes to the manufacturing process. RHBD has become increasingly popular because it enables commercial-off-the-shelf (COTS) FPGAs to be deployed in space while maintaining acceptable reliability.

Table 3: Radiation Effects by FPGA Technology

Technology	TID Sensitivity	SEU Sensitivity	Reprogrammable
SRAM FPGA	Medium	Very High	Yes
Flash FPGA	Medium	Low-Medium	Yes
Anti-fuse FPGA	Low	Very Low	No

Common RHBD techniques include Triple Modular Redundancy (TMR), Error Correcting Codes (ECC), configuration scrubbing, redundant routing, watchdog systems, and fault-detection mechanisms. Rather than preventing radiation events, these techniques detect, mask, or recover from faults before they propagate through the system.

One of the major advantages of RHBD is flexibility. As new mitigation techniques become available, designers can update firmware and design methodologies without requiring changes to the semiconductor manufacturing process. This approach has significantly reduced development costs while enabling the use of high-performance commercial FPGA platforms in increasingly demanding space missions. Nevertheless, RHBD introduces additional hardware overhead, increased power consumption, and potential performance penalties due to redundancy. Therefore, designers must carefully balance reliability against resource utilization and power constraints.

Table 4: Comparision of RHBP and RHBD approaches

Criteria	RHBP (Process-Based)	RHBD (Design-Based)
Primary Principle	Improve intrinsic tolerance through fabrication	Detect, mitigate or recover from errors in design
Advantages	High intrinsic reliability, low upset rates, better long-term stability	Lower cost, high flexibility, applicable to commercial devices
Disadvantages	High cost, older technology nodes, lower performance	Higher area and power overhead, performance penalty
Typical Use Cases	Deep space, military, safety-critical systems	LEO satellites, high-performance payloads, cubesats
Combination Potential	Often combined with RHBD for enhanced robustness	Often combined with RHBP for enhanced robustness

3.3 FPGA Technologies for Space Applications

The susceptibility of an FPGA to radiation depends not only on the mitigation techniques employed but also on the underlying configuration technology. Modern space systems primarily use SRAM-based, Flash-based, or Anti-Fuse FPGAs, each offering different advantages and limitations.

3.3.1 SRAM-Based FPGAs

SRAM-based FPGAs dominate the commercial FPGA market because they provide high logic density, excellent performance, and unlimited reprogrammability. Their configuration data is stored in volatile SRAM cells, allowing hardware functionality to be modified even after deployment.

However, this same configuration memory represents the primary source of vulnerability in radiation environments. A single energetic particle can alter configuration bits, modify routing resources, or corrupt logic functions, potentially affecting the entire implemented design. Consequently, SRAM-based FPGAs require extensive mitigation techniques such as TMR and continuous configuration scrubbing when deployed in space. Despite these challenges, their computational capability continues to make them attractive for advanced onboard processing, artificial intelligence, and high-throughput signal processing applications.

3.3.2 Flash-Based FPGAs

Flash-based FPGAs store configuration information in non-volatile flash memory, providing significantly improved resistance to configuration upsets compared with SRAM devices. Since the configuration cannot be modified by a single radiation event, the probability of catastrophic configuration corruption is substantially reduced.

This improved robustness has led to the widespread adoption of Flash-based devices such as the RTG4 family in many modern spacecraft. While user logic remains susceptible to transient radiation effects, the enhanced stability of the configuration memory simplifies fault management and reduces the need for continuous configuration recovery mechanisms.

3.3.3 Anti-Fuse FPGAs

Anti-Fuse FPGAs represent the most radiation-tolerant configuration technology currently available. During programming, permanent conductive links are created between logic resources, eliminating the volatile configuration memory that characterizes SRAM devices.

The absence of configuration memory provides exceptional immunity to configuration upsets, making Anti-Fuse FPGAs highly suitable for safety-critical missions where reliability outweighs the need for reconfiguration. Their primary limitation is that they cannot be reprogrammed after manufacturing, reducing flexibility for missions requiring in-orbit updates or adaptive processing. Consequently, Anti-Fuse devices are commonly employed in applications where system functionality is fully defined before launch.

3.4 Commercial and Space-Qualified FPGA Devices

The increasing computational demands of modern spacecraft have encouraged manufacturers to develop FPGA families specifically qualified for radiation environments. Space-qualified devices combine radiation-tolerant fabrication technologies with fault-tolerant architectural features, providing improved reliability while preserving many of the benefits of commercial programmable logic.

Recent developments include radiation-tolerant Flash-based devices, radiation-qualified SRAM FPGAs, and emerging platforms capable of supporting artificial intelligence and machine learning workloads directly onboard spacecraft. These devices provide significantly higher computational capability than previous generations while incorporating features such as built-in error detection, redundant configuration memories, and advanced reliability monitoring.

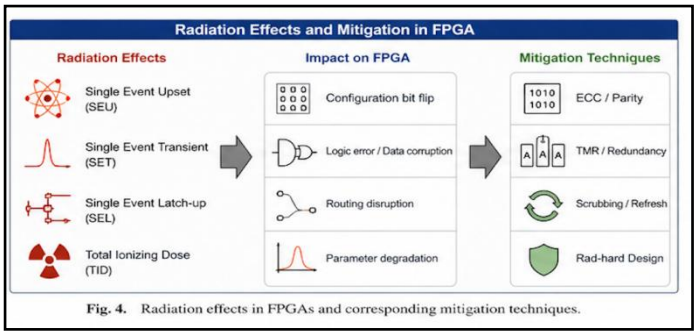

Fig. 4. Radiation effects in FPGAs and corresponding mitigation techniques.

At the same time, the continued advancement of commercial FPGA technology presents a dilemma for space engineers. Commercial devices often outperform radiation-qualified alternatives in terms of logic density and processing capability but require sophisticated fault-tolerance techniques before deployment. As a result, many contemporary missions adopt hybrid strategies that combine commercial hardware with advanced mitigation mechanisms rather than relying exclusively on traditional radiation-hardened components.

Table 5: Comparision of selected space qualified FPGA devices

Device	Manufacturer	Technology	Radiation hard levels	Reprogrammable	Main Use Cases
Xilinx Virtex-5QV	AMD (Xilinx)	SRAM	Rad-Tolerant (QML-V)	yes	NASA payloads, high-performance computing
Microchip RTG4	Microchip	Flash	Rad-Tolerant (QML-V)	yes	Satellites, avionics, space instruments
PolarFire RT	Microchip	Flash	Rad-Tolerant	yes	AI onboard, edge
Microsemi RTAX	Microchip	Anti-Fuse	Rad-Hardened (QML-V)	no	Deep space, safety-critical missions
NG-Medium	ESA / Cobham	SRAM	Rad-Tolerant	yes	European missions, LEO/GEO satellites

3.5 Emerging Trends in Radiation-Hardened FPGA Design

The role of FPGAs in space missions is expanding beyond conventional digital signal processing. Current research increasingly focuses on onboard artificial intelligence, autonomous navigation, image understanding, and adaptive mission planning, all of which demand substantially greater computational performance. Recent surveys indicate growing interest in deploying neural network accelerators and edge AI frameworks on radiation-tolerant FPGA platforms, enabling spacecraft to perform complex data analysis without relying exclusively on ground-based processing.

Another emerging direction involves self-healing FPGA architectures that exploit partial reconfiguration to recover automatically from radiation-induced failures. Instead of merely detecting faults, these systems dynamically reconstruct damaged hardware regions while allowing unaffected portions of the FPGA to continue operating. Such approaches improve system availability and reduce mission downtime, particularly during long-duration autonomous missions where human intervention is impossible.

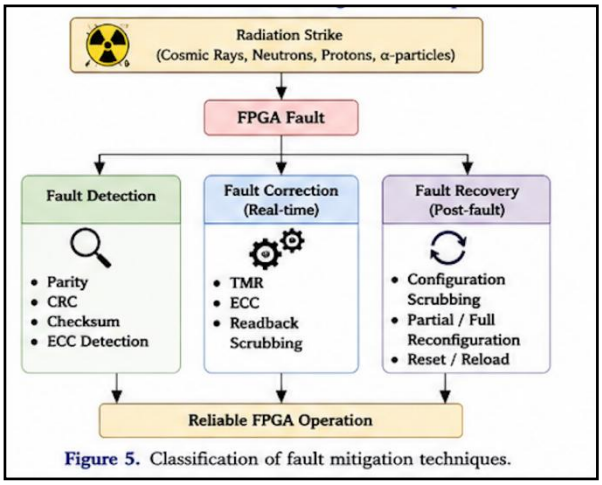

Figure 5. Classification of fault mitigation techniques.

Table 6 : Comparison for FPGA technologies for space application

Feature	SRAM-Based FPGA	Flash-Based FPGA	Anti-Fuse FPGA
Configuration Storage	Volatile SRAM	Non-volatile Flash	Permanent Links
Reprogrammable	Yes	Yes	No
SEU Resistance (Configuration)	Low	Medium-High	Very High
TID Resistance	Medium	High	Very High
Performance (Logic Density, Speed)	High	Medium	Medium
Power Consumption	Medium	Low-Medium	Low
Development Cost	Low	Medium	High
Typical Applications	High-performance processing, payloads	Satellites, avionics, space instruments	Critical missions, deep space, safety-critical systems

3.6 Section Summary

Radiation hardening remains one of the defining challenges in deploying FPGA-based computing systems for space applications. While Radiation-Hardened by Process provides excellent intrinsic reliability, its higher cost and slower technological evolution have encouraged broader adoption of Radiation-Hardened by Design techniques. Advances in configuration technologies, fault-tolerant architectures, and adaptive recovery mechanisms have enabled commercial and radiation-tolerant FPGA platforms to support increasingly demanding onboard applications. As spacecraft continue to incorporate artificial intelligence and autonomous decision-making capabilities, future FPGA architectures are expected to integrate both process-level and design-level hardening techniques to achieve higher performance without compromising mission reliability

4. Fault Mitigation Techniques for Radiation-Induced Errors in FPGA Systems

4.1 Overview of Fault Mitigation Techniques

The increasing deployment of Field-Programmable Gate Arrays (FPGAs) in aerospace and other radiation-intensive environments has significantly improved the computational capabilities of modern embedded systems. Their high processing performance, reconfigurability, and relatively short development cycle have made them indispensable in applications such as onboard satellite processing, autonomous spacecraft control, software-defined radios, and real-time image processing. However, these advantages come with an inherent vulnerability to radiation-induced faults, particularly in SRAM-based FPGA architectures where configuration memory is susceptible to Single Event Upsets (SEUs). As technology continues to scale toward smaller feature sizes, the critical charge required to alter the state of a memory element decreases, increasing the probability of radiation-induced failures.

Radiation-induced faults can propagate through various FPGA resources, including configuration memory, routing resources, user logic, embedded memories, and clock management circuitry. If left uncorrected, these faults may lead to data corruption, timing violations, loss of functionality, or complete system failure. Since physical shielding alone cannot completely eliminate radiation effects and often introduces significant weight

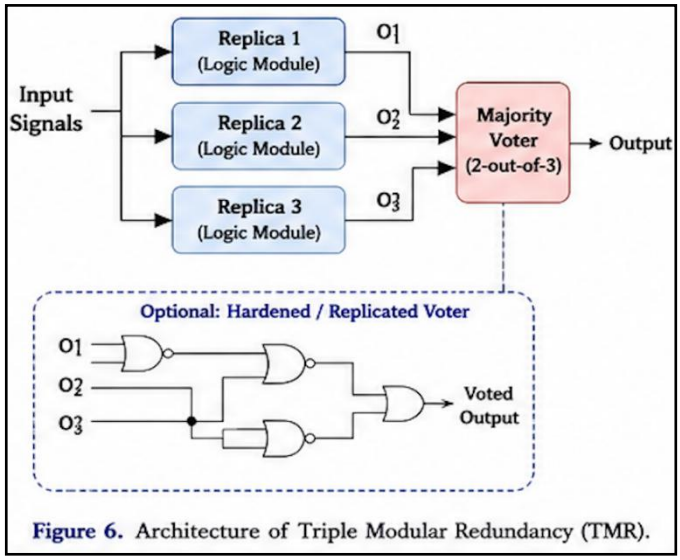

Figure 6. Architecture of Triple Modular Redundancy (TMR).

penalties in spacecraft, modern fault tolerance primarily relies on architectural and design-level mitigation strategies.

Current mitigation approaches generally fall into three complementary categories:

- Fault masking, where redundant hardware prevents errors from affecting system outputs.
- Fault detection and correction, where errors are identified and repaired before propagating.
- Fault recovery, where damaged configurations or hardware modules are restored after a fault occurs.

Most contemporary space-qualified FPGA systems combine several of these techniques simultaneously. For example, Triple Modular Redundancy (TMR) is frequently integrated with configuration scrubbing to mask transient faults while periodically correcting accumulated configuration memory errors. Similarly, Error Correction Codes (ECC) protect embedded memories, whereas partial reconfiguration enables damaged logic regions to be restored without interrupting overall system operation. Such layered protection strategies have become essential for ensuring reliable operation during long-duration missions.

4.2 Triple Modular Redundancy (TMR)

Table 7: Comparision of TMR variants

TMR Variant	Description	Area Overhead	Power Overhead	Reliability	Remarks
Conventional TMR	Three identical replicas + majority voter	≈ 200%	High	5/5	Widely used in space systems
Hardened TMR	TMR with hardened voters & routing	> 200%	Very High	5/5	For mission-critical applications
Selective TMR	TMR applied only to critical modules	30–80%	Medium	4/5	Good area–reliability trade-off
Approximate TMR (ATMR)	Approximate modules with voter	20–60%	Low–Med	3/5	For error-tolerant applications

Triple Modular Redundancy (TMR) is one of the most established and widely adopted fault-tolerance techniques for radiation-prone digital systems. Originally proposed for safety-critical computing applications, TMR has become the de facto standard for protecting SRAM-based FPGAs deployed in space because of its ability to mask transient faults without interrupting system operation. Rather than attempting to prevent radiation events, TMR assumes that faults are inevitable and instead ensures that correct system functionality is maintained despite the occurrence of individual errors.

The fundamental principle of TMR is straightforward: three identical copies of a logic module are implemented in parallel, and their outputs are connected to a majority voter. During normal operation, all three modules produce identical outputs. If a radiation-induced upset affects one module, the remaining two continue to generate the correct result, allowing the majority voter to mask the erroneous output automatically. Consequently, the fault remains transparent to the rest of the system, significantly improving overall reliability.

The effectiveness of TMR depends heavily on the reliability of the majority voter. Because the voter represents a single point of failure, modern implementations often introduce hardened or replicated

voter circuits to improve fault tolerance. Recent studies have also explored hierarchical and distributed voter architectures to reduce vulnerability while minimizing hardware overhead.

Although TMR provides excellent fault masking capability, it introduces considerable implementation costs. Triplicating the logic substantially increases resource utilization, routing complexity, and power consumption. The area overhead may approach 200% compared to a non-redundant implementation, while additional routing resources can increase propagation delay and reduce maximum operating frequency. Consequently, TMR is generally reserved for safety-critical modules rather than being applied indiscriminately throughout an FPGA design.

Recent research has focused on reducing these overheads while preserving fault tolerance. Approximate Triple Modular Redundancy (ATMR) selectively applies redundancy based on application requirements, exploiting the fact that some computational tasks can tolerate small numerical inaccuracies. Such approaches significantly reduce hardware cost while maintaining acceptable reliability for error-resilient applications such as image processing and artificial intelligence. Nevertheless, conventional TMR remains the preferred solution for mission-critical aerospace electronics where functional correctness is mandatory.

Experimental evaluations performed on modern FPGA platforms demonstrate that carefully designed TMR implementations provide substantial improvements in system robustness with relatively modest increases in dynamic power consumption. Recent work has also proposed efficient testing environments based on pseudo-random fault injection mechanisms to evaluate TMR effectiveness under realistic radiation scenarios, enabling designers to optimize mitigation structures before deployment.

Table 8: Advantages and limitations of TMR

Advantages	**Limitations**
Masks single faults instantly	High area and power overhead
No performance interruption	Voter is a single point of failure
Simple and deterministic	Cannot handle multiple faults simultaneously
High reliability for random SEUs	Increased routing congestion
Technology independent	Not suitable for all circuits

4.3 Configuration Scrubbing

Although Triple Modular Redundancy (TMR) effectively masks transient faults during system operation, it does not remove the radiation-induced errors stored within FPGA configuration memory. In SRAM-based FPGAs, configuration bits determine the functionality of logic elements and routing resources. Once an SEU modifies a configuration bit, the erroneous value persists until the affected memory location is rewritten. Consequently, multiple accumulated SEUs may eventually corrupt all redundant modules, rendering TMR ineffective. To overcome this limitation, configuration scrubbing is widely employed as a complementary fault recovery technique that periodically restores the original FPGA configuration.

Configuration scrubbing is the process of continuously or periodically checking the FPGA configuration memory and correcting any detected errors by rewriting the affected configuration frames. Unlike system reboot or complete reconfiguration, scrubbing restores only the corrupted portions of the configuration memory, allowing the user application to continue operating with minimal interruption. This significantly improves system availability and extends the mean time between failures (MTBF) in long-duration space missions.

Several scrubbing strategies have been proposed in the literature, each offering different trade-offs between implementation complexity, resource utilization, and recovery latency.

Blind scrubbing periodically rewrites the entire configuration memory without first checking whether errors are present. The technique is straightforward to implement and provides predictable correction intervals. However, it consumes unnecessary bandwidth and energy because the complete configuration is rewritten regardless of the actual error rate. This makes blind scrubbing less suitable for power-constrained spacecraft.

Readback Scrubbing

Readback scrubbing first reads the current configuration memory, compares it with a reference bitstream, and rewrites only the corrupted frames. Because only affected regions are updated, this approach reduces unnecessary write operations and improves power efficiency. Nevertheless, the additional read-and-compare operations introduce extra latency and require storage of a trusted reference configuration.

Preventative Scrubbing

Recent research has introduced preventative scrubbing, which considers not only existing critical bits but also secondary critical bits that may become hazardous if additional SEUs accumulate. By identifying configuration frames with a higher probability of causing future failures, preventative scrubbing prioritizes correction of the most vulnerable regions. Gear et al. demonstrated that this strategy can improve protection by up to 65% under high SEU rates compared with conventional blind scrubbing techniques.

Frame-Level Intermodular Scrubbing

An alternative strategy is frame-level intermodular scrubbing, where redundant FPGA modules cooperate to repair configuration memory without relying on an external golden bitstream. Giordano et al. proposed such a system for the Belle II experiment, employing majority voting across clustered FPGA modules to identify and correct corrupted configuration frames. Experimental neutron irradiation tests showed that the approach corrected thousands of SEUs before system failure and increased the mean time before failure by approximately 30% compared with traditional vendor-provided scrubbing methods.

Overall, configuration scrubbing has become an indispensable component of modern radiation-tolerant FPGA systems. Rather than replacing redundancy techniques, scrubbing complements them by eliminating accumulated configuration errors, thereby preserving the effectiveness of TMR over extended mission durations.

Table 9: Comparison of Configuration Scrubbing Techniques

Technique	Error Detection	Area Overhead	Power Overhead	Correction Latency	Advantages	Limitations
Blind Scrubbing	No	Low	High	Low	Simple implementation	High bandwidth consumption
Readback Scrubbing	Yes	Medium	Medium	Medium	Corrects only corrupted frames	Read & compare overhead
Preventive Scrubbing	Yes	Medium-High	Medium	Low	Prioritizes critical frames, higher protection	More complex analysis
Frame-Level Intermodular Scrubbing	Yes (Majority)	High	Medium	Low	No golden bitstream needed, high MTBF	Needs redundant FPGA modules

4.4 Error Detection and Correction Codes (ECC)

While configuration scrubbing protects FPGA configuration memory, many radiation-induced faults occur within embedded memories such as Block RAM (BRAM), cache memories, and communication buffers. These memories store mission-critical data and are vulnerable to both Single Event Upsets (SEUs) and Multiple Cell Upsets (MCUs). Error Detection and Correction Codes (ECC) provide an efficient mechanism for identifying and correcting these memory errors with relatively low hardware overhead.

The fundamental principle of ECC is to encode user data by adding redundant parity information before storage. During data retrieval, the stored parity is compared with newly computed parity values. Any discrepancy indicates the presence of an error, allowing the system either to detect or to correct corrupted bits depending on the selected coding scheme.

The simplest implementation is parity checking, which detects single-bit errors but cannot correct them. More advanced techniques such as Hamming Codes enable single-error correction and double-error detection (SECDED), making them widely adopted in FPGA memories. For environments where multiple adjacent memory cells may be affected by a single radiation event, stronger codes such as Reed–Solomon codes and multidimensional ECC schemes provide enhanced protection at the cost of increased implementation complexity.

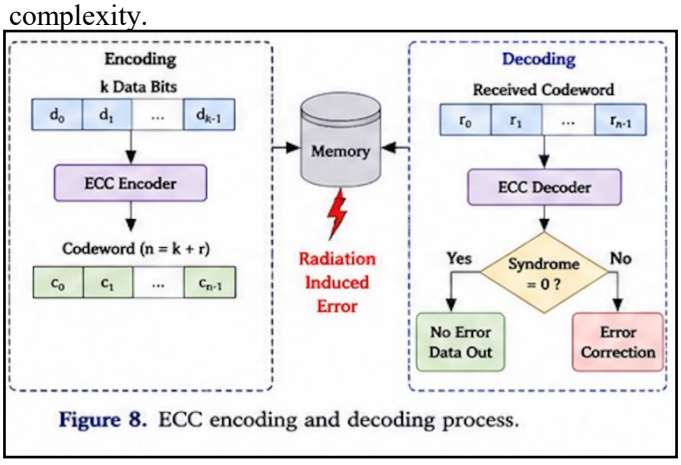

Figure 8. ECC encoding and decoding process.

Modern FPGA-based space systems frequently combine ECC with periodic scrubbing. While ECC immediately corrects transient memory errors, scrubbing prevents long-term accumulation of faults within configuration memory. This layered protection strategy significantly enhances system reliability without incurring the hardware overhead associated with full logic redundancy.

4.5 Fault-Tolerant Strategies for Commercial-Off-The-Shelf (COTS) FPGAs

The rapid evolution of Commercial-Off-The-Shelf (COTS) FPGA technology has significantly transformed modern space electronics. Compared with traditional radiation-hardened devices, COTS FPGAs provide substantially higher logic density, faster processing speeds, lower power consumption per operation, and considerably lower development costs. Consequently, they have become increasingly attractive for NewSpace missions, CubeSats, Earth observation satellites, and onboard artificial intelligence applications. However, these performance advantages come at the expense of increased susceptibility to radiation-induced failures, particularly Single Event Upsets (SEUs) affecting configuration memory and user logic.

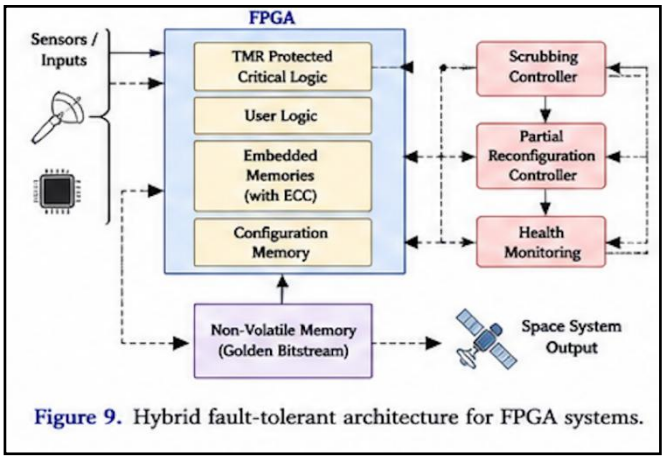

Figure 9. Hybrid fault-tolerant architecture for FPGA systems.

Unlike traditional space-qualified devices, COTS FPGAs are not manufactured using radiation-hardened semiconductor processes. Therefore, achieving mission reliability requires the integration of multiple design-level mitigation techniques rather than relying solely on intrinsic device robustness. Modern spacecraft increasingly employ hybrid fault-tolerant architectures, combining redundancy, error correction, configuration scrubbing, and dynamic recovery mechanisms to achieve acceptable reliability while preserving the computational advantages of commercial hardware.

One widely adopted strategy involves combining Triple Modular Redundancy (TMR) with configuration scrubbing. TMR immediately masks transient faults during operation, whereas scrubbing periodically removes accumulated configuration errors before they compromise redundant logic. This complementary relationship significantly extends system lifetime and has become the standard architecture for many SRAM-based FPGA systems deployed in radiation environments.

Another important development is the integration of partial reconfiguration into fault-tolerant architectures. Rather than interrupting the entire FPGA when a fault occurs, only the affected configuration region is reprogrammed while the remaining logic continues normal execution. This capability greatly reduces recovery time and improves overall system availability. Recent implementations on AMD/Xilinx UltraScale+ MPSoC platforms have demonstrated that combining partial reconfiguration with redundancy techniques can reduce system downtime by more than 90% for representative signal-processing workloads.

Current research also explores hybrid redundancy approaches that combine spatial redundancy, temporal redundancy, and application-specific protection. Instead of triplicating every hardware module, redundancy is selectively applied only to critical computational blocks, reducing resource utilization while maintaining acceptable reliability. Such selective protection strategies are becoming increasingly important as FPGA complexity continues to increase.

4.6 Comparative Analysis of Fault Mitigation Techniques

Although numerous fault-mitigation strategies have been proposed for radiation-tolerant FPGA systems, no single technique provides complete protection against all radiation-induced failures. Each method addresses a specific class of faults and introduces its own trade-offs in terms of hardware overhead, power consumption, implementation complexity, and recovery capability. Consequently, modern spacecraft increasingly employ layered fault-tolerance architectures, where several complementary techniques operate simultaneously to maximize overall system reliability.

Triple Modular Redundancy offers immediate fault masking and remains the preferred solution for protecting mission-critical logic. However, its

substantial area and power overhead make full-device implementation impractical for resource-constrained systems. Configuration scrubbing effectively restores corrupted configuration memory but cannot prevent transient errors between scrubbing intervals. Similarly, Error Correction Codes provide efficient protection for embedded memories yet do not safeguard combinational logic or routing resources. Partial reconfiguration extends system availability by repairing damaged logic regions during operation but requires additional configuration management and control circuitry.

As FPGA complexity continues to increase, researchers have shifted their attention toward adaptive fault-tolerance, where mitigation strategies are dynamically adjusted according to the current radiation environment, application workload, and system health. Such adaptive architectures aim to balance reliability against resource utilization, enabling future spacecraft to maintain dependable operation while minimizing unnecessary redundancy.

Table 10 : Comprehensive Comparison of Fault Mitigation Techniques

Technique	Targets	Typical Overhead (Area)	Power Impact	Reliability Improvement	Best Use Cases
TMR	Logic SEUs	~ 2.0×	High	Very High	Mission-critical logic blocks
ECC	Memory SEUs (MCUs)	1.1–1.3×	Low	High	On-chip BRAM, Buffers, FIFOs
Configuration Scrubbing	Configuration SEUs	1.2–1.5×	Medium	Very High	SRAM-based FPGAs
Partial Reconfiguration	Permanent faults / SEUs	1.3–1.6×	Medium	Very High	Long-duration missions
Hybrid Approaches	All fault types	> 2.0×	High	Excellent	Deep-space & Critical systems

4.7 Open Research Challenges

Despite significant progress in radiation-tolerant FPGA design, several challenges remain unresolved. Technology scaling continues to reduce transistor dimensions, increasing sensitivity to Single Event Effects while simultaneously making fault characterization more complex. The growing adoption of artificial intelligence accelerators and heterogeneous FPGA systems introduces new reliability concerns, particularly for applications requiring continuous autonomous operation in deep-space environments.

Another emerging challenge is the limited availability of comprehensive in-orbit reliability data. Many mitigation techniques are validated through laboratory irradiation experiments, yet long-term operational behavior under actual mission conditions remains insufficiently documented. Furthermore, balancing fault tolerance with stringent spacecraft constraints on mass, power consumption, and computational performance remains an active area of research.

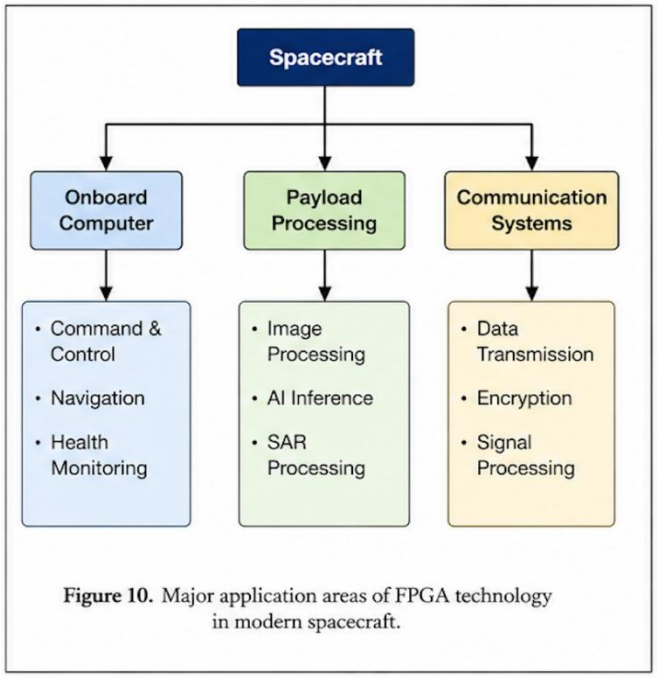

Figure 10. Major application areas of FPGA technology in modern spacecraft.

Future investigations are therefore expected to focus on adaptive redundancy, intelligent fault prediction, self-healing FPGA architectures, and machine-learning-assisted fault management. These approaches have the potential to improve reliability while reducing the implementation overhead traditionally associated with radiation-hardened digital systems.

4.8 Section Summary

Radiation-induced faults remain one of the principal challenges limiting the deployment of high-performance

FPGA systems in space applications. This section reviewed the major design-level fault-mitigation strategies currently employed to enhance FPGA reliability, including Triple Modular Redundancy, configuration scrubbing, Error Correction Codes, partial reconfiguration, and hybrid protection schemes. While each technique offers distinct advantages, no individual solution provides complete fault tolerance under all operating conditions. Instead, contemporary spacecraft increasingly rely on integrated, multi-layered mitigation architectures that combine fault masking, error correction, and dynamic recovery mechanisms. As space missions continue to demand greater onboard processing capability, future FPGA systems are expected to incorporate adaptive, self-healing, and AI-assisted fault-management techniques, enabling higher computational performance without compromising mission reliability.

5. Applications and Case Studies of Radiation-Hardened FPGA Systems

5.1 Introduction

Over the past two decades, Field-Programmable Gate Arrays (FPGAs) have evolved from programmable digital logic devices into versatile computing platforms capable of executing computationally intensive tasks directly onboard spacecraft. Their ability to combine hardware-level parallelism with post-deployment reconfigurability has made them increasingly attractive for modern space missions, where computational requirements continue to grow while power, mass, and communication bandwidth remain constrained. Unlike traditional processors that execute instructions sequentially, FPGA architectures allow multiple operations to be performed simultaneously, enabling real-time processing of sensor data, image streams, communication signals, and artificial intelligence workloads with significantly lower latency.

The transition toward autonomous spacecraft has further accelerated the adoption of FPGA technology. Earlier generations of satellites primarily relied on transmitting raw sensor data to ground stations for analysis. While this approach simplified onboard electronics, it also introduced communication delays, increased bandwidth requirements, and limited the ability of spacecraft to respond immediately to rapidly changing environmental conditions. Modern missions increasingly perform substantial portions of data processing onboard, allowing only relevant information to be transmitted to Earth. This paradigm significantly reduces communication overhead while enabling faster scientific observations and operational decision-making.

Despite these advantages, operating programmable hardware in space remains challenging because electronic devices are continuously exposed to ionizing radiation, energetic particles, and extreme thermal conditions. As discussed in previous sections, radiation-induced faults such as Single Event Upsets (SEUs), Single Event Functional Interrupts (SEFIs), and Total Ionizing Dose (TID) degradation can compromise FPGA functionality if appropriate mitigation strategies are not employed. Consequently, successful deployment of FPGA systems depends not only on computational capability but also on carefully designed fault-tolerant architectures incorporating redundancy, configuration scrubbing, error correction, and dynamic recovery mechanisms. These techniques have enabled programmable logic devices to move beyond experimental demonstrations and become integral components of operational space missions.

Recent advances in semiconductor technology have further expanded the range of FPGA applications in space. High-performance System-on-Chip (SoC) platforms now integrate multicore processors, programmable logic, hardware accelerators, and high-speed communication interfaces within a single device. Such heterogeneous architectures allow computational tasks to be distributed efficiently between software and hardware components, combining the flexibility of general-purpose processors with the parallel execution capability of FPGA logic. This architecture has proven particularly valuable for computationally demanding applications including Synthetic Aperture Radar (SAR) image formation, onboard artificial intelligence, autonomous navigation, hyperspectral image processing, and real-time communication systems.

As spacecraft become increasingly autonomous, FPGA technology is expected to play an even greater role in future missions. Rather than functioning merely as programmable interfaces, FPGAs are now becoming central computing platforms responsible for processing large volumes of scientific data, executing machine learning algorithms, and maintaining reliable system operation under harsh environmental conditions. Understanding how these devices have been successfully deployed in operational missions therefore provides valuable insight into current design practices and future technological trends.

5.2 FPGA Applications in Modern Space Missions

The adoption of FPGA technology within the space industry has been driven by a combination of performance, flexibility, and reliability. Unlike fixed-function Application-Specific Integrated Circuits (ASICs), FPGAs can be reprogrammed after manufacturing and, in many cases, even after launch. This capability enables mission designers to update processing algorithms, correct design flaws, and introduce new functionalities throughout the operational lifetime of a spacecraft. Such adaptability is particularly valuable for long-duration missions where physical hardware replacement is impossible.

One of the earliest and most widespread applications of FPGAs is spacecraft onboard computing. Flight computers are responsible for coordinating subsystem communication, processing sensor information, executing control algorithms, and managing telemetry. These operations often involve concurrent data streams originating from attitude sensors, star trackers, inertial measurement units, propulsion controllers, and communication systems. Because FPGA architectures naturally support parallel execution, they can process multiple sensor inputs simultaneously while maintaining deterministic timing behaviour, an important requirement for safety-critical aerospace systems.

Beyond spacecraft control, FPGAs have become indispensable in payload data processing. Scientific instruments frequently generate data at rates that exceed the available communication bandwidth between spacecraft and ground stations. Earth observation satellites, for example, continuously acquire large volumes of optical, multispectral, hyperspectral, or radar imagery. Transmitting every raw measurement to Earth would require significant communication resources and introduce delays that reduce the practical value of time-sensitive information. Consequently, modern missions increasingly perform compression, filtering, feature extraction, and preliminary interpretation directly onboard before transmitting only relevant results.

Communication subsystems also benefit substantially from programmable hardware. Modern satellites employ increasingly sophisticated communication protocols requiring modulation, coding, encryption, synchronization, and error correction to be executed in real time. FPGA implementations allow these signal-processing operations to be performed with high throughput while maintaining relatively low power consumption. Because communication standards continue to evolve, the ability to update hardware functionality through reconfiguration provides a significant operational advantage over fixed-function hardware implementations.

Another rapidly expanding application area involves autonomous navigation. Spacecraft operating in deep-space environments cannot always rely on continuous communication with ground stations due to propagation delays. Consequently, onboard decision-making has become increasingly important. FPGA accelerators enable real-time processing of camera images, star tracker measurements, LiDAR data, and inertial sensors required for autonomous guidance and navigation. Their deterministic execution characteristics further enhance reliability for time-critical control applications.

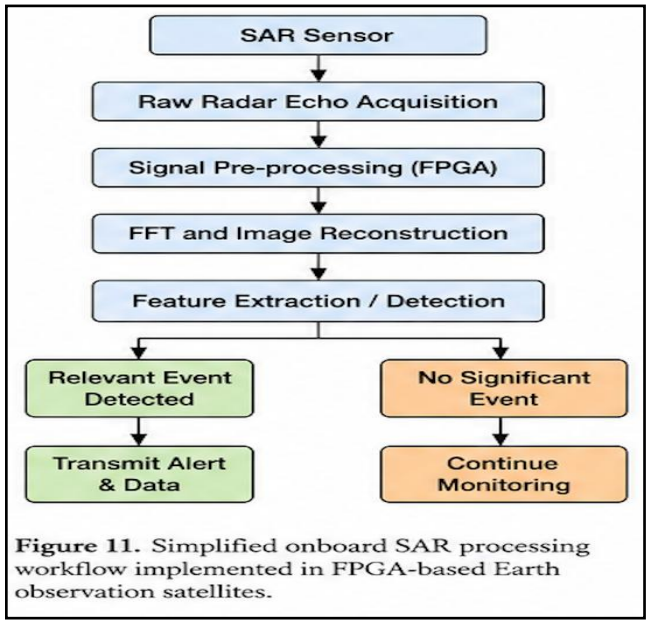

Figure 11. Simplified onboard SAR processing workflow implemented in FPGA-based Earth observation satellites.

The emergence of artificial intelligence has introduced yet another dimension to FPGA applications. Neural networks capable of object detection, terrain classification, anomaly identification, and predictive maintenance require significant computational resources while operating under strict power constraints. GPUs, although computationally powerful, often consume more power than is acceptable for many satellite platforms. FPGA-based neural network accelerators provide an attractive alternative by exploiting customized parallel hardware tailored to specific inference workloads. Their energy efficiency has encouraged increasing adoption for onboard image interpretation and autonomous mission planning.

Recent developments also demonstrate the growing importance of heterogeneous System-on-Chip architectures that combine ARM processors with programmable FPGA logic. Rather than assigning every computation to programmable hardware, software tasks such as mission management, communication protocols, and scheduling execute on embedded processors, while computationally intensive operations including Fast Fourier Transforms (FFT), convolution, image filtering, and signal processing are accelerated by FPGA logic. This division of labour allows each subsystem to execute tasks best suited to its architecture, improving both computational performance and overall energy efficiency.

The continuous diversification of FPGA applications demonstrates that programmable logic has become much more than an auxiliary hardware component. Instead, FPGAs increasingly function as the computational backbone of modern spacecraft, enabling autonomous operation, efficient onboard processing, and adaptive mission capabilities while maintaining the reliability required for radiation-intensive environments.

5.3 Earth Observation and Synthetic Aperture Radar (SAR) Processing

Earth observation has become one of the most demanding applications for onboard satellite computing due to the enormous volume of data generated by modern imaging sensors. Optical cameras, hyperspectral sensors, and Synthetic Aperture Radar (SAR) instruments continuously capture high-resolution images that provide valuable information for environmental monitoring, maritime surveillance, disaster management, agricultural assessment, and national security. Traditionally, satellites transmitted this raw data to ground stations where computationally intensive processing was performed. Although this approach simplified onboard hardware, it introduced significant delays and required substantial communication bandwidth, limiting the ability to respond rapidly to time-sensitive events.

Recent advances in FPGA technology have fundamentally changed this workflow by enabling high-performance image processing directly onboard spacecraft. Instead of transmitting raw sensor data, satellites can now execute computationally demanding algorithms in orbit, allowing only processed information or detected events to be sent to Earth. This approach substantially reduces communication requirements while enabling near real-time decision-making, particularly for missions involving emergency response and continuous environmental monitoring. The combination of high computational throughput, parallel processing capability, and relatively low power consumption makes FPGA-based architectures particularly suitable for these applications.

Synthetic Aperture Radar represents one of the most computationally intensive payloads deployed on Earth observation satellites. Unlike optical sensors, SAR systems actively illuminate the Earth's surface using microwave signals, enabling high-resolution imaging regardless of cloud cover, weather conditions, or time of day. However, transforming raw radar echoes into meaningful images requires complex signal-processing operations, including Fast Fourier Transforms (FFT), range compression, azimuth compression, motion compensation, and image reconstruction. These operations involve large volumes of matrix calculations that are difficult to perform efficiently using conventional onboard processors. FPGA architectures overcome this limitation by executing many processing stages simultaneously through dedicated hardware pipelines, significantly accelerating SAR image formation while maintaining relatively low energy consumption.

A notable example demonstrating the effectiveness of onboard FPGA processing is the EO-ALERT (Earth Observation Alert) project developed under the German Aerospace Center (DLR). The primary objective of EO-ALERT is to reduce the delay between image acquisition and the delivery of actionable information by moving computationally intensive processing from ground stations directly onto the satellite platform. Instead of transmitting complete SAR images, the onboard system automatically identifies relevant events such as ships, flooded regions, or disaster-affected areas and transmits only the extracted information. This significantly reduces downlink bandwidth requirements while enabling authorities to receive critical alerts much faster than with traditional processing workflows.

The EO-ALERT architecture employs a heterogeneous computing platform based on the AMD/Xilinx Zynq UltraScale+ MPSoC, integrating multicore ARM processors with programmable FPGA logic on a single chip. This heterogeneous design allows software-oriented tasks, including mission management and communication protocols, to execute on the embedded processors, while computationally demanding signal-

processing algorithms are accelerated within the FPGA fabric. Such task partitioning exploits the strengths of both processing architectures, providing high computational performance without significantly increasing system power consumption. According to the study, this hardware–software co-design enables efficient execution of SAR processing pipelines while satisfying the stringent energy constraints associated with spaceborne platforms.

One of the most significant advantages of onboard SAR processing is the reduction in communication latency. Conventional Earth observation satellites typically store acquired images before transmitting them to ground stations for processing. Depending on orbital position and ground station availability, this process may introduce delays ranging from several minutes to several hours. By contrast, onboard FPGA-based processing enables immediate analysis of acquired data, allowing emergency events to be detected and reported almost instantly. Such capability is particularly valuable for applications including maritime surveillance, illegal fishing detection, oil spill monitoring, wildfire assessment, flood mapping, and search-and-rescue operations, where rapid response directly influences operational effectiveness.

Despite these advantages, implementing SAR processing on radiation-exposed FPGA platforms presents several engineering challenges. High computational workloads increase power consumption and thermal dissipation, while the harsh space radiation environment introduces the risk of Single Event Upsets (SEUs) affecting configuration memory and processing logic. Consequently, practical onboard processing systems typically combine high-performance FPGA architectures with fault-tolerant techniques such as Triple Modular Redundancy (TMR), configuration scrubbing, and Error Correction Codes (ECC), ensuring reliable operation throughout extended mission durations. These protection mechanisms, discussed in the previous section, are essential for maintaining continuous processing capability without compromising mission safety.

The EO-ALERT project demonstrates a broader trend within the space industry toward intelligent, autonomous spacecraft capable of processing information locally rather than relying exclusively on ground infrastructure. As onboard computing resources continue to improve, FPGA-based systems are expected to support increasingly sophisticated applications, including real-time artificial intelligence, autonomous target recognition, and adaptive mission planning. This transition from data acquisition to onboard knowledge generation represents a significant shift in spacecraft architecture and highlights the central role that radiation-tolerant FPGA platforms will play in future Earth observation missions.

5.4 Artificial Intelligence and Deep Learning on Radiation-Tolerant FPGA Systems

The rapid advancement of artificial intelligence (AI) has significantly transformed the capabilities of modern spacecraft. Unlike conventional satellites that primarily collect and transmit raw data to ground stations, next-generation space systems increasingly perform intelligent data analysis directly onboard. This shift has been driven by the growing demand for autonomous decision-making, reduced communication latency, and efficient utilization of limited downlink bandwidth. Applications such as object detection, terrain classification, cloud identification, anomaly detection, and autonomous navigation require substantial computational resources while operating within strict power and weight constraints. FPGA-based computing platforms have emerged as an attractive solution because they combine hardware-level parallelism with relatively low power consumption, enabling efficient execution of deep learning algorithms in space environments.

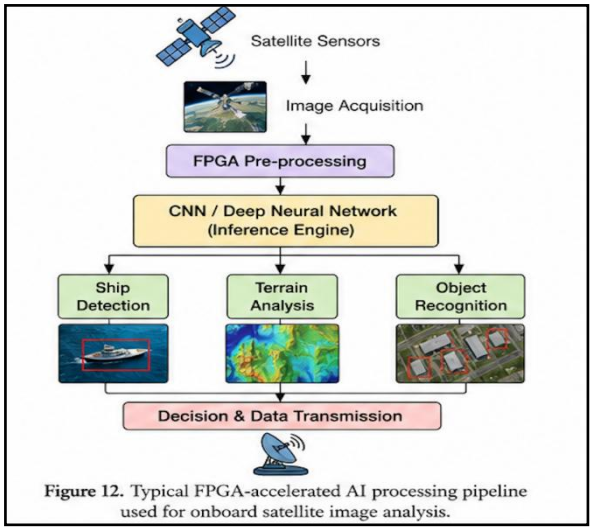

Figure 12. Typical FPGA-accelerated AI processing pipeline used for onboard satellite image analysis.

Deep Neural Networks (DNNs), particularly Convolutional Neural Networks (CNNs), have become the dominant approach for processing satellite imagery due to their ability to automatically extract hierarchical features from complex datasets. In Earth observation missions, CNNs can identify ships, buildings, roads,

vegetation, and disaster-affected regions with remarkable accuracy. However, executing these computationally intensive models on conventional onboard processors often exceeds available computational resources and energy budgets. FPGA accelerators overcome this limitation by implementing convolution, pooling, and activation operations directly in programmable hardware, allowing multiple processing elements to operate concurrently. As a result, neural network inference can be performed with significantly lower latency and improved energy efficiency compared with traditional processor-based implementations.

One representative example is the development of resilient neural network architectures for satellite image analysis presented in the Politecnico di Torino study. The work investigated the implementation of an object detection system based on the Single Shot Detector (SSD) algorithm, using quantized versions of MobileNetV2 and VGG16 networks deployed on FPGA platforms. The application focused on automatic ship detection from satellite imagery, demonstrating that FPGA-based accelerators are capable of performing complex image recognition tasks while maintaining the computational efficiency required for onboard operation. The use of low-bit quantization further reduced memory requirements and computational complexity without significantly affecting detection accuracy, making the approach particularly suitable for resource-constrained space systems.

Despite these advantages, deploying neural networks in radiation environments introduces new reliability challenges. Radiation-induced Single Event Upsets (SEUs) may corrupt configuration memory, processing logic, or intermediate feature maps generated during neural network inference. Because deep learning algorithms involve millions of arithmetic operations and numerous intermediate activations, even a small number of bit-flips may propagate through the network and degrade prediction accuracy. The impact of such faults depends on several factors, including the location of the corrupted bit, the affected network layer, and the numerical significance of the modified value. Experimental fault-injection studies have shown that errors affecting the most significant bits often produce substantially larger degradation than those occurring in less significant positions.

To improve the robustness of AI systems operating in radiation environments, researchers have proposed combining conventional FPGA fault-tolerance techniques with machine learning-specific resilience strategies. Traditional approaches such as Triple Modular Redundancy (TMR), Error Correction Codes (ECC), and configuration scrubbing continue to provide protection against hardware-level faults. At the algorithmic level, techniques including quantization-aware training, fault-aware training, redundant inference, resilient mapping, and adaptive pruning further improve tolerance to transient errors by reducing the sensitivity of neural network parameters to individual bit-flips. Rather than relying exclusively on hardware redundancy, these methods exploit the intrinsic fault tolerance of neural networks, allowing acceptable inference accuracy to be maintained even when limited hardware faults occur.

Another important trend involves the adoption of heterogeneous computing architectures that combine embedded processors with programmable logic. In such systems, general-purpose software tasks execute on multicore ARM processors, while computationally intensive neural network operations are accelerated within FPGA fabric. This hardware–software co-design provides greater flexibility than purely hardware implementations while maintaining the performance advantages of dedicated FPGA accelerators. Recent System-on-Chip devices such as the AMD/Xilinx Zynq UltraScale+ MPSoC exemplify this approach, supporting simultaneous execution of image acquisition, preprocessing, neural network inference, and communication within a single integrated platform. This architecture has become increasingly attractive for autonomous spacecraft requiring real-time decision-making with limited onboard resources.

The integration of artificial intelligence with radiation-tolerant FPGA platforms is expected to play a central role in future space exploration missions. Autonomous planetary rovers, deep-space probes, Earth observation satellites, and CubeSats will increasingly rely on onboard intelligence to reduce dependence on ground-based processing. By combining high-performance programmable hardware with advanced fault-tolerant design techniques, FPGA-based AI accelerators provide an effective balance between computational capability, flexibility, and reliability. Although significant challenges remain regarding long-term resilience under continuous radiation exposure, recent research demonstrates that carefully designed FPGA systems are capable of supporting sophisticated deep learning applications without compromising mission safety or operational efficiency.

5.5 Emerging Non-Volatile FPGA Architectures for Future Space Systems

As space missions become increasingly autonomous and computationally demanding, the limitations of conventional SRAM-based FPGA technology have become more apparent. Although SRAM FPGAs provide excellent flexibility and computational performance, their volatile configuration memory introduces several challenges for long-duration missions. Configuration data must be reloaded after every power interruption, and continuous protection mechanisms such as configuration scrubbing are required to maintain reliable operation in radiation-rich environments. These limitations have motivated significant research into non-volatile FPGA (NV-FPGA) architectures that combine the flexibility of programmable logic with the persistent data storage characteristics of non-volatile memory technologies.

Unlike traditional SRAM-based devices, non-volatile FPGAs store configuration information using emerging memory technologies such as Resistive Random Access Memory (ReRAM), Spin-Transfer Torque Magnetic RAM (STT-MRAM), and Phase Change Memory (PCM). These memories retain their stored information even when external power is removed, eliminating the need to repeatedly reload configuration data after power interruptions. This characteristic significantly reduces startup latency while improving energy efficiency, making NV-FPGAs particularly attractive for spacecraft operating under strict power constraints.

One of the most promising application areas for non-volatile FPGAs is energy-harvesting systems. Small satellites, remote sensing platforms, planetary exploration systems, and distributed sensor networks increasingly rely on intermittent energy sources such as solar panels or energy harvesting modules. Under these operating conditions, temporary power interruptions are unavoidable. Conventional FPGA systems lose both configuration and intermediate computational data whenever power is removed, forcing calculations to restart from the beginning once power becomes available again. This behaviour wastes both time and energy, reducing the overall efficiency of the system.

To overcome this limitation, Zhang et al. proposed a Data Flow Tracking FPGA (DFT-FPGA) framework that intelligently preserves only the essential intermediate computation states during power interruptions. Instead of checkpointing every register within the FPGA, the proposed architecture identifies only those data values that are required for successful computation recovery. Binary counters monitor data flow throughout the design, allowing the system to selectively save critical information into non-volatile storage before power is lost. Experimental results demonstrated that this selective checkpointing strategy substantially reduces storage overhead while shortening recovery time after power restoration.

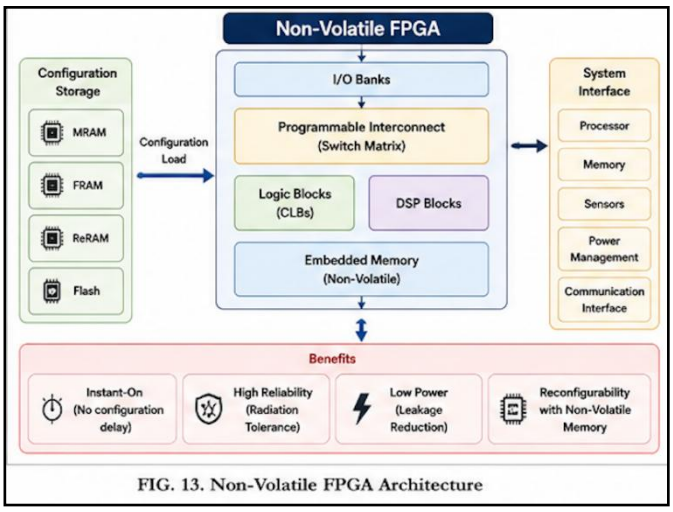

FIG. 13. Non-Volatile FPGA Architecture

Another important advantage of non-volatile FPGA technology is its contribution to overall system reliability. Since configuration information remains permanently stored within the device, dependence on external configuration memories is significantly reduced. This not only decreases system complexity but also eliminates one potential source of failure in radiation-intensive environments. Furthermore, integrating non-volatile memory directly into FPGA architecture reduces repeated configuration transfers, lowering energy consumption while improving operational efficiency during long-duration missions. Such characteristics are particularly attractive for deep-space exploration, where communication delays and limited energy availability require spacecraft to operate with high levels of autonomy.

Despite these advantages, several challenges remain before non-volatile FPGA architectures achieve widespread adoption in space applications. Emerging memory technologies generally exhibit slower write speeds than conventional SRAM and may introduce additional fabrication complexity and manufacturing costs. Integrating non-volatile memory elements with existing CMOS fabrication processes also presents technological challenges, particularly when balancing

memory endurance, write latency, power consumption, and radiation tolerance. Consequently, current research increasingly focuses on hybrid architectures that combine the computational performance of SRAM-based logic with the persistence of non-volatile storage technologies.

Looking ahead, non-volatile FPGA architectures are expected to become a key enabling technology for future intelligent spacecraft. Combined with advanced fault-tolerant techniques, artificial intelligence accelerators, and adaptive computing frameworks, these devices could support highly autonomous missions capable of maintaining computational state despite radiation events, intermittent power availability, and harsh environmental conditions. Their ability to combine energy efficiency, rapid recovery, and reliable operation makes them a promising direction for the next generation of radiation-tolerant programmable computing platforms.

Table 11:Major Applications of FPGA Technology in Space Missions.

Application Area	Primary FPGA Function	Advantages	Representative Missions
Onboard Computer	Command, control, telemetry processing	Deterministic real-time execution	Scientific satellites
Earth Observation	Image preprocessing, compression	Reduced downlink bandwidth	EO satellites
Synthetic Aperture Radar (SAR)	FFT, filtering, image formation	High-speed parallel processing	EO-ALERT prototype
Communication Systems	Encoding, modulation, encryption	High throughput with low latency	Communication satellites
Autonomous Navigation	Sensor fusion, attitude control	Parallel sensor processing	Deep-space probes
Artificial Intelligence	CNN inference, object detection	Energy-efficient edge AI	Future autonomous spacecraft

5.6 Lessons Learned from Current Space Applications

The case studies presented throughout this section illustrate the remarkable evolution of FPGA technology in modern spacecraft. Early FPGA deployments primarily focused on implementing digital control logic and communication interfaces, whereas contemporary systems execute computationally intensive workloads including Synthetic Aperture Radar processing, artificial intelligence inference, autonomous navigation, and real-time scientific data analysis. This transition reflects both advances in programmable hardware and the increasing computational demands of modern space missions.

A common observation across nearly all reported missions is that radiation tolerance cannot rely on a single mitigation technique. Instead, successful FPGA deployments consistently combine multiple protection mechanisms, including Triple Modular Redundancy, configuration scrubbing, Error Correction Codes, and partial reconfiguration. Layering these techniques provides significantly greater reliability than any individual approach while allowing designers to balance performance, power consumption, and hardware resources according to mission requirements.

Another important trend is the growing shift toward onboard intelligence. Rather than functioning solely as programmable digital hardware, FPGA platforms increasingly execute complex software-defined processing pipelines and machine learning algorithms directly within the spacecraft. This reduces communication latency, minimizes downlink bandwidth requirements, and enables autonomous decision-making during time-critical operations. Earth observation satellites, maritime surveillance missions, and future deep-space exploration systems are expected to benefit significantly from this capability.

Finally, emerging technologies such as non-volatile FPGA architectures and heterogeneous computing platforms indicate that future spacecraft will become increasingly autonomous, energy-efficient, and resilient. Although challenges related to radiation effects, power management, and design complexity remain active research topics, current developments strongly suggest that programmable logic will continue to play a central role in the next generation of intelligent space systems.

Table 12: Advantages of FPGA-Based Onboard SAR Processing.

Feature	Traditional Ground Processing	FPGA-Based Onboard Processing
Processing Location	Ground Station	Satellite
Communication Bandwidth	High	Significantly Reduced
Response Time	Minutes to Hours	Near Real-Time
Computational	Dependent on	Parallel Hardware

Performance	Downlink	Acceleration
Energy Efficiency	Not Space-Constrained	Optimized for Onboard Operation
Typical Applications	Image Reconstruction	Disaster Monitoring, Maritime Surveillance, Emergency Response

6. Future Research Directions and Emerging Trends

6.1 Artificial Intelligence for Autonomous Spacecraft

The rapid growth of artificial intelligence (AI) is transforming the way modern spacecraft operate. Traditional satellite missions relied heavily on ground stations for mission planning, data interpretation, and operational decision-making. Spacecraft primarily functioned as data acquisition platforms, continuously transmitting information to Earth for processing. Although this architecture has supported numerous successful missions, it introduces unavoidable communication delays and limits the ability of spacecraft to respond independently to unexpected events. As future missions venture farther from Earth and generate increasingly large volumes of scientific data, continuous dependence on ground-based processing becomes impractical. Consequently, spacecraft are gradually evolving into intelligent autonomous systems capable of analysing data, making decisions, and adapting their behaviour during flight.

Artificial intelligence enables spacecraft to perform many of these tasks directly onboard. Machine learning algorithms can automatically recognise patterns within

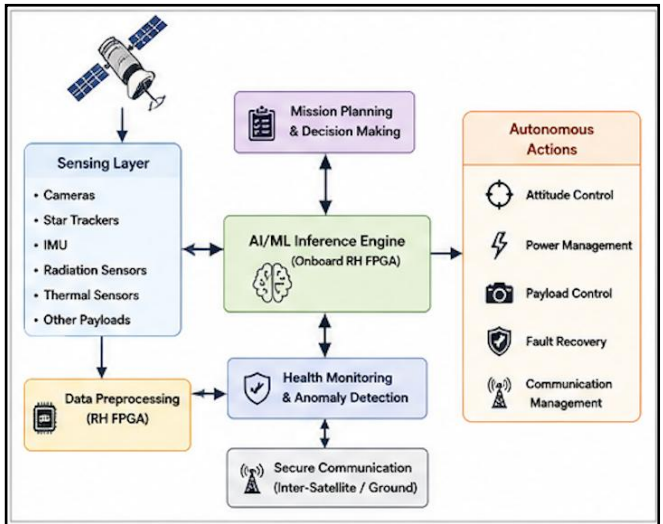

FIG. 15. AI-Enabled Autonomous Spacecraft Architecture

sensor data, identify anomalies, classify terrain, detect spacecraft faults, and optimise operational parameters without requiring continuous human supervision. For Earth observation satellites, AI models can distinguish between ships, roads, buildings, vegetation, flood zones, and wildfire regions immediately after image acquisition. Instead of transmitting complete datasets to Earth, the spacecraft sends only processed information, significantly reducing communication bandwidth while improving response time during emergency situations. Similar approaches are increasingly being investigated for planetary exploration, autonomous docking, robotic

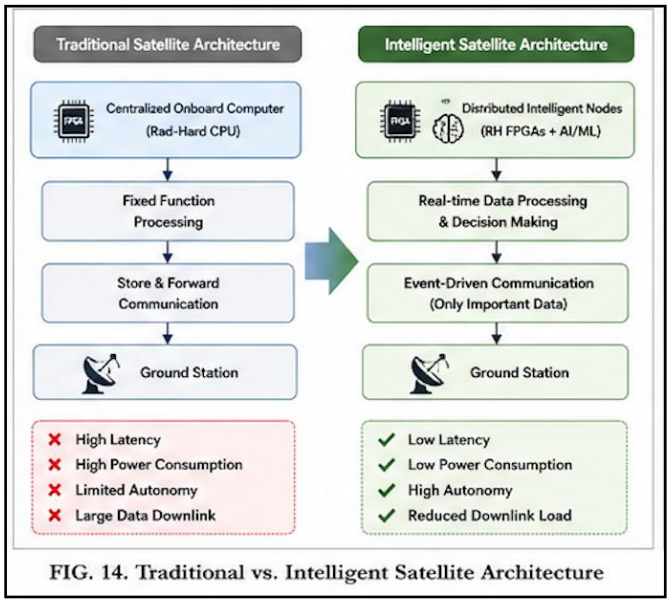

FIG. 14. Traditional vs. Intelligent Satellite Architecture

navigation, and scientific payload management.

The successful deployment of AI in space depends heavily on high-performance yet energy-efficient computing hardware. Conventional processors often struggle to execute deep neural networks within the strict power limitations of satellite platforms, whereas Graphics Processing Units (GPUs) generally consume more energy than many spacecraft can provide. FPGA-based accelerators offer a practical compromise by implementing neural network operations directly in programmable hardware, allowing highly parallel computation while maintaining relatively low power consumption. Recent FPGA platforms integrate embedded processors with programmable logic, enabling computationally intensive inference operations to execute in dedicated hardware while mission management and communication software remain on general-purpose processors. This heterogeneous architecture provides both computational flexibility and improved energy efficiency.

Table 13: AI Applications in FPGA Systems

Application Area	AI Function	FPGA Contribution	Expected Benefit
Earth Observation	Image Classification, Change Detection	CNN / DNN Acceleration	Reduced downlink bandwidth
Planetary Exploration	Terrain Recognition, Path Planning	Parallel Vision Processing	Autonomous rover navigation
Spacecraft Health Monitoring	Anomaly Detection, Fault Diagnosis	Real-time Inference Engine	Predictive maintenance & higher reliability
Deep-Space Missions	Mission Planning, Event Detection	AI Acceleration	Reduced communication dependence
Satellite Constellations	Resource Scheduling, Traffic Prediction	Adaptive Computing Acceleration	Improved Operational efficiency

Despite these advantages, introducing artificial intelligence into spacecraft also creates new reliability challenges. Radiation-induced bit flips occurring within neural network parameters, intermediate feature maps, or accelerator hardware may degrade prediction accuracy or produce incorrect decisions. Consequently, future AI-enabled spacecraft will require closer integration between hardware fault-tolerance mechanisms and algorithm-level robustness. Traditional techniques such as Triple Modular Redundancy, configuration scrubbing, and Error Correction Codes will continue to protect programmable hardware, while AI-specific methods including fault-aware training, redundant inference, quantization-aware optimisation, and adaptive model verification will improve resilience at the software level. The convergence of reliable hardware and resilient artificial intelligence is therefore expected to become one of the defining research directions for future space computing systems.

Another important trend is the transition from rule-based spacecraft control toward adaptive autonomous systems. Instead of executing predefined operational sequences, future spacecraft are expected to continuously evaluate mission conditions, estimate environmental changes, and optimise resource allocation without waiting for commands from Earth. AI-assisted scheduling could dynamically distribute computational workloads among onboard processors and FPGA accelerators while simultaneously monitoring system health and energy availability. Such capabilities would be particularly valuable for deep-space exploration, where communication delays of several minutes or even hours prevent immediate intervention by ground operators. As mission complexity continues to increase, autonomous decision-making will become an essential capability rather than an optional enhancement.

The integration of AI with radiation-tolerant FPGA technology therefore represents far more than an incremental improvement in onboard computing performance. It signifies a shift toward intelligent spacecraft capable of interpreting information, prioritising observations, and responding autonomously to changing mission conditions. Continued advances in FPGA architecture, machine learning algorithms, and fault-tolerant system design are expected to further expand the role of AI across future Earth observation satellites, planetary probes, lunar exploration missions, and autonomous space robotics.

6.2 Digital Twin Technology for Spacecraft Health Monitoring

The increasing complexity of modern spacecraft has created a growing demand for intelligent health monitoring systems capable of predicting failures before they affect mission performance. Traditional spacecraft health management relies primarily on telemetry transmitted to ground stations, where engineers analyse sensor readings and determine appropriate corrective actions. Although this approach has proven successful for many missions, it becomes increasingly difficult as spacecraft operate farther from Earth, generate larger volumes of operational data, and execute more autonomous functions. Communication delays associated with lunar, Martian, and deep-space missions further reduce the effectiveness of continuous ground-based supervision. Consequently, researchers are exploring Digital Twin technology as a next-generation framework for autonomous spacecraft health management and predictive maintenance.

A **Digital Twin** is a dynamic virtual representation of a physical system that continuously receives operational data from sensors embedded within the real system. Unlike conventional simulation models, which are typically used only during design or testing, a Digital Twin remains synchronised with the physical system throughout its operational lifetime. Sensor measurements collected from the spacecraft are transmitted to the virtual model, allowing it to reproduce current operating conditions, estimate component degradation, predict

future failures, and evaluate alternative operational strategies without interfering with the actual mission.

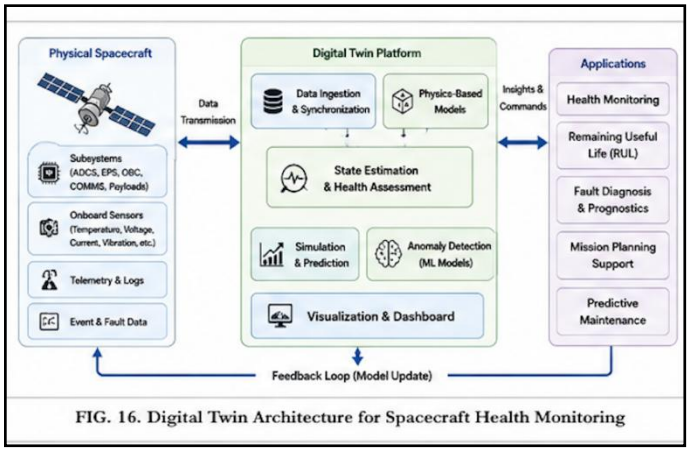

FIG. 16. Digital Twin Architecture for Spacecraft Health Monitoring

This continuous interaction between physical hardware and virtual models enables spacecraft operators to identify abnormal behaviour at a much earlier stage than traditional monitoring techniques.

Table 14: Digital Twin Functions in Radiation-Hardened FPGA Systems

Digital Twin Function	Monitored Parameter	Expected Benefit
Health Monitoring	Temperature, Voltage, Power, Clock Stability	Continuous system awareness
Radiation Monitoring	SEU Rate, Configuration Errors, TID	Early fault detection & trend analysis
Predictive Maintenance	Component Degradation, Error Trends	Reduced mission risk & downtime
Performance Optimization	FPGA Utilization, Throughput, Latency, Power	Improved energy efficiency
Autonomous Recovery	Fault Statistics, Recovery Success Rate	Intelligent reconfiguration & high availability
Mission Planning Support	System Health Trends, Resource Prediction	Extended mission lifetime

Within FPGA-based spacecraft, Digital Twin technology offers particularly attractive possibilities because programmable hardware plays a central role in mission-critical processing tasks. Radiation-induced degradation often develops gradually through repeated exposure to energetic particles, eventually affecting timing behaviour, configuration memory, power consumption, and computational accuracy. Instead of waiting until these effects produce functional failures, a Digital Twin could continuously monitor operational parameters such as configuration memory error rates, device temperature, power consumption, clock stability, and fault recovery statistics. Machine learning algorithms embedded within the virtual model could analyse these measurements to estimate remaining useful life, detect abnormal operating conditions, and recommend corrective actions before critical failures occur. Such predictive capability would significantly improve mission reliability while reducing dependence on manual intervention from ground control.

One of the most important advantages of Digital Twin technology is its ability to combine information obtained from multiple spacecraft subsystems into a unified health assessment. Rather than evaluating FPGA behaviour independently, the virtual model simultaneously considers sensor measurements from power systems, thermal management units, communication subsystems, attitude control systems, and scientific payloads. This holistic perspective enables the identification of interactions that might otherwise remain undetected. For example, an increase in FPGA temperature combined with rising configuration memory upset rates may indicate accelerated radiation-induced degradation requiring immediate reconfiguration or workload redistribution. By analysing these relationships continuously, the Digital Twin provides decision support that extends beyond conventional fault detection techniques.

Recent research has further demonstrated the value of Digital Twins for **predictive fault diagnosis**. Although the wind turbine study focuses on industrial machinery rather than spacecraft, its methodology illustrates how real-time operational data can be integrated with physics-based models and machine learning algorithms to identify developing faults before catastrophic failure occurs. The proposed framework continuously updates the virtual model using sensor information collected from the physical system, allowing degradation trends to be estimated throughout normal operation. A similar strategy could be adapted for radiation-hardened FPGA systems by continuously monitoring error accumulation, power fluctuations, timing variations, and fault mitigation activity during space missions. Instead of simply reporting that an error has occurred, the Digital Twin would estimate the probability of future failures and recommend appropriate recovery actions such as partial reconfiguration, workload redistribution, or preventive maintenance scheduling.

The integration of Digital Twins with artificial intelligence further expands their potential capabilities.

Machine learning algorithms can analyse large volumes of historical telemetry to identify complex relationships between environmental conditions and hardware degradation that are difficult to capture using analytical models alone. As additional operational data become available throughout the mission, prediction models can be continuously refined, improving both diagnostic accuracy and reliability. Future spacecraft may therefore employ Digital Twins not only to monitor hardware health but also to optimise power consumption, schedule computational workloads, evaluate alternative mission scenarios, and support autonomous decision-making during unexpected events. Combined with FPGA-based AI accelerators discussed in the previous section, Digital Twins represent an important step toward fully autonomous spacecraft capable of managing their own operational health.

Despite these promising developments, several technical challenges must be addressed before Digital Twin technology becomes routinely deployed in space systems. Constructing an accurate virtual representation of a spacecraft requires detailed mathematical models describing electrical behaviour, thermal dynamics, radiation effects, and computational performance under varying environmental conditions. Maintaining continuous synchronisation between the physical spacecraft and its virtual counterpart also demands reliable telemetry transmission and efficient onboard data processing. Furthermore, validating prediction models under the highly variable conditions encountered during long-duration space missions remains a significant research challenge. These issues highlight the need for interdisciplinary collaboration involving aerospace engineering, electronics, computer science, and artificial intelligence.

Nevertheless, the concept of Digital Twins represents a major shift in spacecraft operations. Rather than responding to failures after they occur, future missions will increasingly focus on anticipating degradation, preventing faults before they develop, and continuously optimising system performance throughout the mission lifetime. For radiation-hardened FPGA systems, this proactive approach could significantly enhance reliability while enabling increasingly complex autonomous missions beyond Earth orbit.

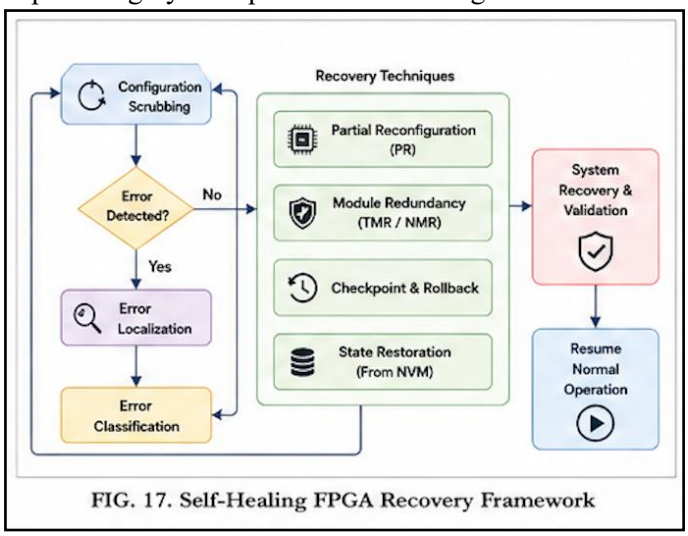

FIG. 17. Self-Healing FPGA Recovery Framework

6.3 Self-Healing FPGA Architectures

Future space missions will require computing platforms that are not only resistant to radiation-induced faults but also capable of recovering from failures autonomously. Current fault-tolerant FPGA systems primarily depend on predefined protection mechanisms such as Triple Modular Redundancy (TMR), Error Correction Codes (ECC), and configuration scrubbing. While these techniques effectively improve system reliability, they generally operate according to fixed rules and require either periodic maintenance or intervention from onboard control software. As spacecraft become increasingly autonomous and communication delays increase during deep-space exploration, future FPGA platforms must evolve beyond passive fault tolerance toward **self-healing computing systems** capable of detecting, diagnosing, and correcting failures with minimal external assistance.

A self-healing FPGA continuously monitors its own operational status and automatically initiates recovery procedures whenever abnormal behaviour is detected. Rather than simply identifying an error, the system determines the location and severity of the fault, selects an appropriate recovery strategy, and restores normal operation without interrupting the overall mission. Such architectures combine hardware redundancy, intelligent monitoring, adaptive reconfiguration, and machine learning algorithms into a unified fault-management framework. The objective is not merely to survive radiation-induced events but to maintain uninterrupted computational capability throughout extended mission durations.

Dynamic Partial Reconfiguration (DPR) represents one of the most promising technologies enabling self-healing FPGA systems. Unlike complete device reconfiguration, which temporarily suspends all system operations, partial reconfiguration allows only the damaged logic region to be replaced while the remaining circuitry continues executing normally. When integrated with fault detection mechanisms, DPR significantly reduces recovery time and improves overall system availability. Future spacecraft could automatically isolate malfunctioning processing modules, reload the affected configuration frames, verify successful recovery, and

resume normal operation without requiring communication with ground stations. Such capability is particularly valuable for long-duration missions where communication delays make immediate external intervention impossible.

Artificial intelligence is expected to further enhance self-healing architectures by improving fault diagnosis and recovery decisions. Machine learning models trained using historical fault data may identify subtle behavioural changes preceding hardware failures and estimate the most appropriate corrective action. Rather than relying exclusively on predefined thresholds, AI-based monitoring systems could recognise complex relationships between temperature variations, power consumption, configuration memory errors, and computational performance. This adaptive capability would enable spacecraft to anticipate failures before they become mission-critical and optimise recovery procedures according to current operating conditions.

Self-healing architectures may also benefit from close integration with Digital Twin technology. As discussed in the previous section, a Digital Twin continuously maintains a virtual representation of the spacecraft and predicts future degradation trends. Information generated by the Digital Twin can be used to determine whether a detected fault requires immediate recovery, gradual workload redistribution, or preventive reconfiguration before functional failure occurs. This combination of predictive analytics and autonomous recovery transforms spacecraft fault management from a reactive process into a proactive reliability strategy.

Future FPGA devices are also expected to incorporate adaptive redundancy techniques. Conventional Triple Modular Redundancy permanently duplicates critical hardware modules regardless of current operating conditions, resulting in substantial resource and power overhead. Adaptive redundancy, by contrast, dynamically adjusts the level of protection according to environmental radiation intensity, mission phase, or application criticality. During periods of low radiation exposure, redundant modules may be temporarily disabled to conserve energy, whereas increased redundancy can be activated automatically during solar particle events or high-radiation orbital regions. Such adaptive protection strategies provide a better balance between reliability and resource utilisation than static redundancy schemes.

Another promising research direction involves distributed self-healing architectures for satellite constellations. Instead of treating each spacecraft as an isolated system, future constellations may cooperate by sharing health information, fault statistics, and recovery strategies through inter-satellite communication links. If one spacecraft experiences abnormal behaviour, neighbouring satellites could assist in validating fault predictions or temporarily assume critical computational tasks while recovery procedures are executed. This collaborative approach extends the concept of self-healing beyond individual devices to entire space networks.

Despite these promising developments, several challenges remain before fully autonomous self-healing FPGA systems become operational. Reliable fault diagnosis requires accurate classification of transient, intermittent, and permanent faults under highly dynamic radiation conditions. Dynamic reconfiguration mechanisms must also guarantee that recovery operations themselves do not introduce additional failures or compromise mission safety. Furthermore, integrating artificial intelligence, Digital Twins, and adaptive hardware management significantly increases system complexity, requiring rigorous verification and validation before deployment in safety-critical missions.

Nevertheless, self-healing architectures represent one of the most important future research directions for radiation-hardened FPGA systems. By combining intelligent monitoring, adaptive redundancy, dynamic partial reconfiguration, and predictive analytics, future spacecraft will be capable of maintaining reliable computation despite continuous exposure to radiation and harsh environmental conditions. Such capabilities are expected to play a fundamental role in enabling long-duration lunar missions, autonomous planetary exploration, and deep-space scientific investigations.

6.4 Open Research Challenges

Despite the significant progress achieved in radiation-hardened FPGA technology, several challenges continue to limit the deployment of highly autonomous computing platforms in future space missions. As semiconductor manufacturing advances toward increasingly smaller technology nodes, FPGA devices become more susceptible to radiation-induced disturbances. Reduced transistor dimensions improve computational performance and energy efficiency but simultaneously decrease the critical charge required to

trigger Single Event Upsets (SEUs), increasing the probability of transient and permanent faults.

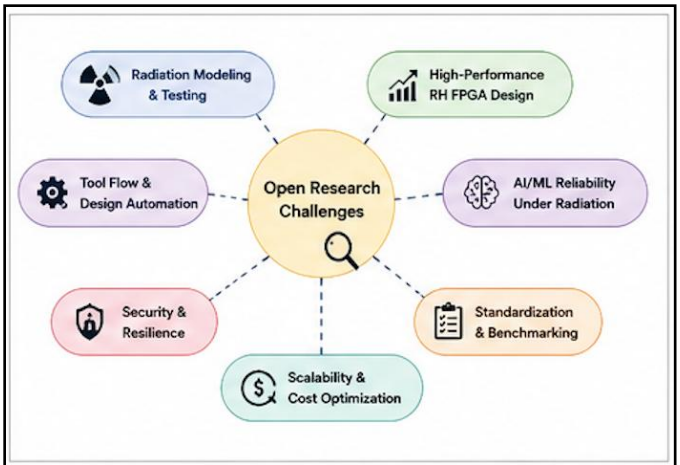

FIG. 18. Open Research Challenges in RH FPGA for Space Applications

Consequently, maintaining reliable operation in harsh radiation environments will require increasingly sophisticated protection strategies that combine hardware resilience, adaptive software techniques, and intelligent system management.

Another major challenge lies in balancing computational performance with resource utilisation. Modern space applications increasingly demand onboard execution of artificial intelligence, image processing, autonomous navigation, and scientific data analysis. Supporting these workloads often requires additional redundancy, error correction, and recovery mechanisms, all of which consume valuable FPGA resources and increase power consumption. Developing architectures capable of providing high computational throughput while maintaining acceptable reliability and energy efficiency therefore remains a critical research objective.

The verification of intelligent fault-tolerant systems also presents an important challenge. Emerging approaches incorporating artificial intelligence, Digital Twins, and adaptive recovery mechanisms significantly increase system complexity compared with traditional deterministic designs. Validating such systems under realistic radiation conditions requires comprehensive fault injection experiments, hardware-in-the-loop simulations, and long-duration operational testing. Establishing standardised evaluation methodologies will therefore become increasingly important as autonomous FPGA systems transition from research laboratories to operational spacecraft.

Digital Twin technology introduces additional research challenges related to model accuracy, computational cost, and real-time synchronisation. A Digital Twin must accurately represent the continuously changing physical state of the spacecraft while simultaneously processing large volumes of telemetry data. Achieving this level of fidelity requires efficient mathematical models, reliable communication between physical and virtual systems, and adaptive algorithms capable of updating predictions throughout the mission lifetime. Future research should therefore focus on improving Digital Twin scalability while reducing computational overhead for onboard deployment.

Finally, emerging non-volatile FPGA technologies, heterogeneous computing platforms, and adaptive reconfiguration frameworks offer promising opportunities but remain relatively immature for large-scale space deployment. Continued collaboration between academia, industry, and space agencies will be essential for validating these technologies under representative operational conditions and establishing design methodologies suitable for future long-duration missions.

6.5 Future Outlook

The continued evolution of space exploration will require computing systems capable of delivering significantly higher computational performance while maintaining dependable operation under extreme environmental conditions. Radiation-hardened FPGA technology has already established itself as a key enabling platform for onboard signal processing, autonomous navigation, scientific payload management, and artificial intelligence acceleration. However, future spacecraft will require considerably more than high-performance programmable hardware. They will demand intelligent computing platforms capable of continuously monitoring their own operational health, predicting hardware degradation, and autonomously recovering from radiation-induced failures without human intervention.

Emerging technologies such as Digital Twins, self-healing FPGA architectures, adaptive redundancy, and AI-assisted fault management represent important steps toward this vision. Rather than treating fault tolerance as an isolated hardware feature, future spacecraft are expected to integrate predictive analytics, machine learning, and dynamic system reconfiguration into a unified reliability framework. Such systems will

continuously evaluate environmental conditions, optimise computational resources, anticipate potential failures, and adapt their behaviour according to changing mission requirements.

At the same time, advances in heterogeneous computing platforms and non-volatile FPGA architectures are expected to further improve energy efficiency, reduce recovery latency, and support increasingly autonomous missions. These developments will enable spacecraft to perform complex onboard processing tasks that currently require extensive ground-based computation, reducing communication bandwidth while improving responsiveness during time-critical operations.

Table 15: Reliability and Autonomous Recovery Technologies for FPGA Systems

Technology	Primary Function	Advantages	Challenges
Dynamic Partial Reconfiguration	Replace/Isolate faulty logic regions	Reduced downtime, High availability	Reconfiguration latency
AI-Based Fault Diagnosis	Predict & classify fault types	Early detection, Higher accuracy	Training data & model validation
Adaptive Redundancy	Adjust redundancy level dynamically	Energy/resource optimization	Control complexity, Overhead
Digital Twin Integration	Predict degradation & system health	Proactive maintenance, Decision support	Model accuracy, Real-time sync
Autonomous Recovery Manager	Coordinate recovery actions	Minimal human intervention	Verification for safety-critical use

Although numerous technical challenges remain, the overall direction of research clearly indicates a transition from conventional fault-tolerant hardware toward intelligent, self-managing computing systems. Future radiation-hardened FPGA platforms will not simply survive the harsh space environment; they will actively adapt to it. This evolution is expected to play a crucial role in enabling long-duration lunar missions, Mars exploration, autonomous satellite constellations, and future deep-space scientific missions.

7. Conclusion

Field-Programmable Gate Arrays (FPGAs) have become indispensable components of modern spacecraft owing to their flexibility, high computational capability, and ability to execute complex parallel processing tasks. Their applications have expanded from traditional onboard control systems to advanced functions such as Synthetic Aperture Radar (SAR) processing, artificial intelligence acceleration, autonomous navigation, scientific payload management, and real-time communication. However, the harsh space radiation environment continues to pose significant challenges to the reliable operation of FPGA-based systems. Radiation-induced phenomena including Total Ionizing Dose (TID), Single Event Upsets (SEUs), Single Event Latch-up (SEL), and other Single Event Effects (SEEs) can degrade device performance, corrupt configuration memory, and compromise mission-critical operations. Ensuring dependable FPGA operation under these conditions therefore remains one of the primary objectives of space electronics research.

This review has presented a comprehensive overview of the current state of radiation-hardened FPGA technology, beginning with the fundamental characteristics of the space radiation environment and the mechanisms through which energetic particles interact with semiconductor devices. The review discussed both Radiation Hardening by Process (RHBP) and Radiation Hardening by Design (RHBD), highlighting the advantages and limitations of various FPGA technologies, including SRAM-based, Flash-based, anti-fuse, and Commercial-Off-The-Shelf (COTS) devices. A comparative analysis demonstrated that the choice of FPGA architecture depends strongly on mission duration, computational requirements, radiation exposure, and system-level design constraints.

The review further examined the principal fault-mitigation techniques currently employed to improve FPGA reliability in radiation-intensive environments. Techniques such as Triple Modular Redundancy (TMR), configuration scrubbing, Error Correction Codes (ECC), partial reconfiguration, and hybrid fault-tolerant architectures were discussed in detail. While each technique offers specific advantages, the literature consistently indicates that no single solution provides complete protection against radiation-induced failures. Instead, modern spacecraft increasingly employ multi-layered fault-tolerance strategies that combine hardware redundancy, error correction, and dynamic recovery mechanisms to achieve the reliability required for long-duration missions.

A significant contribution of this review has been the discussion of real-world FPGA applications in

contemporary space missions. Case studies involving Earth observation satellites, onboard Synthetic Aperture Radar processing, artificial intelligence acceleration, and non-volatile FPGA architectures illustrate the rapid evolution of programmable logic from simple digital control devices to powerful onboard computing platforms. These developments demonstrate that FPGA technology is becoming central to enabling autonomous spacecraft capable of processing large volumes of scientific data directly in orbit while reducing communication latency and bandwidth requirements.

The review also explored emerging research directions that are expected to shape the next generation of spaceborne computing systems. Technologies such as Artificial Intelligence (AI), Digital Twin frameworks, self-healing FPGA architectures, adaptive fault management, and intelligent health monitoring represent a shift from conventional fault-tolerant hardware toward autonomous, self-managing computing platforms. These approaches seek not only to tolerate radiation-induced faults but also to predict, diagnose, and recover from failures with minimal human intervention. Such capabilities will become increasingly important as future missions target the Moon, Mars, asteroid exploration, and deep-space environments where communication delays and operational complexity demand higher levels of onboard autonomy.

Despite the considerable progress achieved in radiation-hardened FPGA design, several challenges remain unresolved. Continued technology scaling increases device sensitivity to radiation, while the growing adoption of heterogeneous computing platforms and AI accelerators introduces additional verification and reliability concerns. Furthermore, the practical implementation of Digital Twins, autonomous recovery systems, and adaptive fault-tolerant architectures requires further validation under realistic space radiation conditions. Addressing these challenges will require close collaboration between researchers, semiconductor manufacturers, and space agencies to develop robust design methodologies, standardized testing procedures, and next-generation radiation-resilient computing platforms.

In conclusion, radiation-hardened FPGA technology will continue to play a pivotal role in future space exploration. By integrating advances in fault-tolerant hardware, intelligent software, artificial intelligence, Digital Twin technology, and autonomous system management, future FPGA-based platforms are expected to provide unprecedented levels of computational capability, reliability, and adaptability. These innovations will not only improve the resilience of spacecraft operating in harsh radiation environments but also enable increasingly autonomous missions capable of supporting scientific discovery, planetary exploration, and long-duration human spaceflight. Consequently, radiation-hardened FPGA systems are expected to remain a cornerstone technology for the next generation of intelligent and reliable spaceborne electronic systems.

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