

Bipolar Digital Logic Local Oscillator for Bitstream Photon Counting Chirped AM Lidar

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Abstract

This paper is a follow-up to a previous paper introducing the new bitstream Photon Counting Chirped Amplitude Modulation (AM) Lidar (PC-CAML) with a Digital Logic Local Oscillator (DLLO) concept. In that previous work, the DLLO was unipolar. In this paper, a new bipolar DLLO for the bitstream PC-CAML is introduced (patent pending).

The bipolar DLLO retains the key advantages of the unipolar DLLO for the bitstream PC-CAML since it also replaces bulky, power-hungry, and expensive wideband RF analog electronics with digital components that can be implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) read-out integrated circuits (ROICs) to make the bitstream PC-CAML with a DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

In addition, the bipolar DLLO improves the electrical power signal-to-noise ratio (SNR) of the bitstream PC-CAML by about 2.5 dB compared to that of the unipolar DLLO as shown by the theoretical and Monte Carlo simulation results presented in this paper. Theoretically, there should be a 3 dB improvement for the bipolar DLLO from the elimination of the signal power loss to the DC component of the intermediate frequency (IF) spectrum that occurs with the unipolar DLLO. However, this improvement is partially offset by a higher quantization noise for the bipolar DLLO compared to that of the unipolar DLLO as explained in this paper.

This paper introduces the bipolar DLLO for bitstream PC-CAML concept and presents the initial signal-to-noise ratio (SNR) theory with comparisons to Monte Carlo simulation results.

1. Bipolar DLLO for Bitstream PC-CAML Concept

The patented photon counting chirped amplitude modulation lidar (PC-CAML) concept has been extensively discussed previously. [ref 1-14] In previous PC-CAML systems, the local oscillator (LO) has been a radio-frequency (RF) analog signal applied using expensive, bulky, and power hungry RF analog electronics either in post-detection mixing or via opto-electronic mixing (OEM) at the photon counting detector, including gating of the detector, or applied via pre-detection mixing using an optical intensity modulator. The reader is referred to references 1-14 for more details on the theory and practice for the traditional PC-CAML system.

This paper is a follow-up to a previous paper introducing the new bitstream Photon Counting Chirped Amplitude Modulation Lidar (PC-CAML) with a Digital Logic Local Oscillator (DLLO) concept.[ref 15] The reader is encouraged to read that paper [ref 15] prior to proceeding to read this paper. In that previous work, the DLLO was unipolar. In this paper, a new bipolar DLLO for the bitstream PC-CAML is introduced (patent pending). [ref 16]

The bipolar DLLO retains the key advantages of the unipolar DLLO for the bitstream PC-CAML stated in the previous paper [ref 15] since it also replaces bulky, power-hungry, and expensive

wideband RF analog electronics with digital components that can be implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) read-out integrated circuits (ROICs) to make the bitstream PC-CAML with a DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

In addition, the bipolar DLLO improves the electrical power signal-to-noise ratio (SNR) of the bitstream PC-CAML by about 2.5 dB compared to that of the unipolar DLLO as shown by the theoretical and Monte Carlo simulation results presented in this paper. Theoretically, there should be a 3 dB improvement for the bipolar DLLO from the elimination of the signal power loss to the DC component of the intermediate frequency (IF) spectrum that occurs with the unipolar DLLO. However, this improvement is partially offset by a higher quantization noise level for the bipolar DLLO compared to that of the unipolar DLLO as explained in this paper.

For the bipolar DLLO, the chirped square wave LO consists of a single sign bit representing the polarity of the LO. The output of the photon counting detector receiving a chirped AM signal is a constant amplitude unipolar count. This signal count pulse is input to an edge-triggered pulse detector which outputs a very short single value bit unipolar digital logic level pulse. The digital mixing of the bipolar DLLO and the unipolar signal logic level count pulses is implemented by assigning in each clock time interval the DLLO's sign bit to the sign bit of a 2-bit signed binary data register for which one bit represents a sign and the other bit represents a binary value, and assigning the signal's value bit to the binary value bit of this 2-bit signed binary data register, as shown in figure 1 (a.). The wideband, high speed 2-bit signed binary digital data from this 2-bit register can be either directly sent to storage and fully digitally processed, or sent through an analog or digital low/band pass filter in the IF band, the output of which is either digitized by a low sample rate analog-to-digital converter (ADC), or digitally down sampled to a low sample rate, respectively, as shown in figure 1 (a.). The low sample rate digital data is then sent to storage and digitally processed by the usual methods for chirped AM lidar.

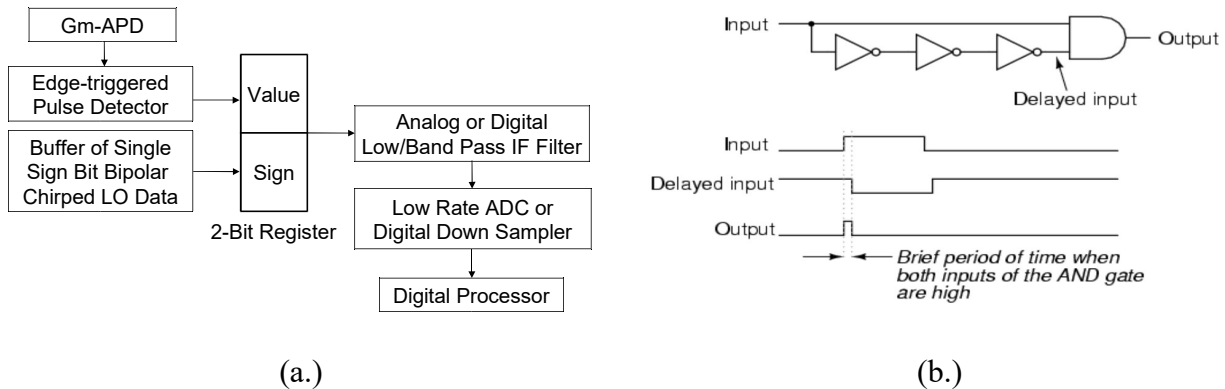


Figure 1. (a.) Bipolar DLLO for Bitstream PC-CAML Concept Diagram and (b.) Example Edge-triggered Pulse Detector circuit from the online textbook [Lessons in Electric Circuits](https://www.allaboutcircuits.com/textbook/digital/chpt-10/edge-triggered-latches-flip-flops/), at <https://www.allaboutcircuits.com/textbook/digital/chpt-10/edge-triggered-latches-flip-flops/>, by Tony R. Kuphaldt and Dennis Crunkilton, License: <https://www.gnu.org/licenses/dsl.html>.

Note that although the description of the bipolar DLLO and signal count digital mixing is given above in terms of a sign bit and a value bit for simplicity and clarity, the 2-bit signed binary data can also use other representations of signed binary numbers, such as one's or two's complement representations, with the digital processing procedures appropriate to those representations.

An example circuit for the edge-triggered pulse detector is shown in figure 1 (b.). The edge-triggered pulse detector allows the single-bit signal pulses to be much shorter than the count pulses output by the Gm-APD, which can be longer than desired due to the Gm-APD dead-time. The edge-triggered pulse detector's output pulse can be as short as a single clock pulse as long as the rising edge of the Gm-APD's count pulse is shorter than a clock pulse, and the delay on the delayed input in the edge-triggered pulse detector circuit is shorter than a clock pulse. Other types of edge-triggered pulse circuits may be used, or the edge-triggered pulse circuit can be eliminated if the Gm-APD output count pulses are short enough.

1.1 Key Advantages of the Bipolar DLLO in Bitstream PC-CAML

The key advantages of the bipolar DLLO in the bitstream PC-CAML are as follows:

1. The bipolar DLLO can be implemented in the unit cells of a photon counting receiver's readout integrated circuit (ROIC) by adding a 2-bit register for signed binary data.
2. The signal count and LO sign data each consist of just a stream of single-bit binary data.
3. The bipolar DLLO eliminates the need for bulky, power-hungry, and expensive wideband RF analog electronics by replacing them with digital electronics. Multi-GHz clocks and digital circuits are readily implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) ROICs.
4. The bipolar DLLO single-bit binary sign data can be computed prior to operation and stored in a buffer in each ROIC unit cell, or in a single buffer in the receiver and distributed to each ROIC unit cell in real-time during operation. The buffer can be a circular buffer for continuous repetition of the bipolar DLLO waveform.
5. The bipolar DLLO improves the electrical power SNR of the bitstream PC-CAML by about 2.5 dB compared to that of the unipolar DLLO.

These advantages make the bitstream PC-CAML with a bipolar DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

2. Bitstream PC-CAML with a Bipolar DLLO SNR Theory

The purpose of this paper is to introduce the new bipolar DLLO for the bitstream PC-CAML technique and to show through simulation results how it works. The purpose of this paper is not to develop a comprehensive theory of operation for the new technique, so the initial SNR theory presented herein has a limited range of applicability to the new technique, and an improved theory needs to be developed in future work.

The initial electrical power signal-to-noise ratio (SNR) theory used herein for the bitstream PC-CAML with a DLLO concept is derived from the SNR theory for photon counting Gm-APDs developed by Gatt, Johnson, and Nichols. [ref 19, pp. 3268-3269] and its modification for bitstream PC-CAML with an unipolar DLLO as detailed in reference 15. The theory developed by Gatt, et. al., is for detection of pulsed lidar returns. This theory, however, can be applied to the single-bit chirped AM waveform and bipolar DLLO as simulated in Mathcad^{®1} by making the following adjustments:

1 Mathcad[®] is a registered trademark of PTC Inc. or its subsidiaries in the U.S. and in other countries.

1. Reducing the SNR by a factor of 8 to account for losses due to the one-sided (aka unipolar) signal and the two-sided (aka bipolar) LO waveforms of the bitstream PC-CAML as discussed in the papers presenting the original PC-CAML concept by Redman, Ruff, and Giza [ref 2-4].
2. Adding quantization noise due to the 2-bit quantization (single value bit and single sign bit) with a bipolar intermediate frequency signal.
3. Setting the arm probability, PA, in the SNR equations of Gatt, et. al., [ref 19, pp. 3268-3269] to 1 since in the theory as used herein, the counts per matched filter impulse response time are output counts after having been subjected to the arm probability.
4. Multiplying the theoretical SNR by $10^{-0.176}$ to account for the scalloping loss due to the Hann window applied to the data in the simulations (see section 3) to reduce sidelobes.

Equation (41) from Gatt, et. al., [ref 19, p. 3269] modified as described above becomes

$$SNR_{theory} = \frac{10^{-0.176} N_s \left[1 - \left(\frac{M}{M + m_{scounts}} \right)^M \right]^2}{8 \left[1 - e^{-\left(m_{ncounts} + m_{qncounts} \right)} \left(\frac{M}{M + m_{scounts}} \right)^M \right] \left[1 - \left[1 - e^{-\left(m_{ncounts} + m_{qncounts} \right)} \left(\frac{M}{M + m_{scounts}} \right)^M \right] \right]} \quad (1.)$$

where N_s = Number of clock time interval samples accumulated over the chirp duration

M = speckle diversity

$m_{scounts}$ = average number of signal counts output by the Gm-APD per clock time interval

$m_{ncounts}$ = average number of noise counts output by the Gm-APD per clock time interval
(includes all of the additive noise sources except for quantization noise)

$m_{qncounts}$ = the average number of quantization noise counts per clock time interval.

(Note that the clock time interval equals the matched filter impulse response time and the dead-time in this theory and in the simulations discussed in section 3.)

This SNR theory does not include the effects of energy loss from the fundamental IF frequency to higher order odd harmonics and their mixing products for the chirped square wave modulation waveforms in the bitstream PC-CAML. This SNR theory also assumes 100% modulation depth for the PC-CAML signal.

2.1 Sinusoidal Modulation Depth Loss Near Saturation

As the average number of signal counts output by the Gm-APD per available clock time interval increases towards 1, the apparent modulation depth of a sinusoidal chirped AM waveform decreases due to the Gm-APD being able to output at most only a single count per dead-time which is set equal to the clock time interval in the simulations (see section 3). For the sinusoidal signal, when the average count rate is so high that a count is output for every clock time interval, the single-bit count data stream looks like that of a constant, unmodulated signal corresponding to a modulation depth of zero and therefore, the SNR goes to zero.

For the sake of brevity, this paper discusses only a chirped sinusoidal signal whereas the previous paper [ref 15] discussed both the chirped sinusoidal signal and the chirped square wave signal. However, the bipolar DLLO can also be used just as easily with a chirped square wave signal as it was for the unipolar DLLO as discussed in reference 15.

2.2 Quantization Noise with the Bipolar DLLO

Noise due to quantization must be calculated to use in the SNR theory of equation (1.). The quantization noise is computed from the Signal-to-Quantization-Noise Ratio in dB (SQNR_{dB}) given by equation 2.38 of Bjorndal [ref. 18, p. 40]:

$$\text{SQNR}_{\text{dB}} = 6.02 \cdot N_{\text{bits}} + 1.76, \text{ where } N_{\text{bits}} = \text{the number of bits of digitization.} \quad (2.)$$

The number of bits input to equation (2.) for the bipolar DLLO concept is determined as follows.

For the Bipolar DLLO multiplied by the Unipolar Signal, there are 3 states (+1, 0, -1) since +0 and -0 are equivalent, degenerate states equal to 0. Therefore, the equivalent number of bits is derived from

$$2^{N_{\text{bits}}} = 3 \implies N_{\text{bits}} \cdot \ln(2) = \ln(3) \implies N_{\text{bits}} = \ln(3)/\ln(2) = 1.5849625 \quad (3.)$$

Therefore, $\text{SQNR}_{\text{dB}}(N_{\text{bits}}=1.5849625) = 6.02 \cdot 1.5849625 + 1.76 = 11.301474 \text{ dB}$, and $\text{SQNR} = 10^{1.1301474} = 13.4942$.

Thus, the quantization noise per count is $1/13.4942$ for $N_{\text{bits}}=1.5849625$ corresponding to 3 states.

The above calculation applies to the N_{bits} quantization noise for the IF data using the unipolar DLLO with the AND logic gate digital mixer. However, Klein states and shows that "...the logic function XOR results in the negative multiplication of two bipolar bit-streams, and the logic function AND results in the multiplication of two unipolar bit-streams...For the logic operation XOR, the standard deviation is doubled in comparison to the operations OR and AND...Due to the fact that the output bit stream changes from zero to one with XOR and only from 0.5 to zero or one with OR and AND, the scaling is expected to be a factor of two of the standard deviations from OR and AND to XOR." [ref 17]

Since for the electrical power SNR, the noise is given by the variance rather than the standard deviation, the quantization noise for the bipolar DLLO is 4 times higher than that for the unipolar DLLO with the same number of quantization bits. Therefore, for the bipolar DLLO, the average number of quantization noise counts per clock time interval is given by:

$$m_{q_n_counts_avg} = 4 m_{spn_counts_avg} / 13.4942 = m_{spn_counts_avg} / 3.37355 \quad (4.)$$

where $m_{q_n_counts_avg}$ = the average number of quantization noise counts per clock time interval in the simulations

$m_{spn_counts_avg}$ = the average number of signal plus noise counts per clock time interval in the simulations.

Therefore, the average number of quantization noise counts per clock time interval for the bipolar DLLO is 1.78 times higher than that of the unipolar DLLO, which is given by $m_{spn_counts_avg}/6$. [ref 15]

In the initial SNR theory, equation (1.), $m_{qncounts}$ is set equal to the value of $m_{q_n_counts_avg}$ from equation (4.) for comparison to the simulation results.

Development of an SNR theory that includes the effects of quantization noise, aliasing, the harmonics and their mixing products, less than 100% signal modulation depth, and Gm-APD saturation for the bitstream PC-CAML that is applicable for both chirped sinusoidal and chirped square wave signals is beyond the scope of this paper and is suggested for future work.

3. Monte Carlo Simulation Results Compared to Initial SNR Theory

The equations and functions for implementing the Monte Carlo simulations of signal and noise for bitstream PC-CAML with the unipolar DLLO in Mathcad® were given in the previous paper. [ref 15]

The only changes for the bipolar DLLO simulations are as follows:

1. Simulating only a chirped sinusoidal signal instead of both a chirped sinusoidal signal and a chirped square wave signal
2. Using the sign of a bipolar chirped square wave LO (equation (5) below) instead of the unipolar chirped square wave LO
3. Using the power spectrum of the IF signal without filtering and down sampling as used in the previous paper [ref 15] since the SNR does not differ significantly before and after filtering and down sampling
4. Implementing looping over the average number of signal counts per clock time interval requiring storing the results in 3D arrays instead of 2D arrays so that the SNR plots were generated by running the Mathcad® worksheet once instead of multiple times with the value of the average number of signal counts per clock time interval being changed manually for each run as done previously. This change required reducing the number of trials in the simulations to 24 from the 64 trials used in the previous paper [ref 15] since the 3D data arrays are much larger in the current simulations and required too much memory for more than 24 trials. The results with 24 trials in the simulations indicate that 24 trials are sufficient, and the results are generated much faster.

The equation for the sign of the bipolar chirped square wave DLLO is given by

$$LO := \overrightarrow{\text{sign}\left[\sin\left[2\pi \cdot (f_0 + k_f \cdot t) \cdot t\right]\right]} \quad (5.)$$

where f_0 = the start frequency of the chirp

k_f = the temporal slope of the chirp = $(f_s - f_0)/T_{\text{chirp}}$, where f_s = the stop frequency of the chirp, and T_{chirp} = the duration of the chirp

t = the clock time from the start of the chirp

$\text{sign}[]$ = the sign of the argument.

In the simulations, the LO's sign is applied to the signal's value by multiplying the result of equation (5) and the signal value for each clock time interval.

Note that the value of the target range used in the simulations is chosen so that the resulting round-trip delay time makes the intermediate frequency (IF) for the target return signal exactly equal to some frequency sample in the power spectrum computed in the simulations to avoid complications in computing the SNR for comparison to the theory due to the target range peak straddling two frequency samples.

As for the previous paper [ref 15], the mixer output is Hann windowed to reduce sidelobes in the IF power spectrum. The Hann windowed mixer output is zero padded to eight times its original length.

The power spectrum of the Hann windowed and zero padded mixer output is computed in Mathcad® for each trial. The resulting power spectra are averaged together to produce the mean power spectrum for all the trials.

The mean noise floor of this mean power spectrum is computed over the portion of the spectrum between the target signal's fundamental IF and the third harmonic of that frequency. The value of this mean noise floor is the denominator in computing a simulation's mean SNR.

The peak value of the mean power spectrum at the fundamental IF minus the value of the mean noise floor is used as the numerator in computing a simulation's mean SNR.

Note that since the simulated data are quantized, the quantization noise is inherently included in the simulated power spectra.

The Monte Carlo simulations generate 24 realizations of signal plus noise for an up-chirp AM signal waveform. The simulations were run for the following parameter values:

$$\begin{aligned}
 N_{\text{trials}} &= \text{Number of simulation trials} = 24 & N_s &= \text{Number of clock time intervals} = 2^{13} \\
 \Delta t &= \text{Clock time interval} = 0.5 \text{ ns} & t_{\text{chirp}} &= \text{chirp duration} = 4.096 \mu\text{s} \\
 f_0 &= 100 \text{ MHz} = \text{chirp start frequency} & f_s &= 500 \text{ MHz} = \text{chirp stop frequency} \\
 \text{Target Range} &= 2.99963379 \text{ m} & \text{Target IF} &= 1.953125 \text{ MHz} \\
 M &= \text{speckle diversity} = 1 \text{ or } 1\text{E}+06 \\
 m_{n_counts_avg} &= \text{average number of additive noise counts per clock time interval} = 1\text{E}-04 \\
 m_{s_counts_avg} &= \text{average number of signal counts per clock time interval} = \text{from } 0.05 \text{ to } 1
 \end{aligned}$$

Figure 2 shows plots of the mean SNR vs. mean signal counts per clock time interval ($m_{s_counts_avg}$) from the simulations and the SNR theory for a chirped sinusoidal signal and a bipolar chirped square wave DLLO as a function of $m_{s_counts_avg}$ for $M=1$ and $M=1\text{E}+06$, with $m_{n_counts_avg}=1\text{E}-04$.

The simulation results and the SNR theory are in good agreement up to an average signal counts per clock time interval, $m_{s_counts_avg}$, of about 0.5 for $M=1$ and 0.7 for $M=1\text{E}+06$. As discussed in section 2.1, above these levels the saturation effects of power loss to the harmonics and their mixing products, and of modulation depth loss make the simulation's SNR results rollover with increasing $m_{s_counts_avg}$. The SNR theory over estimates the SNR for these high signal levels since the effects of power loss to the harmonics and their mixing products, and of modulation depth loss are not included in the SNR theory.

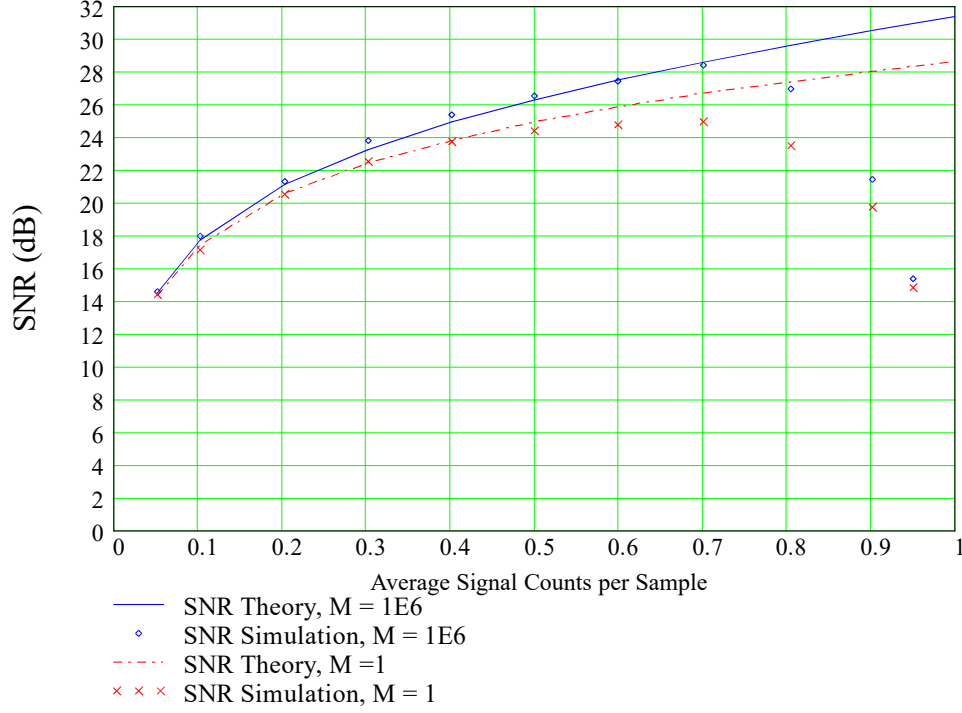


Figure 2. Comparison of SNR results for the Monte Carlo simulations for a chirped sinusoidal signal and a bipolar chirped square wave DLLO, and the SNR theory as a function of average signal counts per clock time interval, $m_{s_counts_avg}$, with the average number of noise counts per clock time interval, $m_{n_counts_avg}$, set equal to $1E-04$.

As explained in section 2.1, the roll-off in SNR at high signal levels is due to the clock time interval samples all being filled with 1's as $m_{s_counts_avg}$ approaches 1 for the chirped sinusoidal signal. This looks like a loss in modulation depth for the sinusoidal signal until at $m_{s_counts_avg} = 1$, the modulation depth goes to 0 and the signal looks like a constant level signal with no modulation.

Note that a well designed PC-CAML system using transmitter power and/or receiver throughput control to prevent saturation would operate at the lower signal levels where the initial SNR theory agrees with the simulation results. For these lower signal levels, these SNR results for the bipolar DLLO are also about 2.5 dB higher than those for the unipolar DLLO [ref 15].

4. Conclusion

The concept and initial performance modeling and simulation results for the new bipolar DLLO for the bitstream PC-CAML were presented in this paper. The results of the initial SNR theory and Monte Carlo simulations presented herein indicate that the bipolar DLLO for the bitstream PC-CAML improves the electrical power SNR by about 2.5 dB compared to that of the unipolar DLLO discussed in reference 15.

The key advantages of the bitstream PC-CAML with a bipolar DLLO are that it can be implemented in the unit cells of a photon counting lidar receiver's ROIC by adding simple digital

circuits, and the received signal and LO each consist of just streams of single-bit binary data, eliminating the need for bulky, power-hungry, and expensive wideband RF analog electronics. The bipolar DLLO single sign bit binary waveform data can be computed prior to operation and stored in a buffer in each ROIC unit cell, or in a single buffer and distributed to each ROIC unit cell in real-time during operation. The DLLO data buffer can be a circular buffer for continuous repetition of the bipolar DLLO single sign bit binary waveform data. Multi-GHz clocks and digital circuits are readily implemented in inexpensive silicon CMOS ROICs, and Multi-tens-of-GHz can be attained with more expensive technologies. The bipolar DLLO improves the electrical power SNR by about 2.5 dB compared to that of the unipolar DLLO. These advantages make the bitstream PC-CAML with a bipolar DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

5. Suggestions for Future Work

Suggestions for future work include:

1. Develop an SNR theory to include the effects of energy loss from the fundamental IF to the higher order odd harmonics and their mixing products in the power spectrum.
2. Develop an SNR theory to include the effects of less than 100% modulation depth for both chirped sinusoidal and chirped square wave signals.
3. Develop an SNR theory that works for both chirped sinusoidal and chirped square wave signals over the whole range of signal levels, including saturation levels, and for any dead-times, matched filter impulse response times, and clock time intervals.
4. Determine whether or not negative binomial plus Poisson (NBPP) distributed random sampling is alias-free for all spectra for any number of count samples accumulated.
5. For bitstream PC-CAML with a DLLO, investigate detection at a harmonic frequency as used for improved range resolution in bitstream radar.
6. Investigate techniques for suppressing harmonics and sidelobes for application to the bitstream PC-CAML with a DLLO system.
7. Investigate eliminating the high power RF electronics in the bitstream PC-CAML transmitter by using, for example, very low power photonic integrated circuit (PIC) laser sources that can be directly modulated at low voltage and current or followed with low voltage and current PIC waveguide modulators, the modulated output of which is amplified by semiconductor optical amplifiers (SOAs) or optical fiber amplifiers.[ref 20]
8. Perform lab experiments to verify the SNR theory and Monte Carlo simulation results.
9. Build and test breadboard and brassboard bitstream PC-CAML with a DLLO prototypes.

6. Acknowledgments

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