Aerosol Jet Printing of Thermally Reliable Hybrid Interconnects via a Conformal Dielectric

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Digital printing technologies offer a versatile platform to integrate bare die and discrete components in heterogeneous electronics assemblies. Such hybrid electronics, combining traditional microelectronics and printed components, offer considerable design flexibility, but pose a key technical challenge to achieve robust performance in complex topographies. Here, we demonstrate a concept for thermally robust nonplanar interconnects with a conformal architecture, in which printed silver interconnects traverse the vertical step between device planes, supported by a thin dielectric layer and compact fillet. This physical design allows effective use of thermally stable dielectrics such as benzocyclobutene, and thermal testing validates electrical performance following single-shot exposures up to 300 °C, 30 thermal cycles from room temperature to 250 °C, and 100 thermal cycles to 150 °C, performance levels that challenge conventional photocurable fillet materials. The conformal architecture scales efficiently to tall step edges (2 mm) and dense multi-step structures. This combination of compact footprint, high thermal stability, reduced material requirements, and geometric scalability establishes conformal interconnects as a compelling architecture for thermally robust hybrid electronics and advanced packaging.

1. Introduction

The growing demand for high-performance electronic systems, driven by applications in 5G/6G communications, artificial intelligence, wearable devices, autonomous systems, and advanced sensing, has intensified efforts to integrate components with diverse functionalities into compact assemblies.[1–3] This places considerable importance on advanced electronics packaging, such as heterogeneous integration, in which bare die, packaged components, and discrete devices from distinct fabrication processes are combined to achieve the necessary density, performance, and customization.[4,5] While conventional assembly methods such as wire bonding and flip-chip attachment are mature and capable, as architectures become increasingly complex there is a growing need for alternative fabrication technologies.[6,7]

Printed and additively manufactured electronics packaging concepts offer a complementary approach, enabling direct digital patterning of conductive traces with programmable routing, rapid design iteration, broad materials compatibility, and geometric versatility.[8–12] Aerosol jet printing (AJP) has received considerable interest for printed interconnects, as it offers digital patterning of micron-scale ink droplets with a resolution of 10-100 μm and a high standoff distance of 1-5 mm to support deposition on nonplanar and rough surfaces.[13,14] AJP has been demonstrated for a wide range of hybrid electronics applications, including conformal antennas and sensors,[15–17] electronics packaging,[18–20] millimeter-wave interconnects,[21,22] and die-level interconnects.[23–25]

A central challenge for additive electronics packaging is the abrupt topography and material transition between substrates, interposers, and semiconductor die. This sharp discontinuity challenges manufacturing processes, and the thermal mismatch and stress concentration at interfaces is a significant reliability concern.[12,26] One strategy to mitigate this discontinuity is to deposit a dielectric fillet or ramp as a structural support for a subsequently printed conductive trace.[27–30] A variety of fillet materials have been explored, most commonly compliant photocurable dielectrics (e.g., NEA121), but also combinations of polyimide and benzocyclobutene (BCB), applied by aerosol jet, inkjet, or dispensing methods.[24,31–35] These fillets create a gradual slope that allows continuous trace deposition, and printed interconnects leveraging fillets have been demonstrated for RF and millimeter-wave applications.[21,22,36]

Despite their demonstrated utility, fillet-based architectures carry several practical limitations. First, the ramp structure extends substantially beyond the chip footprint, consuming valuable real estate and limiting minimization of conductor length and overall assembly size. Second, depositing a sufficiently large fillet can require multiple printing passes and, in some

cases, dedicated thermal processing steps, adding time and complexity to the fabrication sequence along with greater materials use. Third, and perhaps most critical for integration with standard printed conductors, the thermal stability of common fillet materials is often insufficient: photocurable dielectrics including the commonly used NEA121 frequently have limited thermal stability,[37,38] whereas conductive inks often require sintering at moderate temperatures to achieve densification and optimal electrical conductivity.[39–41] Finally, scaling fillet structures to taller step edges, such as those arising from stacked die configurations or bulky discrete components, requires proportionally larger fillets that compound the footprint, process throughput, and thermomechanical reliability challenges.

Benzocyclobutene, commercially available as Cyclotene resin, is a thermoset polymer dielectric well established in advanced electronics packaging, known for its low dielectric constant ($\varepsilon_r \approx 2.65$), low loss tangent (~0.0008–0.002 at 1 MHz–10 GHz), high glass transition temperature ($T_g > 350$ °C), onset of thermal degradation above 450 °C under inert atmosphere, and coefficient of thermal expansion of ~42 ppm K^{-1}.[42–44] Its solubility in aromatic solvents supports liquid-phase deposition and conformal coating on complex surfaces. Recent work from our group demonstrated aerosol jet printing of a formulated BCB ink as a thermally stable, low-loss dielectric for multilayer microwave electronics, achieving loss tangent ~0.002 at 32–40 GHz and robust performance through extended thermal cycling in planar BCB/Ag multilayer structures.[45] The same thermal stability and chemical compatibility that make BCB compelling for multilayer printed electronics also support utility as a thin conformal dielectric for nonplanar interconnects.

Here, we demonstrate a conformal interconnect architecture centered on a compact dielectric layer aerosol jet printed at the substrate-die interface using a 45°-tilted substrate configuration. Using BCB, this yields a thin, conformal dielectric film that naturally rounds the lower transition between substrate and die. After curing the dielectric, silver interconnects are patterned to electrically bridge multiple levels of circuitry. We investigate the structure and electrical characteristics of the resulting conformal interconnect architecture, and validate thermal reliability to temperatures up to 300 °C. Finally, to highlight the benefits of this strategy for tall or multi-stepped surfaces, we demonstrate effective electrical interconnects over a 2 mm step and a dense multi-step structure with 50 μm conductor pitch, illustrating the scalability and versatility for complex and challenging nonplanar geometries. The benefits of this approach in expanded materials compatibility, reduced material use and print time, more efficient use of real estate, and geometric versatility establish a compelling strategy for hybrid electronics and additive electronics packaging.

2. Results and Discussion

2.1 Conformal Interconnect Architecture and Fabrication

To provide a baseline for printed interconnects, the conventional fillet or ramp architecture is illustrated schematically in Figure 1a. In this approach, a dielectric ramp material is deposited at the base of the step edge to create a gradually sloped surface bridging the height transition. Conductive traces are then printed over this ramp, with the slope ensuring a manageable transition for subsequent printing and mitigating the geometric discontinuity of the sharp edge. This approach has been demonstrated with several dielectric ramp materials, including the UV curable urethane-acrylate material NEA121 and polyimide.[27,33,46] NEA121 is a common material choice, as its mechanical compliance can accommodate moderate strain from thermal mismatch and other stresses. While careful control of the NEA121 architecture can support reasonable reliability under thermal cycling to 150 °C, exposure to higher temperatures leads to discoloration, deformation, and cracking, as shown in Figure 1b. Polymers such as BCB can provide higher degradation temperature, higher glass transition temperature, and reduced coefficient of thermal expansion, but thick fillets nonetheless fail during curing at 250 °C (Figure 1c).

Rather than approaching this purely as a materials challenge, the conformal interconnect architecture demonstrated here leverages the scaling of interfacial stress, and is schematically illustrated in Figure 1d. Instead of depositing a large ramp structure, a thin BCB layer is printed conformally over the sharp step edge. This film coats both the horizontal surfaces and the vertical sidewall of the silicon. Instead of serving primarily as a structural ramp, the resulting dielectric layer provides a smooth insulating surface to support printed conductors. Here, the thermal stability of BCB enables silver sintering at 250 °C, which supports improved mechanical and electrical characteristics for many metal nanoparticle inks.[41]

To deposit interconnects conformally across the step edge, the substrate is positioned on a 45° fixture, allowing oblique deposition on all three surfaces in a single print with a toolpath that contours the surface with a fixed standoff distance (Figure 1e-f). Figure 1g shows an optical image of the resulting conformal interconnect array after curing to 250 °C, demonstrating a uniform and regular array of printed traces spanning the step edge without visible cracking or delamination.

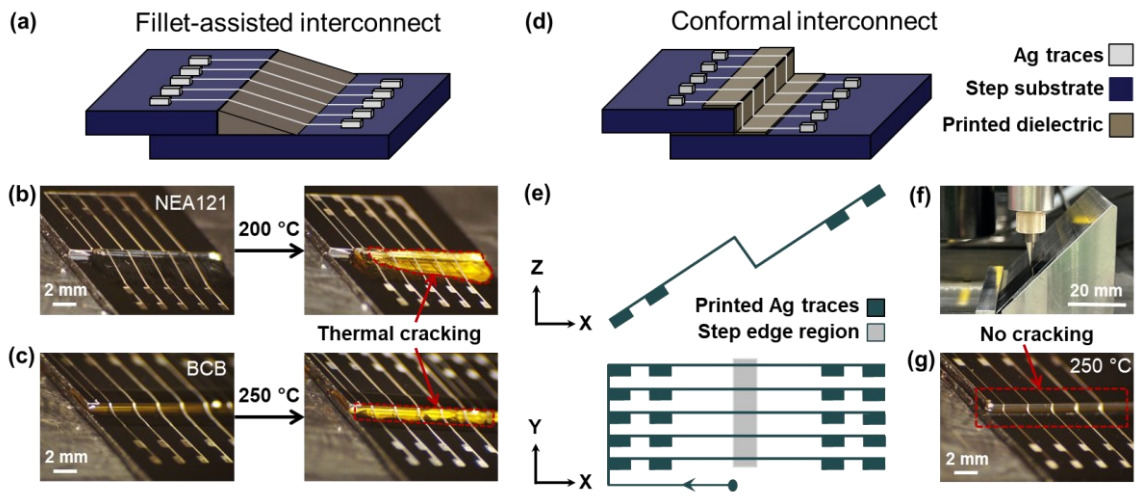

Figure 1. Concept and fabrication of printed conformal interconnects. (a) Schematic of a bulky fillet interconnect, in which a dielectric ramp bridges the height transition between parallel surfaces. (b, c) Optical images of fillet interconnects based on NEA121 and BCB, respectively, as-printed and following heating; NEA121 and BCB fillets show clear thermal failure after heating to 200 °C and 250 °C, respectively. (d) Schematic of the conformal interconnect architecture, in which a thin dielectric supports printed conductive traces that contour the step edge, with only a compact fillet at the base of the step. (e) Typical toolpath used to define the interconnect pattern, including both x-y and x-z views. (f) Optical image of the 45° fixture to hold the substrate during printing. (g) Optical image of the resulting printed conformal interconnects after heating to 250 °C.

2.2 Structural Characterization

To better understand the particular structure of the conformal interconnects, scanning electron microscopy (SEM) was performed on a cleaved sample (Figure 2). An overview SEM image (Figure 2a) shows the array of interconnects, with silver traces traversing the vertical step edge. Higher-magnification imaging of the top of the step (Figure 2b) confirms continuous trace deposition across the corner, with a slight narrowing of the line but no evidence of trace discontinuity or cracking despite the harsh geometry.

Direct side view imaging at the base of the step edge reveals the geometry of the dielectric (Figure 2c). In particular, the BCB forms a smooth, rounded geometry, evidence of flow during the BCB printing and curing process, with a measured radius of curvature of approximately 130 µm. This is important, as any overhang or gap at the interface between the dies would compromise the ability to print a continuous conductive trace, and a sharper corner can also influence aerosol impaction and ink coalescence.[47,48] Notably, this rounded geometry is

achieved without depositing a large amount of material, requiring many printing passes or precise 3D design, or building a thick structure that becomes more prone to stresses.

A magnified cross-sectional image of the vertical wall region (Figure 2d) reveals the thin BCB layer on the sidewall, indicated by red arrows, which is measured to be approximately 2.2 µm thick. This provides a smooth, chemically uniform, and electrically insulating surface for the overlying silver trace.

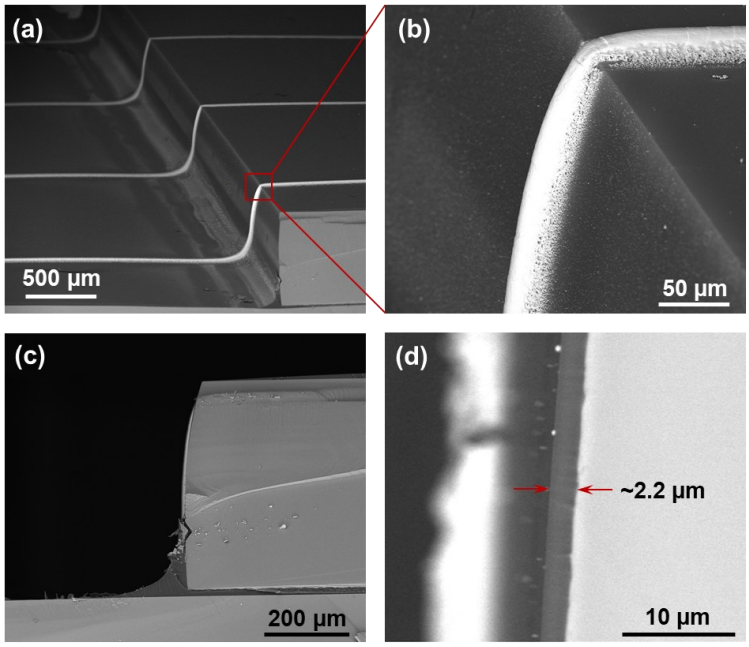

Figure 2. Scanning electron microscopy imaging of the conformal interconnect structure. (a) SEM overview of the printed interconnect array. (b) Higher-magnification SEM at the top of the step, confirming silver continuity across the sharp geometric transition. (c) Cross-section view of the step edge showing a rounded dielectric at the base. (d) Magnified SEM image of the vertical wall region, with dielectric film measuring approximately 2.2 µm thick.

2.3 Electrical Characterization

To understand the impact of this unique conformal interconnect geometry on functional characteristics, electrical testing with varying trace geometry was performed (Figure 3). As a first test, bars were printed with 2–10 printing passes to evaluate consistency with the silver thickness. On a uniform flat surface, the conductance would be expected to be directly proportional to the cross-sectional area, and thus the number of printing passes, implying uniform electrical conductivity independent of the thickness. This same behavior is observed for samples with cross-sectional area from 80–675 μm^2 (Figure 3a–b), implying no meaningful thickness dependence within this range (the bars are ~200 µm wide, implying an average

thickness range from <0.5 to >3 μm). Across all of the samples, the linear dependence of conductance on cross section area, with a fitted intercept of $-0.04 \pm 0.04\ \Omega^{-1}$, is evidence for the fabrication process consistency and limited sensitivity of electrical properties to the detailed trace cross section, supported by a strong linear relationship ($R^2 = 0.95$) observed across all 25 samples (Figure 3c). The fitted slope was $(2.15 \pm 0.10) \times 10^{-3}\ \Omega^{-1}\ \mu m^{-2}$, in which the uncertainty represents standard error from the linear regression. While this is unremarkable for a typical trace geometry, it cannot be taken for granted given the sharp geometric transition in these samples, particularly at the top corner of the step. The effective resistivity extracted from the slope of this relationship, $5.81 \pm 0.27\ \mu\Omega \cdot cm$, is consistent with values reported for sintered silver nanoparticle traces deposited by AJP on planar substrates,[49,50] suggesting that the printing and sintering quality is not compromised by the conformal printing geometry.

To get a more nuanced and quantitative assessment of the electrical resistance related to the conformal interconnect structure, length-dependent resistance test structures were fabricated (Figure 3d). This is effectively a variation of the transfer length method to isolate the resistance contribution of the step edge transition. A set of 40 interconnect traces with lengths from approximately 6–14 mm and cross-sectional areas ranging from 120–550 μm^2 were printed and characterized for electrical resistance (Figure 3e). For a given cross-sectional area, resistance scales approximately linearly with length, confirming consistent resistivity within each set of four traces. The y-intercept of these linear fits, which corresponds to the 'point resistance' or excess resistance contribution attributed to the step edge geometry itself, is extracted and plotted as a function of average line thickness in Figure 3f. The point resistance is highest for the thinnest traces, peaking at approximately 14 Ω, and decreases substantially with increasing trace thickness, averaging $0.76 \pm 0.40\ \Omega$ for traces thicker than approximately 3 μm (n = 5). This trend reflects the localized geometric constraint at the corner: for very thin traces, the step-edge region presents the narrowest cross section along the trace length, creating a locally elevated resistance contribution. For thicker traces, the corner does not restrict the cross section as severely, and the effective step-edge resistance becomes less significant relative to the bulk line resistance. This behavior confirms that the conformal interconnect architecture performs reliably for sufficiently thick traces, with point resistance becoming a minor contribution. Unfortunately, due to a supplier discontinuation of the silver ink used for the test in Figures 3a–c, which exhibited consistently lower resistance, it was not possible to perform a similar evaluation for that material. However, the total trace resistance on the order of 1 Ω for those samples, and consistent measured conductivity even for <1 μm thick samples, suggests a material dependence to this behavior.

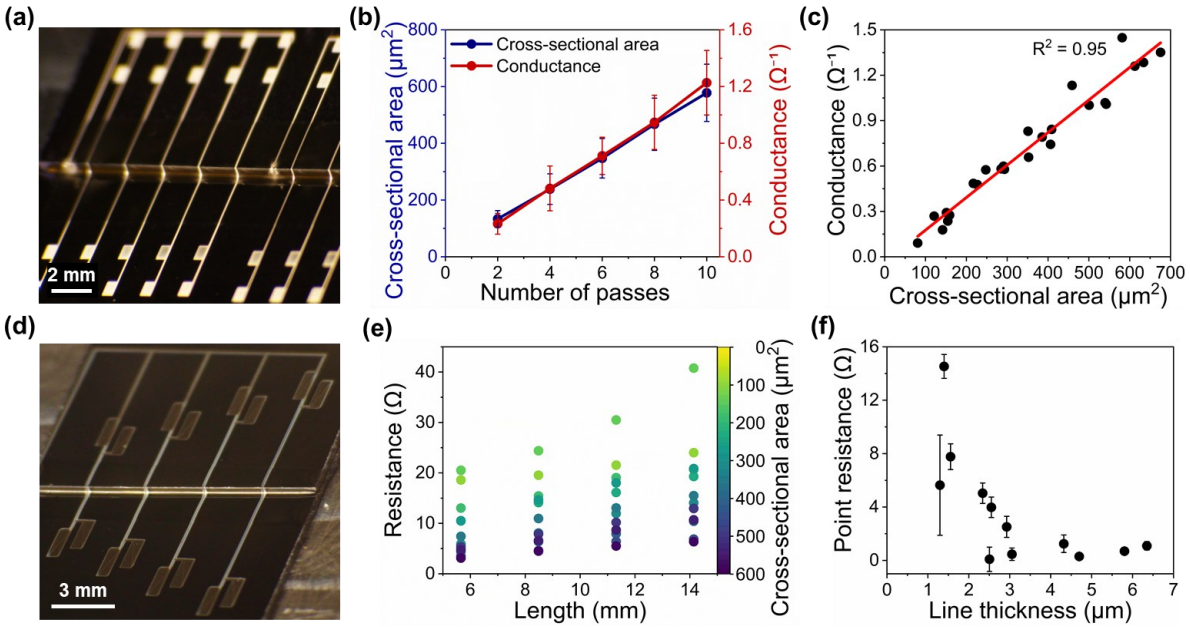

Figure 3. Evaluation of electrical characteristics for conformal interconnects. (a) Optical image of silver interconnects fabricated with 2–10 printing passes to vary the line thickness. (b) Cross-sectional area and conductance as a function of printing passes. (c) Correlation between conductance and cross-sectional area across 25 samples, indicating consistent electrical conductivity. (d) Optical image of length-dependent interconnect test structures. (e) Resistance as a function of total line length, colored based on cross-sectional area. (f) Point resistance associated with the conformal interconnect plotted against average line thickness, showing the resistance contribution arising due to the geometric deviation from a planar trace.

2.4 Thermal Reliability

While fabrication consistency and electrical conductivity are key prerequisites for applications of printed interconnects, thermal reliability often imposes a critical barrier to practical implementation. The BCB dielectric layers presented throughout this work were cured at 250 °C, while the Ag traces were sintered at either 150 or 250 °C depending on the ink used. For a more robust evaluation of thermal stability, four distinct thermal protocols were applied to probe both single-exposure high-temperature compatibility and thermal cycling stability (Figure 4).

The tolerance of electronics to a single exposure to elevated temperature is relevant for process compatibility, for example in solder reflow processes. Here, EI-615 Ag traces initially sintered at 150 °C under an inert atmosphere were exposed sequentially to temperatures from 150 to 350 °C for 10 min in air, with a consistent 5 °C min^{-1} ramp rate for both heating and cooling. Figure 4a shows the conductance normalized to sample cross-sectional area, showing

an improvement in electrical characteristics up to 300 °C without any samples failing, suggesting additional sintering of the silver after the initial post-processing step (Figure S1). Upon heating to 350 °C, many of the samples retain significant, and indeed increased, conductance; however, 7 of the 30 samples exhibit a significant drop in conductance indicative of partial or complete failure. Notably, the failed or severely degraded traces correspond to the 7 samples with the lowest silver cross-sectional area (<75 μm^2) among these samples, suggesting that thinner silver traces are more susceptible to this particular thermal failure mode. These results demonstrate that the conformal BCB-supported interconnects maintain electrical functionality through thermal exposures relevant to high-temperature Ag sintering and other processing steps such as solder reflow, and interconnect thickness is linked to failure under these extreme conditions. This performance substantially exceeds the thermal tolerance observed for fillet-based interconnects, where visible dielectric cracking occurred below or near 250 °C (Figure 1b–c).

While isolated high-temperature stability is important for process compatibility and select applications, repeated thermal cycling is often a more critical stressor in operation. Here, few-cycle thermal exposure to 250 °C was evaluated (Figure 4b). Across 15 samples with varying cross section area, the conductance change remains within 5% throughout the 30-cycle test. Several traces show a slight positive conductance change during the early cycles, consistent with continued thermal consolidation or sintering of the printed Ag microstructure during repeated heating. Traces with larger cross-sectional areas maintain nearly constant conductance throughout cycling, whereas the thinnest traces exhibit the greatest sensitivity to cycling, showing a small negative conductance change after 30 cycles driven by a significant change in a single sample. Consistent with the single-shot temperature exposure, this suggests that thinner traces are more susceptible to this degradation mode. Nevertheless, the overall conductance variation remains limited for most traces, confirming the robust tolerance to challenging thermal conditions supported by the material selection and geometry design.[42]

Extended thermal cycling between room temperature and 150 °C was subsequently performed for 100 cycles (Figure 4c). While wiring connections prevented reliable measurements during cycling (Figure S2), the conductance was measured ex situ before and after cycling using a four-probe setup. Of the 48 samples tested, 44 were successfully measured after cycling, while four were damaged due to sample handling unrelated to thermal stress. All 44 measured samples remained electrically continuous after 100 cycles, with conductance changes ranging from approximately −9% to 14% and a modest positive shift overall (Figure 4c and Figure S3). These results indicate that the conformal interconnects retain electrical

functionality during repeated cycling to 150 °C. An additional thermal cycling test from −55 and 150 °C was conducted to extend this to lower temperature (Figure S4, Figure S5). Of 17 samples evaluated, ten remained electrically continuous following 100 cycles, with final conductance changing approximately −7% and 15%. However, the remaining seven samples failed, typically following at least 50 cycles, potentially due to the absence of encapsulation and humidity control within the thermal cycling chamber, with some of the failures attributed to cracking in the Ag itself rather than the dielectric. While not a wholesale success, this provides a promising foundation and direction for future efforts to further improve thermal reliability.

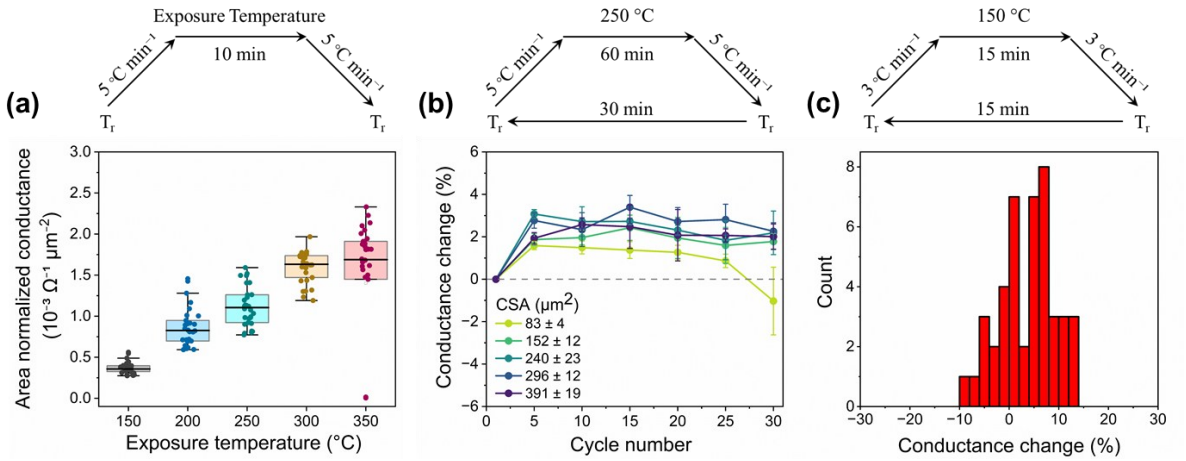

Figure 4. Thermal reliability testing of printed conformal interconnects. (a) Area-normalized conductance following sequential thermal exposure from 150–350 °C, showing a general increase in conductance through 300 °C and isolated sample failures following heating to 350 °C. (b) Conductance change during repeated thermal cycling from room temperature to 250 °C, showing limited variation over 30 cycles for traces with different cross-sectional areas. (c) Histogram of the relative conductance change for 44 samples measured following 100 thermal cycles between room temperature and 150 °C. All samples remained electrically continuous after cycling.

2.5 Extension to Complex Geometries

Alongside the advantages of this architecture for thermal stability, a primary motivation for the conformal interconnect design is its natural scalability to diverse and complex multiplanar geometries with material, process time, and footprint efficiency. This is exemplified in Figure

5, which demonstrates applicability regardless of step height, and the seamless accommodation of the 45° tilted deposition geometry for multiple steps without modification to the process flow.

Interconnects were first demonstrated on a tall step edge with a 2 mm height transition to validate the scalability of the conformal approach to step heights relevant to thick substrates and multi-chip configurations (Figure 5a). Optical imaging confirms continuous trace formation across the step, with consistent morphology on both the upper and lower horizontal surfaces and the tall vertical sidewall. Electrical characterization (Figure 5b) confirms continuity and reveals a strong linear conductance-area relationship ($R^2 = 0.98$), quantitatively comparable to the baseline step-edge samples. Importantly, the material uses and printing time scales linearly with the step height, rather than quadratically as a typical fillet or ramp structure would.

Dense multi-step structures were fabricated to demonstrate the viability of the conformal approach for high-density interconnect arrays relevant to die-to-die routing and multi-chip integration (Figure 5c–f). For the main demonstration, a long silver serpentine was printed across three silicon substrates with a 50 µm center-to-center line pitch using 2, 4, and 6 printing passes (Figure 5c). Each serpentine had an approximate continuous printed length of 125 mm and traversed each of the two step edges 10 times, representing a stringent test for interconnect density and reliability. Optical imaging (Figure 5c) confirms regular, well-defined traces across multiple step transitions, with no evidence of shorting or trace discontinuity in the dense array. Higher resolution SEM imaging (Figure 5d) provides detailed visualization of the printed interconnects at the step transitions, showing regular, high-precision lines with consistent morphology; the magnified inset confirms separated line morphology at the 50 µm pitch scale without obvious merging between adjacent traces, along with some line edge waviness along the vertical wall potentially due to motion system artifacts.

Profilometry of the line height profile for this dense serpentine shows uniform pitch and trace height (Figure 5e), with the sample printed with 4 layers exhibiting a typical peak line thickness of approximately 2.7 µm. For comparison, the corresponding 2-pass and 6-pass arrays show average line thicknesses of approximately 1.2 and 4.4 µm, respectively (Figure S6). Conductance for these samples increases monotonically with trace thickness, as expected, confirming the electrical continuity across 20 step-edge transitions (Figure 5f).

To further support the scalability of the approach, additional multi-step interconnect arrays were fabricated with a relaxed 100 µm center-to-center pitch using the same 2, 4, and 6 pass printing conditions. Each 100 µm-pitch array also had an approximate continuous printed length of 125 mm. Optical images of these structures show continuous and well-separated traces across

the multi-step regions, and SEM images further confirm regular printed morphology without visible line merging (Figure S7). The corresponding height profiles and conductance measurements are provided in the Supporting Information (Figure S8). Together, these results demonstrate that the conformal interconnect architecture with BCB supports both large step heights and chip stacking configurations at high interconnect densities.

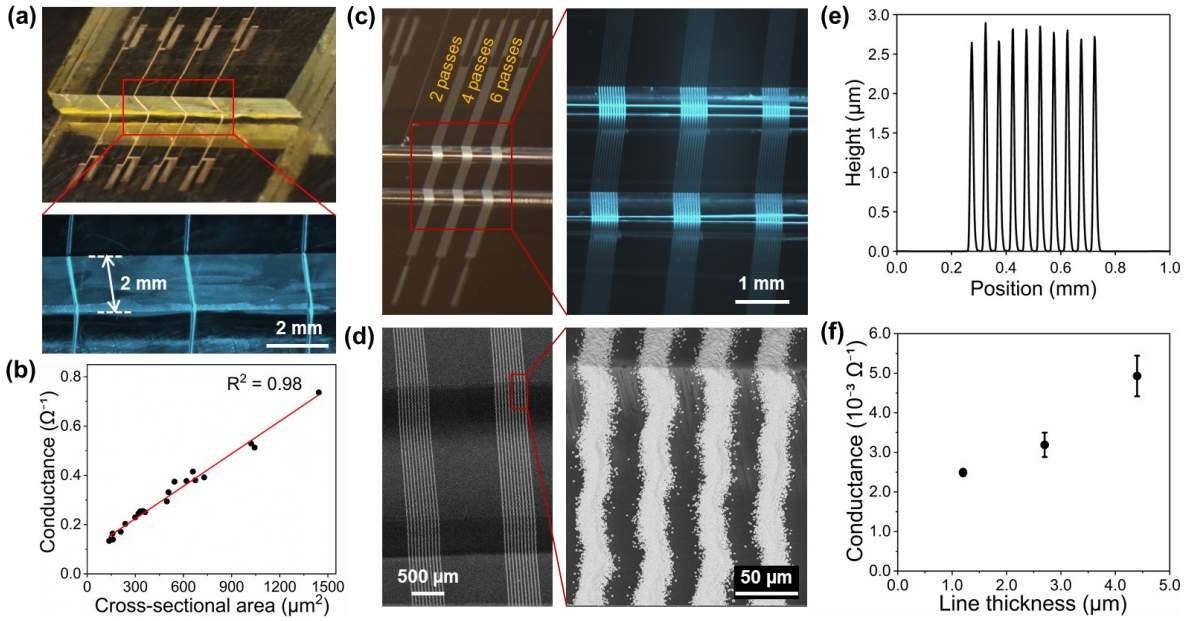

Figure 5. Generalization of printed conformal interconnects to complex geometries. (a) Optical images of silver interconnects printed across a tall 2 mm step edge, demonstrating extension to large out-of-plane transitions without a bulky fillet. (b) Conductance as a function of cross-sectional area for interconnects printed across the 2 mm step edge, confirming electrical continuity across the tall step with a consistent effective conductivity. (c) Optical images of dense multi-step serpentine patterns printed with 2, 4, and 6 passes at a 50 μm center-to-center line pitch. Each array has an approximate continuous printed length of 125 mm and includes 20 total step-edge crossings. (d) SEM images showing isolated and continuous printed lines across the multi-step architecture, with the magnified image highlighting the morphology at the top corner of the step. (e) Representative profilometry height profile of the 4-pass, 50 μm-pitch serpentines. (f) Conductance as a function of printed line thickness for the 50 μm pitch multi-step interconnects.

3. Conclusion

This work demonstrates a conformal architecture for printed interconnects to bridge multiplanar geometries, in this case enabled by a thin, printed benzocyclobutene dielectric layer.

The dielectric forms a naturally rounded lower transition without a bulky ramp or fillet structure. This supports reduced material usage and print time, more effective utilization of device footprint, and improved thermomechanical reliability that lessens constraints on material selection. This is validated for <1 μm thick conductor traces, and demonstrates excellent thermal stability upon heating to 300 °C, few-cycle temperature exposure to 250 °C, and 100 cycle testing between room temperature and 150 °C. This design approach scales efficiently to 2 mm step heights and more complex multiplanar samples, including for high density printed conductors, establishing its versatility for complex hybrid integration geometries. Altogether, this approach presents a viable design option for advanced manufacturing in electronics packaging, overcomes material and thermal constraints of previously demonstrated printed interconnect architectures, and establishes a compelling strategy for additive electronics packaging and hybrid integration.

4. Experimental Section

Materials and Substrate Preparation

A B-staged divinylsiloxane bis-benzocyclobutene (DVS-BCB) resin, Cyclotene™ 3022–46, was acquired from Kayaku Advanced Materials, Inc. For deposition on the stacked substrates, the as-received resin was diluted with xylenes and tetralin in a volume ratio of 4:7:1 (resin/xylenes/tetralin) to achieve a viscosity suitable for ultrasonic atomization, as described in our previous work.[45] Two silver nanoparticle inks were used for experiments due to a supply chain disruption during the project. The first was UTD-Ag40X from UT Dots, Inc., which is a 40% wt. silver nanoparticle dispersion in xylenes; the as-received ink was mixed with xylenes and terpineol in a 2:7:1 v/v ratio (ink:xylenes:terpineol).[51] The second was EI-615 from Electroninks, a silver nanoparticle ink formulated for aerosol jet printing, which was used as received. The stacked substrates were prepared by bonding two silicon or glass substrates using a thin printed layer of BCB as the adhesive material (Figure S9). The step height was controlled by changing the number of stacked silicon or glass substrates, resulting in step heights ranging from 0.5 to 2.0 mm. Prior to BCB coating, all substrates were cleaned with isopropanol and dried under a stream of compressed air. After BCB coating and bonding, the bonded substrates were soft cured on a hot plate at approximately 150 °C for 15 min.

Conformal Printing

All printing experiments were performed using a custom three-axis aerosol printing system equipped with an ultrasonic atomizer and in situ light scattering for process monitoring. A solvent-saturated sheath gas (using a tetralin bubbler) was employed while printing BCB to

regulate droplet evaporation within the printhead and reduce overspray.[45] For conformal printing, the substrate was mounted on a fixture tilted at 45° with respect to the printhead nozzle axis, enabling deposition on both the horizontal substrate surface and the vertical step sidewall in a single print. A 200 μm nozzle (Nordson) was used with a standoff distance of ~2 mm.

The conformal BCB layer was printed onto the bonded substrates (Figure S10). Prior to printing, the substrates were plasma treated to improve wetting. The BCB was printed with an atomizer voltage of 32 V, a carrier gas flow rate of 10 sccm, a focusing ratio of 3, and a print speed of 5 mm s^{-1}. Following deposition, the BCB was cured in a nitrogen atmosphere to a peak temperature of 250 °C with a 5 °C min^{-1} ramp rate and a 60 min dwell.

After curing the dielectric layer, Ag traces were printed across the stacked substrates using the same 45° tilted configuration (Figure S11). For the UTD-Ag40X Ag ink, the carrier gas flow rate and focusing ratio were set to 10 sccm and 5, respectively, with an ultrasonic atomizer voltage of 25 V and a printing speed of 2.5 mm s^{-1}, to achieve an approximate line resolution of 40 μm. For samples printed with the EI-615 Ag ink, an atomizer voltage of 20–22 V, a carrier gas flow rate of 7–8 sccm, and a focusing ratio of 3 were used. For dense serpentine patterns spanning three silicon substrates, a 150 μm nozzle was used with a higher printing speed of 5 mm s^{-1} to achieve an approximate line resolution of 20 μm. The UTD-Ag40X Ag traces were sintered at 250 °C, whereas the EI-615 traces were sintered at 150 °C, both for 60 min under a nitrogen atmosphere.

Thermal Reliability Testing

Single-shot thermal exposures were performed by placing samples on a programmable hot plate under ambient atmosphere. The samples were heated from room temperature to target temperatures of 150–350 °C at a ramp rate of 5 °C min^{-1}, held at the target temperature for 10 min, and then cooled to room temperature at 5 °C min^{-1}. After each temperature exposure, the electrical resistance of each individual sample was measured. A total of 30 samples with cross-sectional area ranging from approximately 25–250 μm^2 were evaluated in the single-shot thermal exposure test.

Thermal cycling to 250 °C was conducted on a programmable hot plate under ambient atmosphere. Each cycle consisted of heating to 250 °C at 5 °C min^{-1}, holding at 250 °C for 60 min, cooling to room temperature at 5 °C min^{-1}, and holding at room temperature for 30 min. Samples were subjected to up to 30 thermal cycles, and electrical resistance was measured after every 5 cycles. A total of 15 interconnect samples with cross-sectional areas ranging from approximately 80 to 400 μm^2 were evaluated.

Extended thermal cycling between room temperature and 150 °C was performed using a CSZ microclimate chamber (Model: MCB-1.2-.33-.33-H/AC). Each cycle consisted of heating from room temperature to 150 °C at 3 °C min^{-1}, holding at 150 °C for 15 min, cooling to room temperature at 3 °C min^{-1}, and holding at room temperature for 15 min. Conductance was measured ex situ before and after cycling using a four-probe setup. Additional thermal cycling tests over a broader temperature range from −55 to 150 °C used the same chamber and included in situ measurements recorded at 5 min intervals. The chamber was initially cooled from 25 to −55 °C at 3 °C min^{-1}. Each cycle then consisted of heating from −55 to 150 °C at 3 °C min^{-1}, holding at 150 °C for 15 min, cooling to −55 °C at 3 °C min^{-1}, and holding at −55 °C for 15 min.

Characterization

Scanning electron microscopy was performed using a FEI Quanta-FEG 250 field-emission SEM instrument. Cross-sectional specimens were prepared by mechanically cleaving to expose the step-edge region. Prior to imaging, the specimens were sputter-coated with a thin Au conductive layer to minimize charging during SEM observation. Optical profilometry (Zygo NewView 9000) was used to measure line height profiles and cross-sectional areas of printed traces. For imaging of conformal interconnects across the step-edge geometry, samples were positioned at a 45° tilt relative to the objective lens to enable visualization of both the horizontal substrate surface and the vertical sidewall. Electrical characterization was performed ex situ using a four-point probe configuration with a source meter (Keithley 2450). In situ resistance measurements during thermal cycling were collected using a four-point probe configuration with a benchtop multimeter (Siglent 3055-SC).

Artificial Intelligence Generated Content

The artificial intelligence tool Claude (Sonnet 4.6) was used to support manuscript preparation. This was used solely to aid the transition from an expanded outline to an initial draft, and only affected text. This has been thoroughly reviewed and revised, and the authors remain fully responsible for accuracy and completeness. The use of Claude did not influence the science done, claims, conclusions, or any quantitative data or visual elements, but supported the identification of relevant prior literature.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Author Contributions

Md Ramjan Ali: Methodology; Investigation (lead); Validation; Visualization; Writing – original draft. **Garrett A. Clasen:** Investigation (support); Writing – review & editing (support). **Louis O. Morgan:** Investigation (support); Writing – review & editing (support). **Ethan B. Secor:** Conceptualization; Software; Supervision; Funding acquisition; Resources; Writing – review & editing (lead).

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References

[1] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. K. Soong, J. C. Zhang, *IEEE J. Select. Areas Commun.* **2014**, *32*, 1065.
[2] B. Bertenyi, *IEEE Wireless Commun.* **2021**, *28*, 4.
[3] N. Asadizanjani, H. Reddy Kottur, H. Dalir, In *Introduction to Microelectronics Advanced Packaging Assurance*, Springer Nature Switzerland, Cham, **2025**, pp. 141–159.
[4] A. S. Obeidat, A. Umar, R. Al-Haidari, W. T. Alshaibani, Z. Dou, F. Alshatnawi, S. Gonya, M. D. Poliks, C. Hoel, L. Boyd, C. Bellows, G. Soto-Valle, J. Iannotti, T. Budka, K. Duffel, J. Case, F. Pavinatto, *Journal of Manufacturing Processes* **2025**, *148*, 408.
[5] P. Martins, N. Pereira, A. C. Lima, A. Garcia, C. Mendes-Filipe, R. Policia, V. Correia, S. Lanceros-Mendez, *Adv Funct Materials* **2023**, *33*, 2213744.
[6] M. R. Pulugurtha, H. Sharma, R. Pucha, M. Kathaperumal, R. Tummala, *J Indian Inst Sci* **2022**, *102*, 461.
[7] E. S. Rosker, M. T. Barako, T. Tran, E. Nguyen, M. S. Goorsky, J. Tice, *IEEE Access* **2022**, *10*, 32973.
[8] K. Skarżyński, M. Słoma, *Adv Elect Materials* **2023**, *9*, 2300238.
[9] Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer, A. C. Arias, *Advanced Materials* **2020**, *32*, 1905279.
[10] B. I. Guyll, L. D. Petersen, C. L. Pint, E. B. Secor, *Adv Funct Materials* **2024**, *34*, 2316426.
[11] J. D. Rurup, E. B. Secor, *Journal of Manufacturing Processes* **2024**, *120*, 1231.

[12] A. S. Dahiya, A. Christou, S. Ma, R. Dahiya, *Adv Materials Technologies* **2025**, *10*, 2401213.
[13] E. B. Secor, *Flex. Print. Electron.* **2018**, *3*, 035002.
[14] N. J. Wilkinson, M. A. A. Smith, R. W. Kay, R. A. Harris, *Int J Adv Manuf Technol* **2019**, *105*, 4599.
[15] P. Karipoth, J. H. Chandler, J. Lee, S. Taccola, J. Macdonald, P. Valdastri, R. A. Harris, *Adv Eng Mater* **2024**, *26*, 2301275.
[16] C. Fisher, L. N. Skolrood, K. Li, P. C. Joshi, T. Aytug, *Adv Materials Technologies* **2023**, *8*, 2300030.
[17] Yuxiao He, C. Oakley, P. Chahal, J. Albrecht, J. Papapolymerou, In *2017 International Workshop on Antenna Technology: Small Antennas, Innovative Structures, and Applications (iWAT)*, IEEE, Athens, Greece, **2017**, pp. 179–182.
[18] E. Kepros, S. K. Ghosh, B. Avireni, P. Chahal, *IEEE Trans. Compon., Packag. Manufact. Technol.* **2025**, *15*, 2235.
[19] M. J. Renn, L. Gamba, *SMTA International* **2025**, *27*, 23.
[20] E. Kepros, B. Avireni, P. Chahal, In *2026 IEEE 76th Electronic Components and Technology Conference (ECTC)*, IEEE, Orlando, FL, USA, **2026**, pp. 2183–2187.
[21] B. Germann, A. Ramm, F. Herrault, J. Hamre, J. Feng, *Journal of Surface Mount Technology* **2023**, *36*, 20.
[22] S. Lotfi, M. Janda, J. Reboun, T. Blecha, *Sci Rep* **2025**, *15*, 39422.
[23] C. Crump, Y. Chu, P. Chahal, *International Symposium on Microelectronics* **2021**, *2021*, 000224.
[24] X. Konstantinou, J. D. Albrecht, P. Chahal, J. Papapolymerou, *IEEE Trans. Compon., Packag. Manufact. Technol.* **2022**, *12*, 682.
[25] A. Sherehiy, M. Sassa, D. Jackson, D. Sills, D. Ratnayake, R. Zhang, Z. Yang, K. Walsh, J. Naber, D. O. Popa, In *Volume 2: Manufacturing Equipment and Automation; Manufacturing Processes; Manufacturing Systems; Nano/Micro/Meso Manufacturing; Quality & Reliability*, American Society of Mechanical Engineers, Knoxville, Tennessee, USA, **2024**, p. V002T08A003.
[26] Y. Wang, H. Liu, L. Huo, H. Li, W. Tian, H. Ji, S. Chen, *Micromachines* **2024**, *15*, 422.
[27] N. Sturim, P. Chahal, M. Hodek, J. D. Albrecht, J. Papapolymerou, In *2026 IEEE Wireless and Microwave Technology Conference (WAMICON)*, IEEE, Clearwater, FL, USA, **2026**, pp. 1–4.
[28] R. Al-Haidari, M. Alhendi, D. Richmond, E. M. Abbara, A. Obeidat, U. S. Somarathna, M. Schadt, M. Poliks, A. V. Gowda, J. Erlbaum, H. Xiong, C. Hitchcock, In *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, IEEE, Orlando, FL, USA, **2023**, pp. 668–675.
[29] R. Al-Haidari, D. Richmond, M. Alhendi, E. M. Abbara, A. Obeidat, F. Alshatnawi, M. Schadt, M. Poliks, A. V. Gowda, J. Erlbaum, H. Xiong, C. Hitchcock, *IEEE Open J. Power Electron.* **2025**, *6*, 1656.
[30] L. Davidson, R. S. Aga, F. Ouchen, T. Pandhi, C. Bartsch, E. Heckman, In *International Workshop on Thin Films for Electronics, Electro-Optics, Energy and Sensors 2022* (Eds.: Subramanyam, G.; Banerjee, P.; Lakhtakia, A.; Sun, N. X.), SPIE, Boston, United States, **2023**, p. 13.
[31] Y. Gu, D. Park, D. Bowen, S. Das, D. R. Hines, *Adv Materials Technologies* **2019**, *4*, 1800312.
[32] Y. Gu, D. R. Hines, V. Yun, M. Antoniak, S. Das, *Adv Materials Technologies* **2017**, *2*, 1700178.
[33] M. T. Craton, X. Konstantinou, J. D. Albrecht, P. Chahal, J. Papapolymerou, *IEEE Trans. Microwave Theory Techn.* **2020**, *68*, 3418.
[34] A. Sherehiy, D. Jackson, M. Sassa, D. Sills, D. Ratnayake, R. Zhang, Z. Yang, K. Walsh, J. Naber, D. O. Popa, *Journal of Micro and Nano Science and Engineering* **2025**, *13*, 011003.

[35] M. T. Craton, X. Konstantinou, J. D. Albrecht, P. Chahal, J. Papapolymerou, *IEEE Trans. Microwave Theory Techn.* **2021**, *69*, 4191.
[36] M. T. Craton, J. D. Albrecht, P. Chahal, J. Papapolymerou, *IEEE Microw. Wireless Compon. Lett.* **2021**, *31*, 697.
[37] C. Areias, Y. Piro, O. Ranasingha, A. Akyurtlu, *Flex. Print. Electron.* **2023**, *8*, 015009.
[38] Y. Piro, C. Areias, A. Luce, M. Michael, P. Biswas, O. Ranasingha, J. F. Reuther, S. Trulli, A. Akyurtlu, *ACS Appl. Mater. Interfaces* **2023**, *15*, 35449.
[39] I. J. Fernandes, A. F. Aroche, A. Schuck, P. Lamberty, C. R. Peter, W. Hasenkamp, T. L. A. C. Rocha, *Sci Rep* **2020**, *10*, 8878.
[40] X. Long, X. Ding, T. Mou, F. Zhang, R. Dong, J. Zhu, Z. Shen, P. M. Iyela, W. Yan, J. Liu, X. Geng, C. Chang, *J. of Materi Eng and Perform* **2025**, *34*, 4564.
[41] S. Jahan, C. Hu, B. Yuan, S. M. Ritchie, R. Panat, *Additive Manufacturing* **2024**, *92*, 104385.
[42] P. E. Garrou, R. H. Heistand, M. G. Dibbs, T. A. Manial, C. E. Mohler, T. M. Stokich, P. H. Townsend, G. M. Adema, M. J. Berry, I. Turlik, *IEEE Trans. Comp., Hybrids, Manufact. Technol.* **1993**, *16*, 46.
[43] S. Costanzo, I. Venneri, G. Massa, A. Borgia, *J Infrared Milli Terahz Waves* **2009**.
[44] Dow Chemical Company, *CYCLOTENE^{TM} 3000 Series Advanced Electronic Resins*.
[45] M. R. Ali, T. Moritz, M. T. Al Qaseer, E. B. Secor, *[In Revision]*.
[46] C. Areias, A. Luce, E. Harper, Y. Zhang, A. Akyurtlu, *IEEE Trans. Microwave Theory Techn.* **2025**, *73*, 7177.
[47] R. R. Tafoya, E. B. Secor, *Flex. Print. Electron.* **2020**, *5*, 035004.
[48] J. D. Rurup, E. B. Secor, *Adv Eng Mater* **2023**, *25*, 2201919.
[49] A. J. Schwartz, J. D. Rurup, E. B. Secor, *Adv Materials Technologies* **2026**, *11*, e01700.
[50] B. I. Guyll, B. L. Sanford, C. L. Pint, E. B. Secor, *Small Science* **2025**, *5*, 2500069.
[51] J. D. Rurup, E. B. Secor, *Adv Eng Mater* **2024**, *26*, 2301348.

Supporting Information

Aerosol Jet Printing of Thermally Reliable Hybrid Interconnects via a Conformal Dielectric

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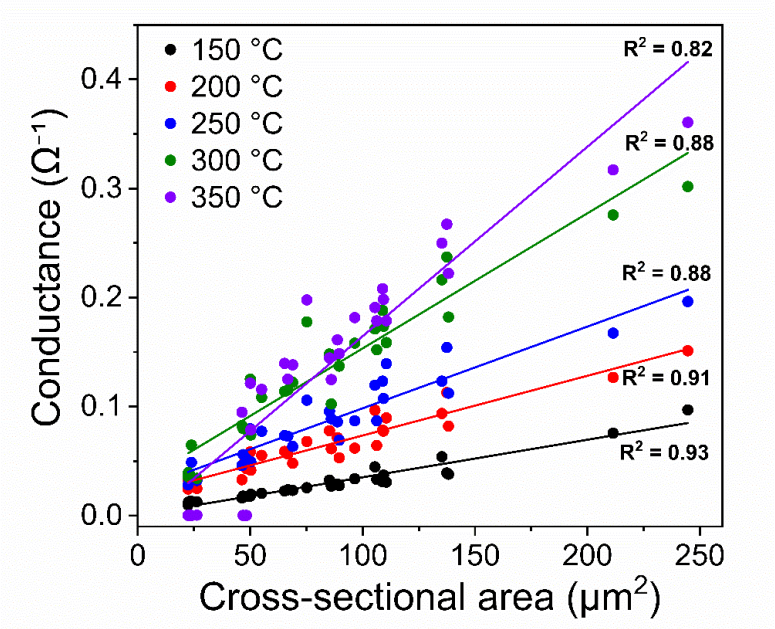

Figure S1. Conductance as a function of cross-sectional area for EI-615 Ag interconnects following sequential thermal exposures from 150 to 350 °C. Solid lines represent linear fits at each exposure temperature, with the corresponding R^2 values shown. The increasing slope indicates improved effective conductivity, consistent with continued sintering of the Ag traces, while greater variability at 350 °C reflects partial degradation of some samples.

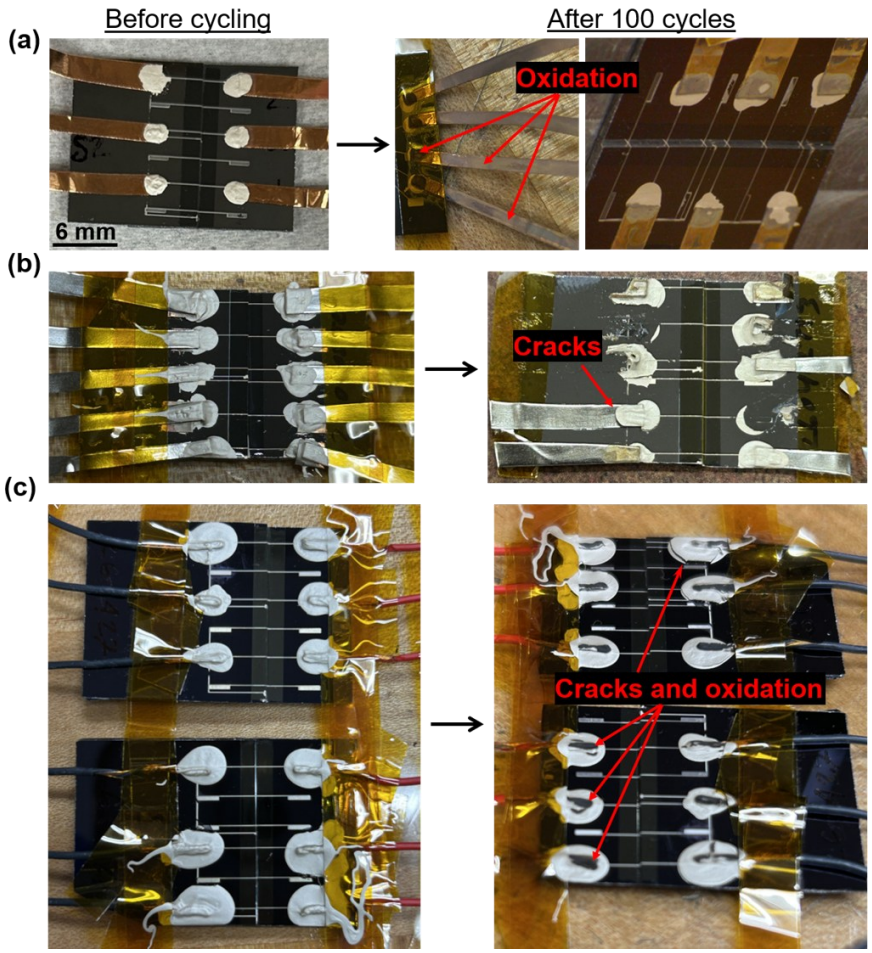

Figure S2. Photographs of the wiring configurations used during thermal cycling from room temperature to 150 °C. Oxidation and cracking at the external wiring and attachment regions prevented reliable continuous measurements during cycling.

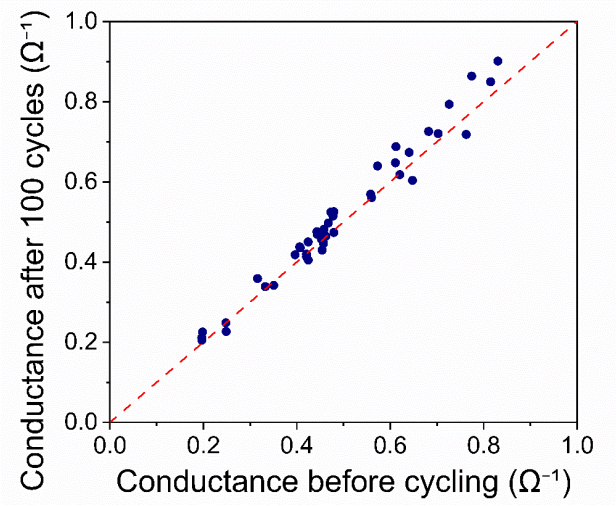

Figure S3. Conductance after 100 thermal cycles between room temperature and 150 °C plotted against the initial conductance for 44 samples. Most values remaining close to or slightly above the equality line, with no clear trend as a function of conductance.

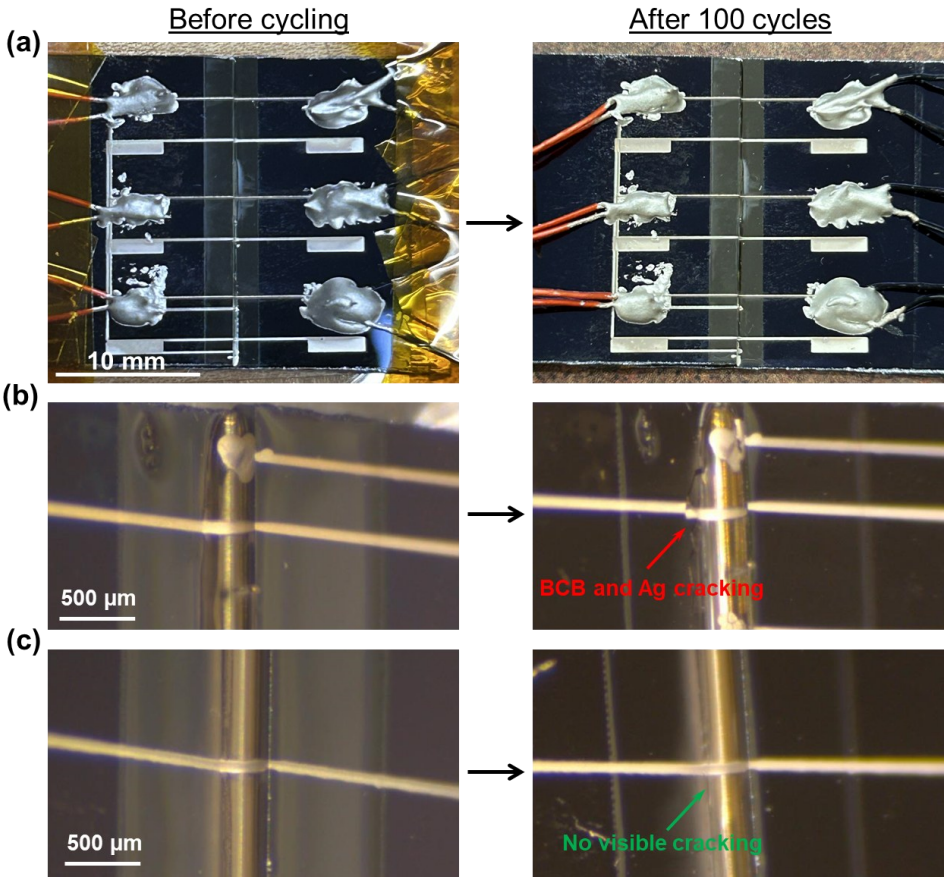

Figure S4. Optical images of the improved wiring configuration and representative step-edge regions before and after 100 thermal cycles between −55 and 150 °C. (a) Overall sample and wiring configuration before (left) and after (right) cycling, respectively. (b, c) Representative samples before and after cycling, showing failed and stable samples, respectively.

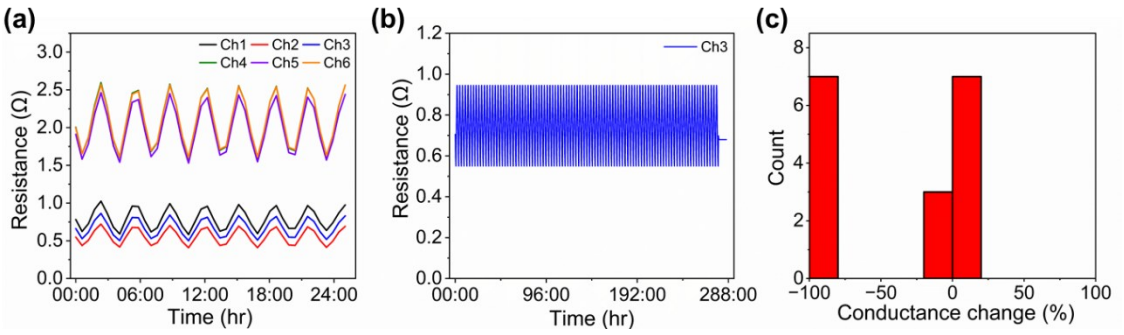

Figure S5. In situ electrical monitoring during 100 thermal cycles between −55 and 150 °C. (a) Resistance of six representative channels during the first 24 h of cycling, showing periodic resistance changes associated with temperature variation. (b) Representative resistance response of Channel 3 over the full approximately 288 h test duration. (c) Distribution of the conductance change for 17 samples following 100 cycles. Ten samples remained electrically continuous, while seven failed samples are represented by a conductance change of −100%.

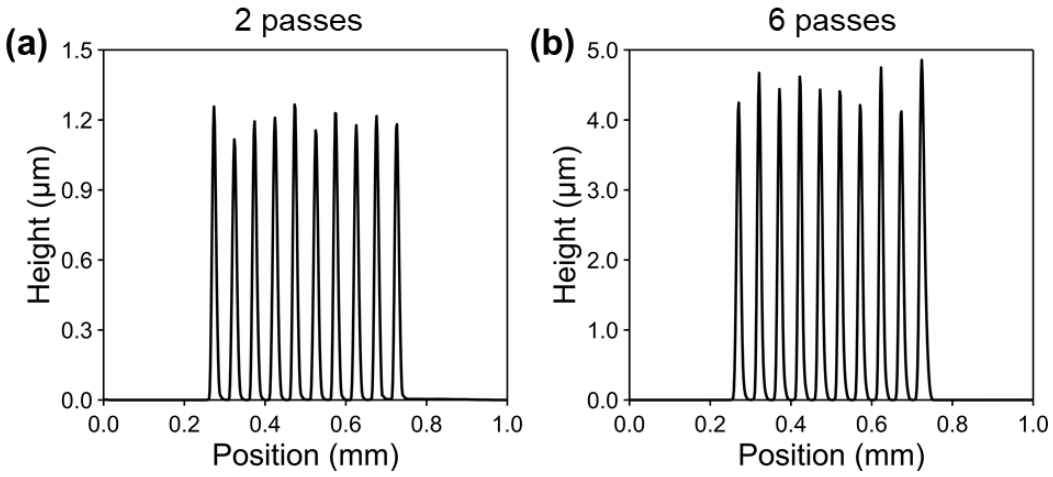

Figure S6. Profilometry height profiles of dense 50 µm pitch silver serpentines printed across the multi-step substrate, for (a) 2-pass and (b) 6-pass patterns.

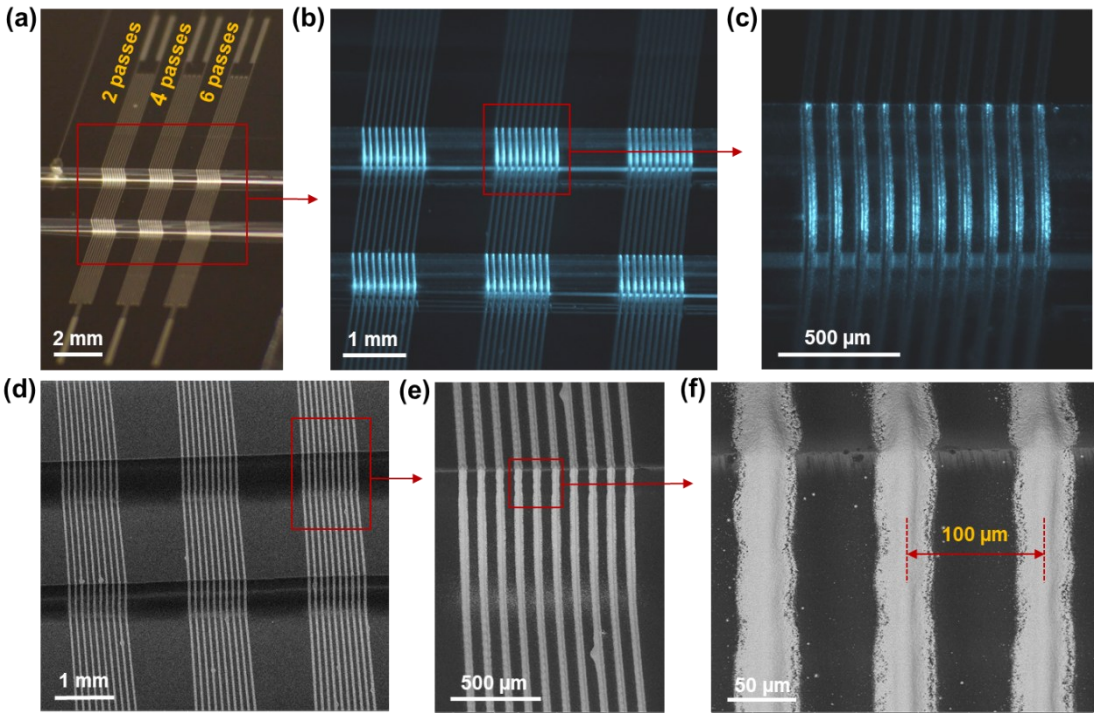

Figure S7. Optical and SEM imaging of 100 µm-pitch silver lines printed across the multi-step architecture. (a, b) Optical images of 2, 4, and 6-pass silver samples. (c) Magnified image of the 4-pass sample at the step transition. (d-f) SEM images showing silver line printed conformally over the multi-step structure; higher magnification images correspond to the 6-pass sample.

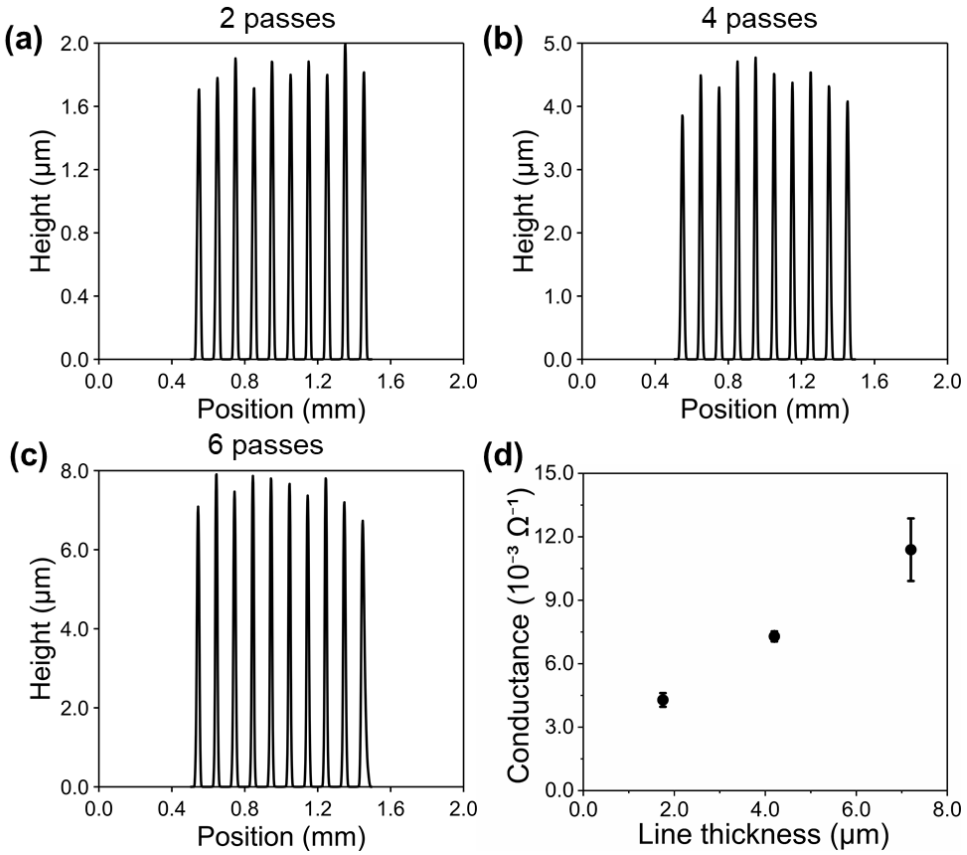

Figure S8. Profilometry and electrical characterization of 100 μm pitch Ag lines printed across the multi-step structure. (a–c) Representative line height profiles of 2, 4, and 6-pass printed serpentines, respectively, showing regularly spaced and consistent peaks. (d) Conductance of the 100 μm-pitch patterns as a function of average line thickness, showing electrical continuity for all samples and well-behaved increase in conductance with increasing printing passes.

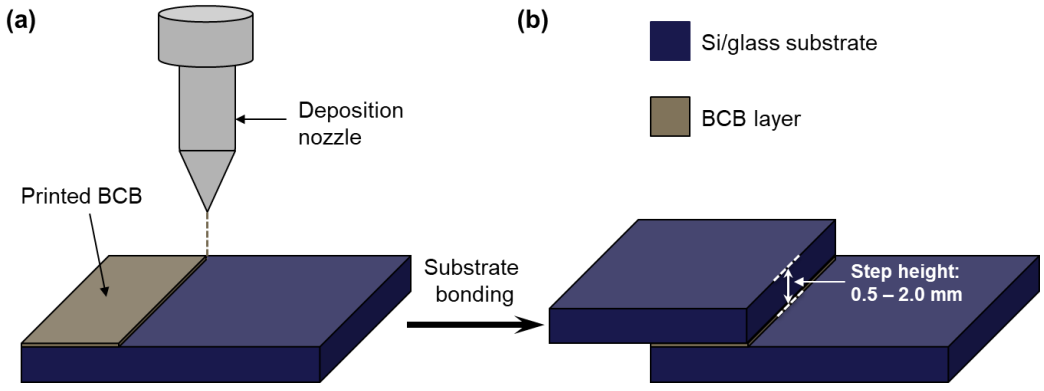

Figure S9. Schematic of step-edge substrate preparation using printed BCB as an adhesive layer. Thin BCB was printed onto silicon or glass substrates and used to bond stacked substrates, forming sharp step-edge structures for conformal interconnect printing. The step height was controlled by varying the number and type of stacked substrates, producing heights from 0.5 to 2.0 mm. After bonding, the substrates were soft cured at ~140 °C for 15 min.

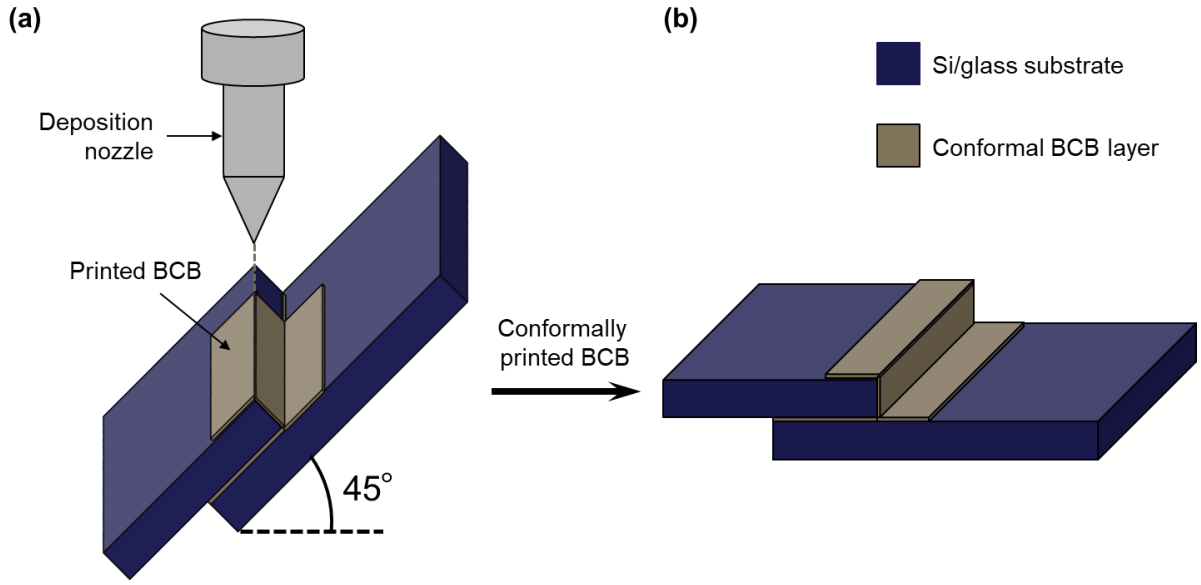

Figure S10. Schematic illustration of conformal BCB deposition on step-edge substrates by AJP. A thin BCB layer was printed across the BCB-bonded step-edge structure to form a conformal dielectric coating over the horizontal surfaces and vertical sidewall.

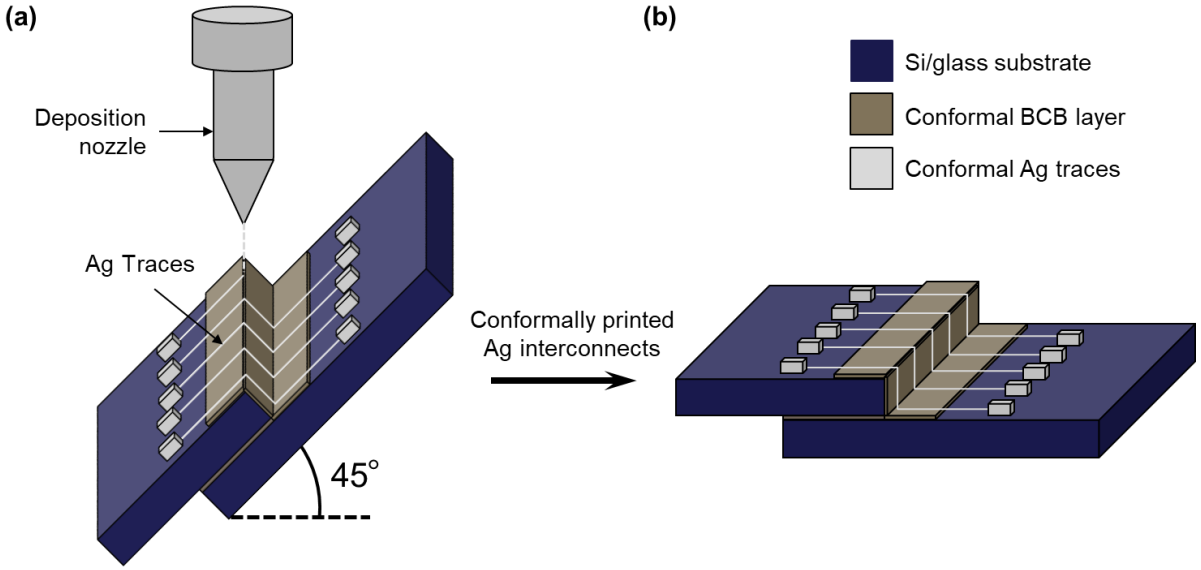

Figure S11. Schematic illustration of conformal Ag interconnect printing across BCB-coated step-edge substrates. After curing the conformal BCB dielectric layer, Ag traces were printed across the step-edge structures to form continuous electrical interconnects over the horizontal surfaces and vertical sidewalls.