Bitstream Photon Counting Chirped AM Lidar with Digital I/Q Demodulation

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Abstract

This paper is a follow-up to two previous papers, one introducing the new bitstream Photon Counting Chirped Amplitude Modulation (AM) Lidar (PC-CAML) with the unipolar Digital Logic Local Oscillator (DLLO) concept, and the other paper introducing the improvement thereof using the bipolar DLLO. In that previous work, there was only a single channel of digital mixing of the DLLO with the received photon counting signal. This paper introduces a new bitstream PC-CAML receiver architecture with an in-phase (I) digital mixing channel and a quadrature phase (Q) digital mixing channel for digital I/Q demodulation with the bipolar DLLO to improve the signal-to-noise ratio (SNR) by 3 dB compared to that for the single digital mixing channel with the bipolar DLLO and by 5.5 dB compared to that for the single digital mixing channel with the unipolar DLLO. (patent pending)

The bipolar DLLO with digital I/Q demodulation architecture discussed in this paper retains the key advantages of the previous bitstream PC-CAML with a DLLO systems since it also replaces bulky, power-hungry, and expensive wideband RF analog electronics with digital components that can be implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) read-out integrated circuits (ROICs) to make the bitstream PC-CAML with a DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

This paper introduces the bipolar DLLO with digital I/Q demodulation receiver architecture for bitstream PC-CAML and presents the initial signal-to-noise ratio (SNR) theory with comparisons to Monte Carlo simulation results.

1. Bipolar DLLO for Bitstream PC-CAML Concept

The patented photon counting chirped amplitude modulation lidar (PC-CAML) concept has been extensively discussed previously. [ref 1-14] In previous PC-CAML systems, the local oscillator (LO) has been a radio-frequency (RF) analog signal applied using expensive, bulky, and power hungry RF analog electronics either in post-detection mixing or via opto-electronic mixing (OEM) at the photon counting detector, including gating of the detector, or applied via pre-detection mixing using an optical intensity modulator. The reader is referred to references 1-14 for more details on the theory and practice for the traditional PC-CAML system.

This paper is a follow-up to two previous papers, one introducing the new bitstream Photon Counting Chirped Amplitude Modulation (AM) Lidar (PC-CAML) with the unipolar Digital Logic Local Oscillator (DLLO) concept [ref 15], and the other paper introducing the improvement thereof using the bipolar DLLO [ref 16]. In that previous work, there was only a single channel of digital mixing of the DLLO with the received photon counting signal. This paper introduces a new bitstream PC-CAML receiver architecture with an in-phase (I) digital mixing channel and a quadrature phase (Q) digital mixing channel for digital I/Q demodulation with the bipolar DLLO to improve the signal-to-noise ratio (SNR) by 3 dB compared to that for

the single digital mixing channel with the bipolar DLLO and by 5.5 dB compared to that for the single digital mixing channel with the unipolar DLLO. (patent pending) [ref 17] The reader is encouraged to read the previous papers [ref 15 and 16] prior to proceeding to read this paper.

The bipolar DLLO with digital I/Q demodulation architecture discussed in this paper retains the key advantages of the previous bitstream PC-CAML with a DLLO systems stated in the previous papers [ref 15 and 16] since it also replaces bulky, power-hungry, and expensive wideband RF analog electronics with digital components that can be implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) read-out integrated circuits (ROICs) to make the bitstream PC-CAML with a DLLO more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

This paper introduces the bipolar DLLO with digital I/Q demodulation receiver architecture for bitstream PC-CAML and presents the initial signal-to-noise ratio (SNR) theory with comparisons to Monte Carlo simulation results.

The single channel of digital mixing between the signal and DLLO described in the previous papers [ref 15 and 16] results in an electrical power SNR that is 3 dB lower than is achievable using digital in-phase and quadrature-phase (I/Q) demodulation since for the single mixer configuration “the thermal noise from the image sideband will always be present, so the noise floor will be 3 dB higher than could be achieved using I/Q mixers.” [ref 18]

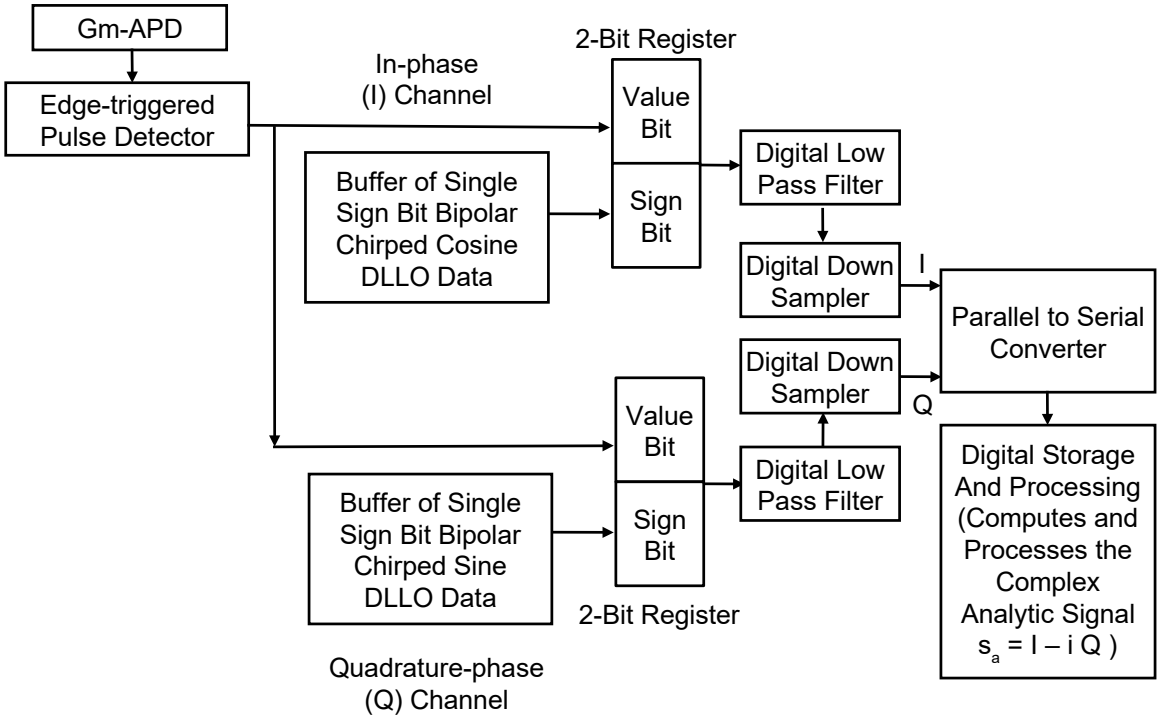
Figure 1 shows (a.) a block diagram for the bitstream PC-CAML with a bipolar DLLO and digital I/Q demodulation, and (b.) a block diagram of an example edge-triggered pulse detector circuit along with its signal timing diagram.

In figure 1 (a.) the constant amplitude, single-bit binary output count of the Geiger-mode Avalanche Photodiode Detector (Gm-APD) (also known as a single-photon avalanche diode (SPAD)) photon counting detector is input to an edge-triggered pulse detector which outputs a shorter binary digital logic level pulse to the value bit of two 2-bit registers for each of which one bit is the value bit and for each of which the other bit is the sign bit.

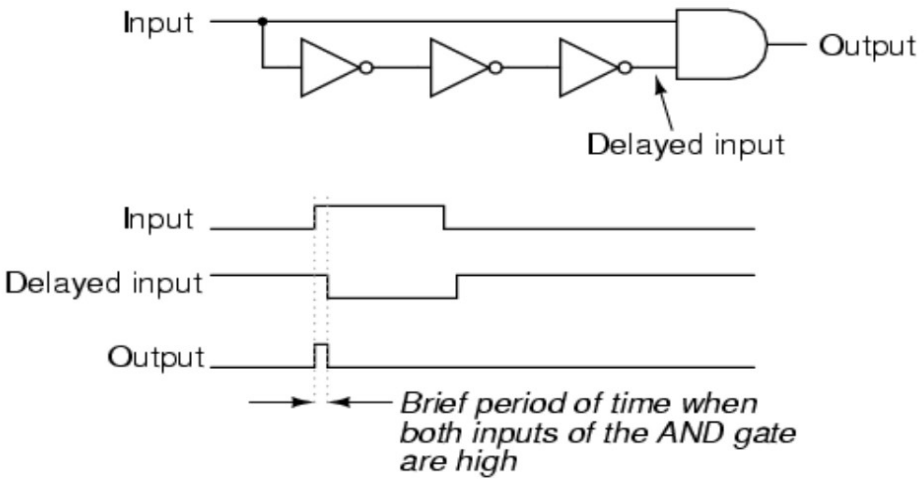
The sign bit of the first 2-bit register, which is the in-phase (I) channel register, is connected to the binary sign data stream of a bipolar chirped cosine DLLO signal, which can be generated and stored in a data buffer prior to operation of the lidar. The sign bit of the second 2-bit register, which is the quadrature-phase (Q) channel register, is connected to the binary sign data stream of a bipolar chirped sine DLLO signal, which can be generated and stored in a data buffer prior to operation of the lidar. The DLLO data buffers may be circular buffers to enable continuous repetition of the DLLO waveform.

The signed digital data output from each 2-bit register are then sent to a corresponding digital low pass filter, the output of which is sent to a corresponding digital down sampler. The in-phase (I) and the quadrature-phase (Q) signals from the digital down samplers are input to a parallel to serial converter which outputs the I and Q signals digital data on a single serial line to the inputs of the digital data storage and processing subsystem. The digital signal processor (DSP) in this subsystem combines the real-valued I and Q data into the complex analytic signal data, $s_a = I – iQ$, where $i=(-1)^{½}$, and computes the power spectrum of s_a given by $S_a = |\text{cfft}(s_a)|^2$, where

cfft(argument) is the complex fast Fourier transform (FFT) of the argument, and |expression| is the magnitude of the enclosed expression. The DSP finds peaks in the power spectrum S_a, which represent target returns. The frequency of a peak in S_a is proportional to a target range just as in the standard data processing for the standard PC-CAML.



(a.)



(b.)

Figure 1. (a.) Bitstream PC-CAML receiver architecture with a bipolar DLLO and digital I/Q demodulation block diagram and (b.) Example edge-triggered pulse detector circuit from the online textbook Lessons in Electric Circuits, at https://www.allaboutcircuits.com/textbook/digital/chpt-10/edge-triggered-latches-flip-flops/ , by Tony R. Kuphaldt and Dennis Crunkilton, License: https://www.gnu.org/licenses/dsl.html .

Note that although the description of the bipolar DLLO and unipolar signal count digital mixing is given above in terms of a sign bit and a value bit for simplicity and clarity, the 2-bit signed data can also use other representations of signed binary numbers, such as one's or two's complement representations, with the digital processing procedures appropriate to those representations.

An example circuit for the edge-triggered pulse detector is shown in figure 1 (b.). The edge-triggered pulse detector allows the single-bit signal pulses to be much shorter than the count pulses output by the Gm-APD, which can be longer than desired due to the Gm-APD dead-time. The edge-triggered pulse detector's output pulse can be as short as a single clock pulse as long as the rising edge of the Gm-APD's count pulse is shorter than a clock pulse, and the delay on the delayed input in the edge-triggered pulse detector circuit is shorter than a clock pulse. Other types of edge-triggered pulse circuits may be used, or the edge-triggered pulse circuit can be eliminated if the Gm-APD output count pulses are short enough.

1.1 Key Advantages of the Bipolar DLLO with Digital I/Q Demodulation in Bitstream PC-CAML

The key advantages of the bipolar DLLO with digital I/Q demodulation in the bitstream PC-CAML are as follows:

1. The bipolar DLLO with digital I/Q demodulation can be implemented in the unit cells of a photon counting receiver's readout integrated circuit (ROIC) by adding two digital mixing channels, each with a buffer for the DLLO's binary digital sign data, a 2-bit register for signed binary data, a digital low pass filter, and a digital down sampler.
2. The signal count, and the in-phase and quadrature-phase DLLO sign data each consist of just a stream of single-bit binary data.
3. The bipolar DLLO with digital I/Q demodulation eliminates the need for bulky, power-hungry, and expensive wideband RF analog electronics by replacing them with digital electronics. Multi-GHz clocks and digital circuits are readily implemented in inexpensive silicon complementary metal-oxide-semiconductor (CMOS) ROICs.
4. The in-phase and quadrature-phase bipolar DLLO single-bit binary sign data can be computed prior to operation and stored in buffers in each ROIC unit cell, or in a single buffer for each of the in-phase and quadrature-phase bipolar DLLOs in the receiver and distributed to each ROIC unit cell in real-time during operation. The buffers may be circular buffers for continuous repetition of the in-phase and quadrature-phase bipolar DLLO waveforms.
5. The bipolar DLLO with digital I/Q demodulation improves the electrical power SNR of the bitstream PC-CAML by about 5.5 dB (2.5 dB from using the bipolar DLLO instead of the unipolar DLLO plus 3 dB from using digital I/Q demodulation) compared to that of the original bitstream PC-CAML using the unipolar DLLO with a single channel of digital mixing.

These advantages make the bitstream PC-CAML with a bipolar DLLO and digital I/Q demodulation more suitable for compact lidar-on-a-chip systems and lidar array receivers than previous PC-CAML systems.

2. Bitstream PC-CAML with a Bipolar DLLO and Digital I/Q Demodulation SNR Theory

The purpose of this paper is to introduce the new bipolar DLLO with digital I/Q demodulation for the bitstream PC-CAML technique and to show through simulation results how it works. The purpose of this paper is not to develop a comprehensive theory of operation for the new technique, so the initial SNR theory presented herein has a limited range of applicability to the new technique, and an improved theory needs to be developed in future work.

The initial electrical power signal-to-noise ratio (SNR) theory used herein for the bitstream PC-CAML with the Bipolar DLLO and digital I/Q demodulation technique is derived from the SNR theory for photon counting Gm-APDs developed by Gatt, Johnson, and Nichols. [ref 19, pp. 3268-3269] and its modification for bitstream PC-CAML with the bipolar DLLO and a single channel of digital mixing as described in reference 16. The theory developed by Gatt, et. al., is for detection of unmodulated pulsed lidar returns. This theory, however, can be applied to the single-bit chirped AM waveform and bipolar DLLO with digital I/Q demodulation as simulated in Mathcad®[1] by making the following adjustments:

1. Reducing the SNR by a factor of 4 to account for losses due to the one-sided (aka unipolar) signal and the two-sided (aka bipolar) DLLO waveforms of the bitstream PC-CAML, but with the 3 dB improvement due to the digital I/Q demodulation, as discussed in the papers on the original PC-CAML concept by Redman, Ruff, and Giza [ref 2-4].
2. Adding quantization noise due to the 2-bit quantization (single value bit and single sign bit) with a bipolar intermediate frequency (IF) signal.
3. Setting the arm probability, PA, in the SNR equations of Gatt, et. al., [ref 19, pp. 3268-3269] to 1 since in the theory as used herein, the counts per matched filter impulse response time are output counts after having been subjected to the arm probability.
4. Multiplying the theoretical SNR by $10^{-0.176}$ to account for the scalloping loss due to the Hann window applied to the data in the simulations (see section 3) to reduce sidelobes.

Equation (41) from Gatt, et. al., [ref 19, p. 3269] modified as described above becomes

$$SNR_{theory} = \frac{10^{-0.176} N_s \left[1 - \left(\frac{M}{M + m_{scounts}}\right)^M\right]^2}{4\left[1 - e^{-\left(m_{ncounts} + m_{qncounts}\right)}\left(\frac{M}{M + m_{scounts}}\right)^M\right]\left[1 - \left[1 - e^{-\left(m_{ncounts} + m_{qncounts}\right)} \cdot \left(\frac{M}{M + m_{scounts}}\right)^M\right]\right]} \quad (1.)$$

where N_s = Number of clock time interval samples accumulated over the chirp duration
M = speckle diversity
$m_{scounts}$ = average number of signal counts output by the Gm-APD per clock time interval
$m_{ncounts}$ = average number of noise counts output by the Gm-APD per clock time interval (includes all of the additive noise sources except for quantization noise)
$m_{qncounts}$ = the average number of quantization noise counts per clock time interval.

Note that the clock time interval equals the matched filter impulse response time and the dead-time in this theory and in the simulations discussed in section 3.

1 Mathcad® is a registered trademark of PTC Inc. or its subsidiaries in the U.S. and in other countries.

This SNR theory does not include the effects of energy loss from the fundamental IF frequency to higher order odd harmonics and their mixing products for the chirped square wave modulation waveforms in the bitstream PC-CAML. This SNR theory also assumes 100% modulation depth for the PC-CAML signal.

2.1 Sinusoidal Modulation Depth Loss Near Saturation

As the average number of signal counts output by the Gm-APD per available clock time interval increases towards 1, the apparent modulation depth of a sinusoidal chirped AM waveform decreases due to the Gm-APD being able to output at most only a single count per dead-time which is set equal to the clock time interval in the simulations (see section 3). For the sinusoidal signal, when the average count rate is so high that a count is output for every clock time interval, the single-bit count data stream looks like that of a constant, unmodulated signal corresponding to a modulation depth of zero and therefore, the SNR goes to zero.

For the sake of brevity, this description discusses only a chirped sinusoidal signal whereas reference 15 discussed both the chirped sinusoidal signal and the chirped square wave signal. However, the bipolar DLLO with digital I/Q demodulation can also be used just as easily with a chirped square wave signal as it was for the unipolar DLLO and single channel of digital mixing discussed in reference 15.

2.2 Quantization Noise with the Bipolar DLLO

Noise due to quantization must be calculated to use in the SNR theory of equation (1.). The quantization noise is computed from the Signal-to-Quantization-Noise Ratio in dB ($SQNR_{dB}$) given by equation 2.38 of Bjorndal [ref. 20, p. 40]:

$$SQNR_{dB} = 6.02*N_{bits} + 1.76, \text{ where } N_{bits} = \text{the number of bits of digitization.} \quad (2.)$$

The number of bits input to equation (2.) for the bipolar DLLO concept is determined as follows.

For the Bipolar DLLO multiplied by the Unipolar Signal, there are 3 states (+1, 0, -1) since +0 and -0 are equivalent, degenerate states equal to 0. Therefore, the equivalent number of bits is derived from

$$2^{N_{bits}} = 3 \Longrightarrow N_{bits}\cdot\ln(2) = \ln(3) \Longrightarrow N_{bits} = \ln(3)/\ln(2) = 1.5849625 \quad (3.)$$

Therefore, $SQNR\_dB(N_{bits}=1.5849625) = 6.02*1.5849625 + 1.76 = 11.301474$ dB, and $SQNR = 10^{1.1301474} = 13.4942$.

Thus, the quantization noise per count is 1/13.4942 for $N_{bits}=1.5849625$ corresponding to 3 states.

The above calculation applies to the N_{bits} quantization noise for the IF data using the unipolar DLLO with the AND logic gate digital mixer. However, Klein states and shows that "…the logic function XOR results in the negative multiplication of two bipolar bit-streams, and the logic function AND results in the multiplication of two unipolar bit-streams...For the logic operation XOR, the standard deviation is doubled in comparison to the operations OR and AND...Due to

the fact that the output bit stream changes from zero to one with XOR and only from 0.5 to zero or one with OR and AND, the scaling is expected to be a factor of two of the standard deviations from OR and AND to XOR." [ref 21]

Since for the electrical power SNR, the noise is given by the variance rather than the standard deviation, the quantization noise for the bipolar DLLO is 4 times higher than that for the unipolar DLLO with the same number of quantization bits. Therefore, for the bipolar DLLO, the average number of quantization noise counts per clock time interval is given by:

$$m_{q\_n\_counts\_avg} = 4 \cdot m_{spn\_counts\_avg}/13.4942 = m_{spn\_counts\_avg}/3.37355 \quad (4.)$$

where $m_{q\_n\_counts\_avg}$ = the average number of quantization noise counts per clock time interval in the simulations

$m_{spn\_counts\_avg}$ = the average number of signal plus noise counts per clock time interval in the simulations.

Therefore, the average number of quantization noise counts per clock time interval for the bipolar DLLO is 1.78 times higher than that of the unipolar DLLO, which is given by $m_{spn\_counts\_avg}/6$. [ref 15]

In the initial SNR theory, equation (1.), $m_{qncounts}$ is set equal to the value of $m_{q\_n\_counts\_avg}$ from equation (4.) for comparison to the simulation results.

Development of an SNR theory that includes the effects of quantization noise, aliasing, the harmonics and their mixing products, less than 100% signal modulation depth, and Gm-APD saturation for the bitstream PC-CAML that is applicable for both chirped sinusoidal and chirped square wave signals is beyond the scope of this paper and is suggested for future work.

3. Monte Carlo Simulation Results Compared to Initial SNR Theory

The equations and functions for implementing the Monte Carlo simulations of signal and noise for bitstream PC-CAML with the unipolar and bipolar DLLOs with a single digital mixing channel in Mathcad® were given in the previous papers. [ref 15 and16]

The only changes for the bipolar DLLO with digital I/Q demodulation simulations are as follows:

1. Using the sign of a bipolar chirped cosine (in-phase (I)) square wave DLLO (equation (5 a.)) and the sign of a bipolar chirped sine (quadrature-phase (Q)) square wave DLLO (equation (5 b.)) instead of the sign of the single bipolar chirped square wave DLLO used in reference 16
2. Forming the complex analytic signal from the outputs of the I and Q digital mixers, and computing the power spectra of this complex analytic signal plus noise for 24 trials in the Monte Carlo simulations.

The equations for the sign of the I and Q bipolar chirped square wave DLLOs are given by

$$LO\_I := \overrightarrow{sign\left[\cos\left[2\pi\cdot\left(f_0 + k_f\cdot t\right)\cdot t\right]\right]} \qquad (5\text{ a.})$$

$$LO\_Q := \overrightarrow{sign\left[\sin\left[2\pi\cdot\left(f_0 + k_f\cdot t\right)\cdot t\right]\right]} \qquad (5\text{ b.})$$

where f_0 = the start frequency of the chirp
k_f = the temporal slope of the chirp = $(f_s - f_0)/T_{chirp}$, where f_s = the stop frequency of the chirp, and T_{chirp} = the duration of the chirp
t = the clock time from the start of the chirp
sign[] = the sign of the argument.

In the simulations, the LOs' signs are applied to the signal's value by multiplying separately the results of equations (5 a.) and (5 b.) by the signal value for each clock time interval to form the digitally mixed I and Q intermediate frequency (IF) signals. The I and Q IF signals are combined as follows to form the complex analytic signal:

$$IQ\_cplx = Mixed\_I - i\ Mixed\_Q \qquad (6.)$$

where Mixed_I = the product of LO_I and the signal plus noise counts
Mixed_Q = the product of the LO_Q and the signal plus noise counts
$i = (-1)^{1/2}$

The complex analytic signal is Hann windowed to reduce sidelobes in the IF power spectrum. The Hann windowed complex analytic signal is zero padded to eight times the original length.

The power spectrum of the Hann windowed and zero padded complex analytic signal is computed in Mathcad® for each trial. The resulting power spectra are averaged together to produce the mean power spectrum for all the trials.

The mean noise floor of this mean power spectrum is computed over the portion of the spectrum between the target signal's fundamental IF and the third harmonic of that frequency. The value of this mean noise floor is the denominator in computing a simulation's mean SNR.

The peak value of the mean power spectrum at the fundamental IF minus the value of the mean noise floor is used as the numerator in computing a simulation's mean SNR.

Note that since the simulated data are quantized, the quantization noise is inherently included in the simulated power spectra.

The Monte Carlo simulations generate 24 realizations of signal plus noise for an up-chirp AM signal waveform. The simulations were run for the following parameter values:

N_{trials} = Number of simulation trials = 24	N_s = Number of clock time intervals = 2^{13}
Δt = Clock time interval = 0.5 ns	t_{chirp} = chirp duration = 4.096 μs
f_0 = 100 MHz = chirp start frequency	f_s = 500 MHz = chirp stop frequency
Target Range = 2.99963379 m	Target IF = 1.953125 MHz

M = speckle diversity = 1 or 1E+06
$m_{n\_counts\_avg}$ = average number of additive noise counts per clock time interval = 1E-04
$m_{s\_counts\_avg}$ = average number of signal counts per clock time interval = from 0.05 to 1

Note that the value of the target range used in the simulations is chosen so that the resulting round-trip delay time makes the intermediate frequency (IF) for the target return signal exactly equal to some frequency sample in the power spectrum computed in the simulations to avoid complications in computing the SNR for comparison to the theory due to the target range peak straddling two frequency samples.

Figure 2 shows plots of the mean electrical power SNR vs. mean signal counts per clock time interval ($m_{s\_counts\_avg}$) from the simulations and the SNR theory for a chirped sinusoidal signal and a bipolar chirped square wave DLLO with digital I/Q demodulation as a function of $m_{s\_counts\_avg}$ for M=1 and M=1E+06, with $m_{n\_counts\_avg}$=1E-04.

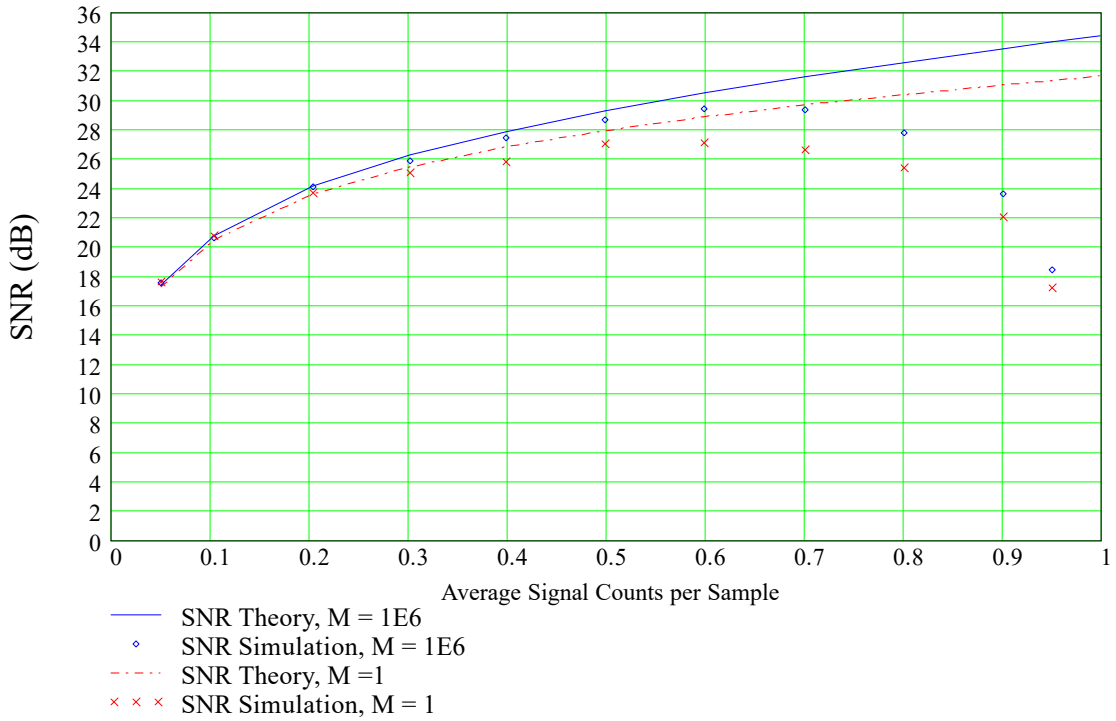


Figure 2. Comparison of SNR results for the Monte Carlo simulations for a chirped sinusoidal signal and a bipolar chirped square wave DLLO with digital I/Q demodulation, and the SNR theory as a function of average signal counts per clock time interval, $m_{s\_counts\_avg}$, with the average number of noise counts per clock time interval, $m_{n\_counts\_avg}$, set equal to 1E-04.

The simulation results and the SNR theory are in good agreement up to an average signal counts per clock time interval, $m_{s\_counts\_avg}$, of about 0.5. As discussed in section 2.1, above this level the saturation effects of power loss to the harmonics and their mixing products, and of modulation depth loss make the simulation's SNR results rollover with increasing $m_{s\_counts\_avg}$. The SNR theory over estimates the SNR for these high signal levels since it does not account for the effects of power loss to the harmonics and their mixing products, and of modulation depth loss.

As explained in section 2.1, the roll-off in SNR at high signal levels is due to the clock time interval samples all being filled with 1's as $m_{s\_counts\_avg}$ approaches 1 for the chirped sinusoidal signal. This looks like a loss in modulation depth for the sinusoidal signal until at $m_{s\_counts\_avg} = 1$, the modulation depth goes to 0 and the signal looks like a constant level signal with no modulation.

Note that a well designed PC-CAML system using transmitter power and/or receiver throughput control to prevent saturation would operate at the lower signal levels where the initial SNR theory agrees with the simulation results. For these lower signal levels, these SNR results for the bipolar DLLO with digital I/Q demodulation are also about 5.5 dB higher than those for the unipolar DLLO with a single channel of digital mixing shown in reference 15. These SNR results for the bipolar DLLO with digital I/Q demodulation are also about 3 dB higher than those for the bipolar DLLO with a single channel of digital mixing shown in reference 16.

4. Conclusion

The concept and initial performance modeling and simulation results for the new bipolar DLLO with digital I/Q demodulation technique for the bitstream PC-CAML were presented in this paper. The results of the initial SNR theory and Monte Carlo simulations presented herein indicate that the bipolar DLLO with digital I/Q demodulation technique for the bitstream PC-CAML improves the electrical power SNR by about 5.5 dB compared to that of the unipolar DLLO with a single channel of digital mixing [ref 15], and by about 3 dB compared to that of the bipolar DLLO with a single channel of digital mixing [ref 16].

The key advantages of the bitstream PC-CAML with a bipolar DLLO and digital I/Q demodulation are that it can be implemented in the unit cells of a photon counting lidar receiver's ROIC by adding simple digital circuits, and the received signal and LO each consist of just streams of single-bit binary data, eliminating the need for bulky, power-hungry, and expensive wideband RF analog electronics. The in-phase (I) and quadrature-phase (Q) bipolar DLLOs' single sign bit binary waveform data can be computed prior to operation and stored in a pair of buffers in each ROIC unit cell, or in a single pair of buffers and distributed to each ROIC unit cell in real-time during operation. A DLLO data buffer can be a circular buffer for continuous repetition of the bipolar DLLO single sign bit binary waveform data. Multi-GHz clocks and digital circuits are readily implemented in inexpensive silicon CMOS ROICs, and Multi-tens-of-GHz can be attained with more expensive technologies. The bipolar DLLO with digital I/Q demodulation technique improves the electrical power SNR by about 5.5 dB compared to that of the unipolar DLLO with a single channel of digital mixing, and by about 3 dB compared to that of the bipolar DLLO with a single channel of digital mixing. These advantages make the bitstream PC-CAML with a bipolar DLLO and digital I/Q demodulation more suitable for compact lidar-on-a-chip systems and for lidar array receivers than previous PC-CAML systems.

5. Suggestions for Future Work

Suggestions for future work include:

1. Develop an SNR theory to include the effects of energy loss from the fundamental IF to the higher order odd harmonics and their mixing products in the power spectrum.
2. Develop an SNR theory to include the effects of less than 100% modulation depth for both chirped sinusoidal and chirped square wave signals.
3. Develop an SNR theory that works for both chirped sinusoidal and chirped square wave signals over the whole range of signal levels, including saturation levels, and for any dead-times, matched filter impulse response times, and clock time intervals.
4. Determine whether or not negative binomial plus Poisson (NBPP) distributed random sampling is alias-free for all spectra for any number of count samples accumulated.
5. For bitstream PC-CAML with a DLLO, investigate detection at a harmonic frequency as used for improved range resolution in bitstream radar.
6. Investigate techniques for suppressing harmonics and sidelobes for application to the bitstream PC-CAML with a DLLO system.
7. Investigate eliminating the high power RF electronics in the bitstream PC-CAML transmitter by using, for example, very low power photonic integrated circuit (PIC) laser sources that can be directly modulated at low voltage and current or followed with low voltage and current PIC waveguide modulators, the modulated output of which is amplified by semiconductor optical amplifiers (SOAs) or optical fiber amplifiers.[ref 22]
8. Perform lab experiments to verify the SNR theory and Monte Carlo simulation results.
9. Build and test breadboard and brassboard bitstream PC-CAML with a DLLO prototypes.

6. Acknowledgments

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