

Variation-Aware Thermal Design for Advanced Packaging: A Systematic Review

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Abstract—Thermal design of flip-chip, 2.5D and 3D packages uses nominal values of features—bond line thickness, voids, coverage, warpage, die thickness, bonded-interface conductance—that are manufactured outcomes with unit-to-unit distributions. This systematic review, conducted to a protocol written before the search and reported following PRISMA 2020, asks what the peer-reviewed literature reports about the magnitude and distribution of such variation, its thermal effect, the metrology that resolves it, and the statistical and specification practice connecting the three. From 2,253 records screened, 388 studies were included (210 on flip-chip, 2.5D and 3D packages; 178 on power-module and LED die attach as an adjacent comparator); the 142 studies carrying quantitative data were extracted, 136 from full text. Normalised sensitivities from 41 studies show that distributed voids raise thermal resistance by 0.5–1.2% per percentage point of area, whereas contiguous or largest voids raise it by 1.5–9% per point along exponential relations with thresholds of 5–40%; bond line raises resistance by 1–5% per micrometre depending on TIM conductivity; and 36–61 μm of warpage produces corner-to-centre temperature-rise ratios of 1.5–2 when the TIM cannot follow the die. Geometric metrology resolves voids, bond lines and warpage to micrometres, but the gauge repeatability of the inspection metrics behind specifications is reported once, and buried bond interfaces cannot yet be measured non-destructively. Only 72 studies apply a statistical treatment or state a specification, and only five derive a permitted variation from a thermal requirement. A gap map identifies the cells without quantitative evidence and proposes five studies to fill them.

Index Terms—Advanced packaging, heterogeneous integration, 2.5D/3D integration, hybrid bonding, thermal interface materials, bond line thickness, voids, warpage, thermal metrology, manufacturing variation, variation-aware design, tolerance design, systematic review.

I. INTRODUCTION

HETEROGENEOUS integration has moved the thermal bottleneck of high-performance packages into the package itself. Flip-chip processors, 2.5D interposer modules with high-bandwidth memory, and hybrid-bonded three-dimensional (3D) stacks now dissipate several hundred watts through a stack of thin layers—die, bonded interfaces, thermal interface materials (TIMs), lids and spreaders—whose thermal resistances are set less by bulk material properties than by the geometry that assembly leaves behind [1]–[3]. Thermal design of these packages is, almost without exception, carried out at nominal values: a bond line thickness (BLT) taken from a process specification, a void-free interface, a flat die, a datasheet thermal conductivity. Yet every one of these quantities is a manufactured outcome with a distribution across units, lots and time. The TIM under a lidded flip-chip package is thinner at the die

centre than at the corners because the substrate and the lid warp differently as they cool [4], [5]; a solder TIM entraps voids whose size follows a log-normal distribution controlled by lid roughness and reflow atmosphere [6]; a polymer TIM loses coverage at the die corners during thermal cycling until a fraction of the die is no longer in contact with the lid [7], [8]; the effective conductivity of the copper pads of a hybrid-bonding layer is 40% below that of a blanket film [9]. Each of these deviations raises the junction temperature of some units above the value the nominal model predicts, and the tail of that distribution—not its centre—decides yield, throttling behaviour and field reliability.

The question this review asks is how well the published literature supports a variation-aware thermal design of advanced packages. Three bodies of work bear on it, and they have grown largely apart. The first is the packaging-process literature, which measures and controls the sources of variation—warpage, coplanarity, void formation, bond-line formation, wafer thinning—usually with mechanical or yield objectives and rarely with a thermal metric attached. The second is the package-thermal literature, which quantifies the effect of a defect or a dimension on a thermal resistance, usually one source at a time, at a nominal base condition, and often for a power module or LED rather than for a flip-chip or stacked logic package. The third is the metrology and statistics literature, which reports what acoustic microscopy, X-ray, profilometry, transient thermal testing or thermoreflectance can resolve, and which occasionally applies designed experiments, Monte Carlo sampling or reliability-based optimisation to a package thermal problem. A designer who wants to know, for example, how much junction-temperature margin a 20% BLT tolerance costs on a large lidded die, what void fraction an acoustic inspection can actually guarantee, and whether that fraction is the right quantity to specify, has to assemble the answer from all three, and no source shows where the answer does not exist.

This paper is a systematic review of that combined literature. It is organised around five questions. What magnitudes and distributions of manufacturing variation have been reported for the thermally relevant features of advanced packages (RQ1)? What thermal sensitivities to those features have been measured or computed, and can they be normalised and compared (RQ2)? What can the available metrology resolve, non-destructively and in-line, at the relevant scale (RQ3)? How have statistical methods and specifications been used to connect variation to thermal outcomes (RQ4)? And where are the gaps—which source-by-evidence cells hold no quantitative data at all (RQ5)? The review follows a written protocol fixed before the search (Supplementary Document S1) and is reported following PRISMA 2020 practice, covers the peer-reviewed literature

TABLE I
VARIATION SOURCES, THEIR REPRESENTATIONS AND THE EVIDENCE TYPES SOUGHT

Source (code)	Definition	Natural unit	Typical representation in the literature
TIM bond line (TIM_BLT)	Thickness of TIM1 (die–lid) or TIM2 (lid/die–sink), nominal and local	μm	Nominal $\pm$ tolerance; centre/corner values; diagonal profile; standard deviation across units (rare)
TIM voids (TIM_void)	Air- or flux-filled cavities within TIM or at its interfaces	% of area (or volume); largest-void size	Single % per unit; process-window %; log-normal size distribution (rare)
TIM coverage / delamination (TIM_coverage)	Fraction of die area in contact through the TIM; separation at an interface	% of area	Initial and post-stress %; failure threshold
TIM property / degradation (TIM_prop)	In-situ conductivity, contact resistance and their change with time	W/mK; $\text{mm}^2\text{K/W}$; % change	Vendor vs in-situ values; relative change vs cycles or hours
Warpage / coplanarity (WARP)	Out-of-plane deformation of die, lid, substrate or heat sink; tilt	μm (peak-to-valley or centre-to-corner)	Value at temperature; JEDEC limit; sample range (rare)
Die thickness / TTV (DIE_THK)	Thickness after thinning and its total variation	μm	Process outcome
Bonded interfaces (BOND)	Hybrid Cu–Cu, micro-bump, fusion or sinter bond geometry, voids and conductance	$\text{m}^2\text{K/MW}$; % voids; μm	Property values; void maps; simulated levels
TSV / BEOL (TSV_BEOL)	Through-silicon-via and back-end-of-line stack geometry, alignment and effective conductivity	W/mK; μm	Mapped or computed values
Die-attach voids (DA_VOID), adjacent	Voids in solder or sinter die attach of power devices and LEDs	% of area; largest-void size	Per-unit % with sample statistics; size distributions
Die-attach bond line / tilt (DA_BLT), adjacent	Thickness and tilt of the die-attach layer	μm	Nominal vs tilted; process window

Evidence types: (A) reported magnitude or distribution of the variation; (B) thermal effect attributable to the variation; (C) metrology capability for the feature; (D) statistical treatment or specification.

indexed through September 2026, and treats the adjacent literature on power-module and LED die attach as a comparator because it is where void-to-thermal-resistance relations have been studied most thoroughly and where the transfer of methods to advanced packages is most direct. Earlier reviews have covered TIM materials and their reliability [10]–[12], the thermal issues of hybrid-bonded HBM [2] and machine-learning prediction of warpage and thermal response [13]; none, to our knowledge, has treated manufacturing variation as the object of study or mapped the evidence by source and by type.

The remainder of the paper is organised as follows. Section II describes the review protocol. Section III characterises the evidence base and presents the coverage matrix. Sections IV to VII answer RQ1 to RQ4 in turn, source by source, with normalised sensitivities collected in Table III and Fig. 4. Section VIII presents the gap map and a research agenda, Section IX states the limitations of the review, and Section X concludes.

II. REVIEW METHOD

A. Protocol and scope

The review was conducted to a written protocol fixed before searching (Supplementary Document S1); the protocol was not deposited in a public registry. Its scope is the peer-reviewed literature on manufacturing variation in the thermally relevant features of advanced electronic packages and its consequences for package thermal performance. “Advanced packages” are flip-chip packages with or without a lid, 2.5D interposer modules, and 3D stacks including high-bandwidth memory and hybrid-bonded stacks; power-module and LED die-attach studies were admitted as an adjacent comparator because their void-to-resistance literature is mature and directly transferable. The variation sources are those listed in Table I: TIM bond

line thickness, TIM voids, TIM coverage and delamination, TIM property and degradation, package or die warpage and coplanarity, die thickness and total thickness variation, bonded interfaces (hybrid, micro-bump and fusion bonds), through-silicon vias and back-end-of-line stacks, and, for the adjacent set, die-attach voids and die-attach bond line. Four evidence types were sought for each source: (A) a reported magnitude or distribution of the variation, (B) a thermal effect—a change of a thermal resistance or of a temperature—attributable to the variation, (C) a metrology capability for the feature, and (D) a statistical treatment or a specification.

B. Eligibility

Records were eligible if they were peer-reviewed journal articles or conference papers in English, published from January 2000 to the search dates according to the index year, that treat at least one source in Table I as a variable rather than a nominal constant, and report at least one of the four evidence types. Studies of TIM materials at a single nominal condition, of nominal thermal design, of second-level (board) interconnect, of electrical or mechanical reliability with no thermal quantity, and of encapsulant or substrate materials with no thermal outcome were excluded. Preprints, patents, standards, theses, news and white papers were excluded. Exclusion codes were E1 (no variation source treated as a variable), E2 (no thermal outcome and no unit-level statistics), E3 (object or level out of scope), E4 (not peer-reviewed, language, document type or publication date), E5 (duplicate report of the same study), and E6 (full text inaccessible). Background records (BG) that describe nominal thermal behaviour of the package classes were retained for context but not synthesised.

C. Information sources and search

The primary source was the OpenAlex scholarly index, searched with 34 sub-queries built from the source and outcome vocabularies of Table I (the full strings and hit counts are in Supplementary Table S2). Thirty sub-queries were executed completely and one partially on 30 September 2026 before the daily request budget of the index was exhausted; the partial sub-query was re-run and the remaining three were executed on 1 October 2026 (deviation D2). Each sub-query was capped at its 3,000 most relevant records; the 34 complete runs retrieved 24,285 records (the retrieval count of the partial run was not recorded), of which 3,274, together with 87 from the partial run, satisfied the package, variation and thermal concept blocks of the protocol on title and abstract, and these 3,361 records merged on OpenAlex work identifier to 2,513 unique records. The 303 records found only by the over-broad die-thickness sub-query (9,834 hits) were set aside (deviation D1), leaving 2,210 database records for screening. Citation chasing was then performed for every study included at the first pass: the reference lists of the 346 studies were retrieved from Crossref (5,431 reference entries resolving to 2,779 unique DOIs; 1,507 entries without a DOI could not be resolved) and their citing works from OpenAlex (3,406 citing-record entries), the concept-block filter was applied to title and abstract, and the 43 records not already screened (25 backward, 18 forward) were screened in the same way. IEEE Xplore and ScienceDirect were used, through an institutional subscription, to obtain full texts, together with open-access repositories. Metadata (title, authors, venue, year, document type, DOI, abstract where available) were taken from OpenAlex for 250 included records at the first pass and from Crossref for the remainder after the OpenAlex daily request budget was exhausted (deviation D2), abstracts unavailable from Crossref being read from the search results; the metadata of every record added on 1 October were taken from OpenAlex, and the reference list was checked against Crossref (Supplementary Table S3e).

D. Selection

Titles and abstracts of all 2,253 records were screened against the eligibility criteria by a large-language-model assistant applying the written codes (Supplementary Document S3f) under the direction of the author; every decision and its code are recorded in Supplementary Table S3a. A 10% random sample of the 2,167 first-pass records (217 records; the sampling seed is recorded in Supplementary Table S3g) was re-screened blind by an independent run of the assistant that saw only the written codes and the titles and abstracts (deviation D4). The two passes agreed on inclusion versus exclusion for 183 of the 217 records (84.3%; Cohen's $\kappa = 0.53$) and on the exact code for 122 (56.2%; $\kappa = 0.44$), the exclusion codes E1–E3 being the main source of disagreement. The 34 inclusion disagreements were adjudicated by re-reading each abstract against the codes: 15 records excluded at the first pass were admitted (the first pass had under-included power-module and LED die-attach studies with a thermal effect and flip-chip warpage studies reporting a magnitude only; one of the 15 was reclassified as background at coding), 2 records included at the first pass

were excluded as system- or board-level objects, and 17 first-pass decisions were upheld; the adjudication is recorded in Supplementary Table S3g. Records marked “check” because the abstract was insufficient were resolved at the coding or full-text stage. Full texts were obtained for open-access reports and, through an institutional library subscription, for IEEE Xplore and ScienceDirect reports; reports for which no full text could be obtained within the review period were coded from their abstracts and, where extracted, flagged “abstract-only” in the extraction table, so that the reader can see which statements rest on abstract-level evidence (deviation D3).

E. Coding, extraction and appraisal

Every included report was coded for package class (flip-chip, 2.5D, 3D, power module, LED, other), variation source(s), evidence type(s) A–D, method (experiment, finite-element, computational fluid dynamics, analytical, surrogate or machine learning), statistical treatment, and a priority for full-text extraction. Type A was assigned when a magnitude, range, tolerance or distribution of the source is reported, whether measured on units or stated as a specification; type B when a change of a thermal resistance or temperature is quantified against the source; type C when a metrology method for the feature is reported with a stated capability; and type D when the study applies a statistical method to the variation or to its thermal effect—a designed experiment or response surface, probabilistic propagation, distribution fitting, process-capability or gauge analysis—or states or derives a specification for the source. Curve fits that merely express a deterministic sensitivity, and uncertainty analyses of a thermal tester, were coded B and C respectively rather than D. Coding was made from titles and abstracts and was reconciled with the full text for every report that was read in full—evidence types, package class, statistical method and the list of variation sources for which a value was extracted—and each reconciliation is logged with its reason in Supplementary Table S3c. Three records retained at screening that proved to carry none of the evidence types were excluded at this stage (E2). The synthesis is two-staged. Every report whose title and abstract indicated a quantified magnitude, thermal sensitivity, metrology capability or statistical treatment (priority H, and priority M where the data appeared transferable) was sought in full and extracted; reports that indicated only nominal-design context, a qualitative statement or a single metrology demonstration (the remaining priority M and all priority L reports) were coded from their abstracts and enter only the coverage matrix of Fig. 2 and the counts of Section III. Every quantitative statement in Sections IV–VII therefore rests on a full text, except the six extraction rows and the citations that are flagged “abstract-level” where they occur. Quantitative data were extracted into one row per study, source and outcome with the fields of the protocol: how the variation is represented (scalar, range, distribution, map, modelled field), its magnitude with the reported statistic and sample size, the metrology and its resolution or uncertainty, the thermal quantity, the thermal sensitivity as reported with its base value, the method, the statistical treatment, and the availability of the underlying data. Values read from figures rather than text or tables are

marked “fig-read”. Each extracted study was appraised on four items: whether the variation magnitude is measured or assumed; whether the thermal method is validated against measurement; whether the sensitivity is reported with a base condition and units that allow normalisation; and whether variability (sample size, spread or confidence) is reported. The appraisal weights the narrative synthesis and does not exclude studies.

F. Normalisation and synthesis

Thermal sensitivities were normalised to the percentage change of the relevant thermal resistance—or of the temperature rise above the reference temperature—per unit of the source in its natural unit: micrometres of bond line, percentage points of void area, micrometres of warpage or gap, and watts per metre-kelvin of conductivity, using the base resistance stated in the study. Where a study reports a non-linear relation, the local slope at the stated base and the value at the largest reported variation are both given. Where a study also reports a spread of the source, a spread-weighted sensitivity (percentage change per one standard deviation of the source) is computed. Sensitivities are summarised per source as a range and displayed as a dot-and-range plot; no pooled effect size is computed because the studies differ in package, method and base condition. Coverage is displayed as a source-by-evidence matrix with study counts, separately for the core and adjacent sets, and the gap map lists the cells with no or qualitative-only evidence.

G. Deviations from protocol

Four deviations are recorded. D1: the eight planned sub-query groups (S1–S8) were implemented as 34 sub-queries in eleven groups because the OpenAlex search operator does not support the nested boolean depth of the full string; three groups were added for metrology terms, for 2.5D, chiplet and HBM package terms, and for unit-to-unit variation terms, the bonded-interface and die-thickness groups were split because their original strings returned few hits, and the die-thickness sub-query that returned 9,834 hits was capped at its 3,000 most relevant records, the 303 records found by it alone being set aside. D2: the OpenAlex daily request budget was exhausted on 30 September before the last three sub-queries (HBM, thermal-yield and unit-to-unit terms) were executed and during the interposer sub-query; these four sub-queries were run on 1 October 2026, one day after the others, and metadata retrieval for the first-pass records switched from OpenAlex to Crossref for 197 records, whose abstracts were taken from the search results (five records were completed from the search results alone). Citation chasing used Crossref reference lists and OpenAlex citing works rather than Google Scholar, and references without a DOI were not resolved. D3: the protocol listed reports whose full text could not be obtained (E6) as not synthesised; because the request budgets and access pauses left 252 of the 388 eligible studies without a full text within the review period, these studies were synthesised at abstract level and flagged rather than excluded. D4: the protocol assigned the blind re-screening of the 10% sample to the author; it was performed by an independent run of the assistant instead, and the disagreement rate, κ and adjudication are reported

in Section II-D so that the reader can weigh the screening reliability. A further limitation that was not a deviation but affected completeness is that IEEE Xplore paused institutional full-text access twice during retrieval; the number of full texts read is reported in Section III and every abstract-level row is flagged.

III. THE EVIDENCE BASE

A. Search and selection

Fig. 1 summarises the selection. The 34 database sub-queries retrieved 24,285 records, of which 3,361 satisfied the three concept blocks on title and abstract; these merged on OpenAlex identifier to 2,513 unique records, and 2,210 remained for screening after the 303 records found only by the capped die-thickness sub-query were set aside (Section II-G). Citation chasing of the 346 studies included at the first pass contributed 43 further records after the same filter (Section II-C). Title/abstract screening of the 2,253 records, including the adjudicated re-screening sample, excluded 1,751 (E1 545, E2 326, E3 663, E4 145, E5 72) and retained 404 for full assessment, together with 98 background records that describe the nominal thermal behaviour of the package classes and are cited in the Introduction and Discussion but not synthesised. At the coding and full-text stage, 8 records were found to be duplicate reports of a study already included (E5) and 8 failed the eligibility criteria (2 with no variation source treated as a variable, E1; 3 with no thermal outcome or statistics and none of the evidence types A–D, E2; 3 out of scope, E3), leaving 388 studies in the synthesis: 210 on the core package classes (162 flip-chip, 8 2.5D, 36 3D or HBM stacks, 3 that cover both a flip-chip and a power package, and 1 generic package model) and 178 on the adjacent classes (109 power modules or discrete power devices, 44 LEDs, and 25 other). Of the 388, 44 were added by the completed search and the re-screening (5 by the four sub-queries run on 1 October, 11 by backward and 14 by forward citation chasing, and 14 by the adjudication of the re-screening sample) and 2 first-pass studies were removed, so the first pass had found 89% of the final set. Full texts were read for 136 of the 388—100 IEEE reports, 16 Elsevier reports, 14 IMAPS and other society reports, 3 MDPI, 2 ASME and 1 AIP report, obtained through the institutional subscriptions and open-access repositories—covering 116 of the 140 studies given high priority for quantitative extraction; the remaining 252 studies were coded from their abstracts, and the six extraction rows in Supplementary Table S4 that rest on an abstract alone are flagged.

B. Character of the literature

Two thirds of the studies (241 of 388) are conference papers—chiefly ECTC, ITherm, SEMI-THERM, THERMINIC, EPTC, ICEPT and the IMAPS symposia—and 147 are indexed as journal articles (some of them society proceedings indexed as such), led by the ASME Journal of Electronic Packaging, the IEEE Transactions on Components, Packaging and Manufacturing Technology and its predecessors, IEEE Transactions on Device and Materials Reliability, and Microelectronics Reliability. The literature is recent and accelerating (Fig. 3): 182 of the 388

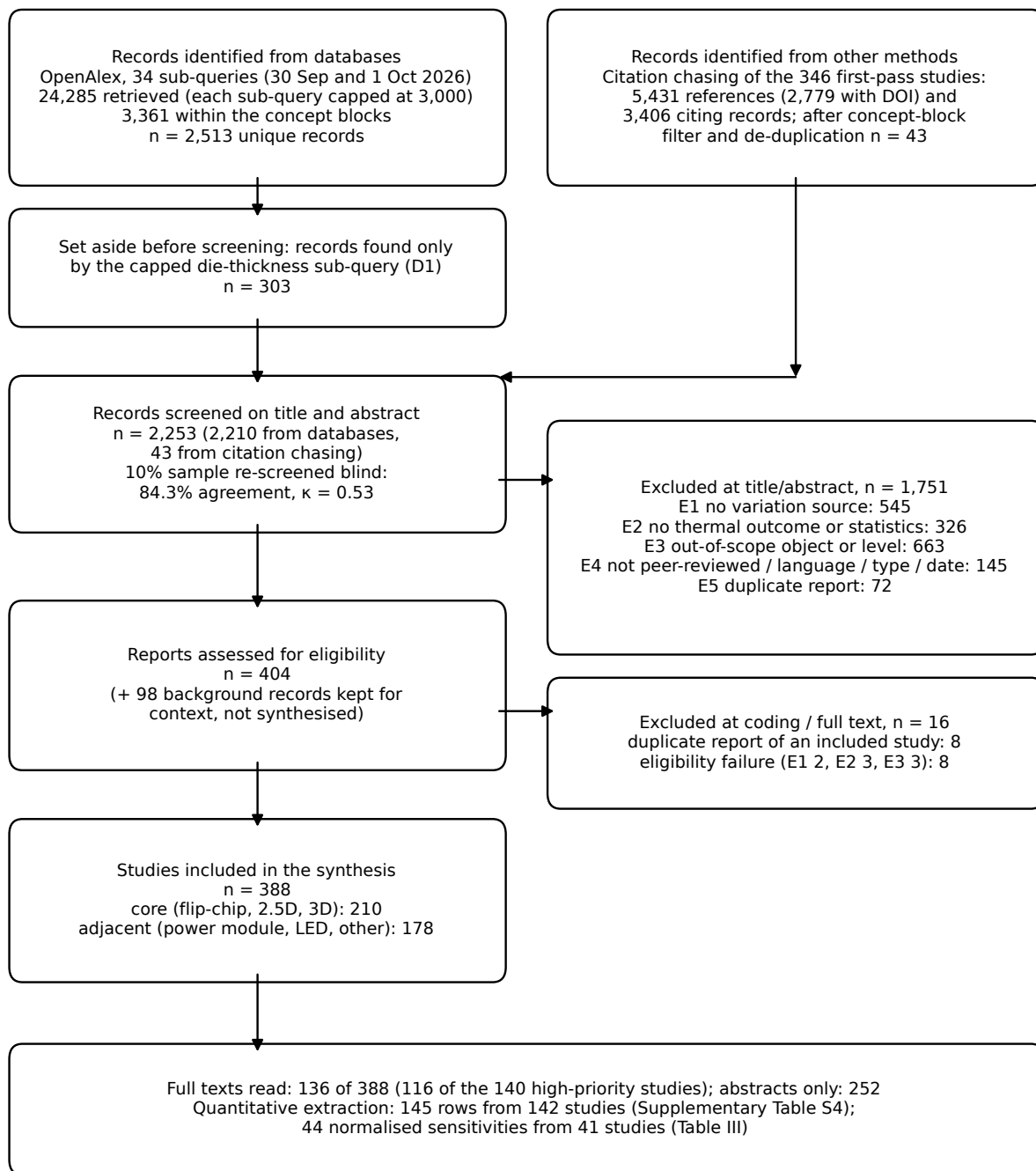


Fig. 1. Flow of records through the review (PRISMA 2020 style) with the database and citation-chasing streams. E1–E5: exclusion codes of Section II-B; D1: protocol deviation of Section II-G.

studies appeared in 2021–2026 and 239 since 2016. The recent growth is shared by the package classes—74 flip-chip, 23 3D/HBM and 58 power-module studies appeared in 2021–2026 against 16, 4 and 22 in 2016–2020—whereas the 2006–2010 peak was about two thirds flip-chip TIM work. Experimental work dominates: 292 studies report measurements, 240 of them measurements alone, whereas 96 report no measurement

(finite-element models in 63 of them, analytical or phonon-transport models in 13, CFD in 5, surrogate or machine-learning models in 10, two studies combining methods, and 7 overviews, specifications or condition-monitoring methods that report no thermal method). Across the whole set, finite-element models are used in 106 studies, analytical models in 19, CFD in 7 and surrogate or machine-learning models in 12.

The evidence types are unevenly represented. Of the 388

	(a) Core: flip-chip, 2.5D, 3D (n = 210 studies)				(b) Adjacent: power modules, LEDs, other (n = 178 studies)			
	Magn.	Thermal	Metrol.	Stat./spec.	Magn.	Thermal	Metrol.	Stat./spec.
TIM voids	36	18	21	12	2	1	0	0
TIM bond line	44	44	29	8	4	5	1	0
TIM coverage / delamination	21	14	10	5	0	2	0	1
TIM property / degradation	17	49	18	3	2	14	3	1
Warpage / coplanarity	38	33	22	12	8	5	3	4
Die thickness / TTV	4	0	1	1	2	1	0	1
Bonded interfaces	10	6	10	5	1	1	2	0
TSV / BEOL	7	5	4	1	0	0	0	0
Die-attach voids	2	2	1	0	53	82	36	26
Die-attach bond line / tilt	1	1	0	0	10	12	6	3

Fig. 2. Coverage matrix: number of synthesised studies reporting each evidence type for each variation source, (a) core flip-chip, 2.5D and 3D packages and (b) adjacent power-module, LED and other packages. A study contributes to every cell it reports.

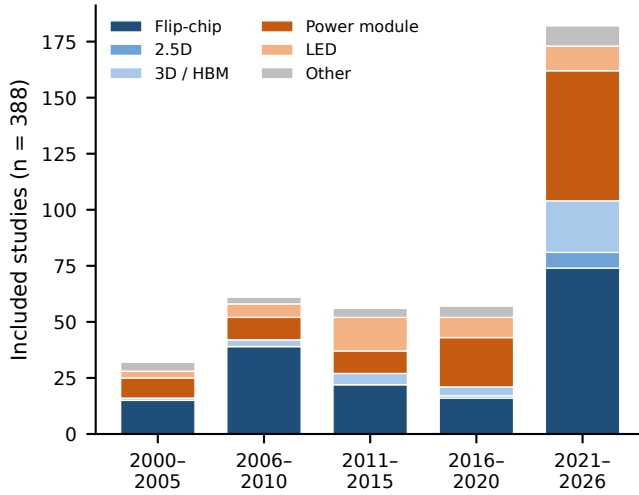


Fig. 3. Synthesised studies by publication period and package class (n = 388).

studies, 79 report metrology capability only (type C) and 79 report a thermal effect only (type B, usually a parametric simulation or a single test-vehicle comparison at a nominal condition); 44 report a magnitude only (type A). Eighty-one studies report both a magnitude and a thermal effect (types A and B), which is the combination a variation-aware model

needs, but 42 of them report nothing else, and only 39 report A, B and either a metrology capability or a statistical treatment. A statistical treatment or a specification (type D, as defined in Section II-E) appears in 72 studies, 29 of them in the core set.

C. Coverage matrix

Fig. 2 arranges the 388 studies by variation source and evidence type, separately for the core and adjacent sets; a study contributes to every cell of every source it reports. Three features stand out. First, the core evidence is concentrated on the TIM: TIM bond line (67 core studies), TIM property and degradation (56), warpage (52) and TIM voids (46) account for most of the core cells, and within them the thermal-effect column is well populated for properties (49 of 56), bond line (44 of 67) and warpage (33 of 52) but thinner for voids (18 of 46) and coverage (14 of 22). Second, the sources that distinguish 2.5D and 3D packages from flip-chip—bonded interfaces (17 core studies), TSV/BEOL stacks (9) and die thickness (4)—are represented mainly by metrology and magnitude studies; their thermal-effect cells hold 6, 5 and 0 entries (eight distinct studies, three of which count in both rows), nearly all simulations; the measured contributions are a wafer-level TSV thermal test key and a 2001 laser-flash characterisation of the interfaces of a bare-die stack with copper through-vias, the latter available to this review only as an abstract. Third, the adjacent die-attach literature is the deepest in the matrix (109 adjacent studies on die-attach voids,

82 with a thermal effect and 26 with a statistical treatment or specification) and is the only place where the same source has been measured, modelled, imaged and specified by many independent groups. The statistics/specification column is thin in the core set (29 studies, of which 12 concern TIM voids and 12 warpage), and in the die-thickness and TSV/BEOL rows it holds a single study each—a thickness distribution after extreme thinning and a simulated tile-to-tile spread of BEOL conductivity.

IV. MAGNITUDES AND DISTRIBUTIONS OF VARIATION (RQ1)

Table II collects the reported magnitudes by source, with the form in which each is reported—a single value, a range, a map, or a distribution with a sample size—because only the last of these can be propagated to a temperature distribution. This section reads the table for mechanisms and for the few places where a distribution, rather than a value, is available.

A. TIM bond line thickness

The bond line of a polymer or gel TIM1 is nominally 20–100 μm and is set by three things that vary independently: the assembly process, the incoming material, and the warpage of the die and lid. Its spread is reported in three forms (Table II). As a specification—a tolerance around the nominal, such as $50 \pm 20 \mu\text{m}$ [14] or a shim-controlled $97 \pm 4 \mu\text{m}$ [15]—it describes the intent, not the outcome. As a unit-to-unit statistic it is reported in a single core study: on a 65 mm high-performance FCBGA the BLT of paste-type TIMs had a standard deviation of about 20% of the mean, against about 6% for a graphite sheet whose thickness is fixed by the sheet itself [16]. As a spatial map it is the best documented: the bond line is systematically thicker at the die corners than at the centre because the substrate and the lid warp differently, by a factor of about two in cross-sections of an FC-PBGA [4] and by a factor of three to four in simulated and analytical maps of lidded packages [5], [17], and the map moves with temperature—the centre BLT grows and the corner BLT shrinks as the package heats—as in-situ laser profilometry [5], spatially resolved thermal measurements [18] and frequency-domain impedance measurements [19] all show. Two process mechanisms add to warpage: particle stacking during squeeze flow, which sets a minimum bond line near the largest filler diameter and leaves diagonal “paste-cross” lines of non-uniform thickness [20], and the squeezing rate, which changes the final BLT by about 30% [21]. For TIM2 under a heat sink the dominant mechanism is tilt from the loading hardware, which is worst for bare-die packages (a worst-case average of about 333 μm against 21 μm for a molded package) [22]; on a 2.5D module a 2 μm tolerance was needed to reconcile the BLT and warpage maps [23].

B. TIM voids

Void area in TIM1 is reported almost always as a single percentage per unit and rarely as a distribution. The values span two orders of magnitude and are governed by the process rather than by the material: for indium TIM1, fluxless or vacuum

reflow gives 1–4%, pressure legs 10–13% and a non-optimised profile 36% [24]–[26], whereas an established process grows only 0.07–0.18% in 1,000 h at 125 °C [27]. The only void-size distributions in the core set are the log-normal fits of Qiu et al., in which the mean void diameter rose from 320 to 450 μm and the mean void fraction from 23% to 29% as the lid roughness increased under atmospheric reflow, but hardly at all under positive-pressure curing [6]. The mechanism that links voids to the other sources is shape: a CFD wetting model validated against C-SAM to within 1% showed near-zero voiding for concave lids below 60 μm peak-to-valley and a sharp rise beyond, and zero voiding when a 60 μm concave lid was matched to a 60 μm convex die [28]; a substrate deflection of about half the bond line prevented wetting altogether [24]; and on a 65 mm FCBGA the indium void after three reflows correlated with the warpage change between 150 and 260 °C [29]. Polymer TIM1 voids are usually smaller, but a heat-curable TIM on a large die voided up to 25% of the die area in a ring near the perimeter attributed to warpage [30], and six of six modules built from one in-specification lid lot and one in-specification TIM lot voided to a mean of 2.0% [31]. Only one core study treats TIM1 void content probabilistically, sampling an areal void distribution of 1–7% at the two TIM interfaces in 3,000 Monte Carlo trials [32].

C. TIM coverage and delamination

Coverage is the complement of voids and delamination and is the quantity most often tracked through reliability testing, so it is the one TIM feature for which a time series across stress is routinely reported (Table II): indium coverage falling from above 90% to about 20% after 1,000 thermal cycles on an FCLGA, with delamination initiating at the die–TIM interface [7]; polymer TIM1 coverage falling to an average of 58.5% after 1,800 thermal-shock cycles, tabulated for six groups of eight samples, with 60% adopted as the failure threshold [8]; and thermoset TIMs losing 6–8% after 1,200 cycles [33]. The driver is again warpage: an indium TIM degraded at the die corners as the substrate warpage rose to 184 μm above 150 °C while the lid stayed within 20 μm [34], adhesive separation at the chip centre appeared under power cycling but not under isothermal aging because the sealband is in tension only during cycling [35], and on warped bare dies the corners lose contact wherever the compressible thickness of a pad TIM (17 μm for a 100 μm pad) is smaller than the warpage height (36–61 μm) [36], [37]. As-built coverage on a 77.5 mm test vehicle was 65–95% depending on the TIM type [38].

D. TIM property and degradation

The property variation that matters for the package is not the vendor conductivity but the in-situ effective conductivity and contact resistance and their change with time. Interface-inclusive effective conductivities back-calculated from θ_{JC} , coverage and BLT were about 40% below the vendor values for silicone and graphite TIMs [38]; a gap filler mapped at 10 μm resolution had a conductivity of $4.39 \pm 0.68 \text{ W/mK}$, a

TABLE II
REPORTED MAGNITUDES OF VARIATION BY SOURCE (CORE PACKAGES UNLESS NOTED)

Source	Reported magnitude	Form	Studies
TIM1 bond line, nominal	20–100 μm polymer/gel; below 20 μm demonstrated; solder preforms $\geq 100 \mu\text{m}$ with 30–50 μm collapse; 102–508 μm preforms in process studies	nominal	[18], [24], [25]
TIM1 bond line, spread	$50 \pm 20 \mu\text{m}$ (spec); $97 \pm 4 \mu\text{m}$ (shim); sd $\approx 20\%$ of mean for paste TIMs vs $\approx 6\%$ for graphite sheet on a 65 mm package (units)	spec; sd	[14]–[16]
TIM1 bond line, map	$\times 2$ centre-to-edge (FC-PBGA cross-sections); 30 μm centre / 82 μm corner after cure, reversing at 265 $^{\circ}\text{C}$ (FCLBGA, simulated); 24 μm centre / 97 μm corner (analytical, 200 W); in-situ BLT vs temperature measured	map	[4], [5], [17]–[19]
TIM1 bond line, process	Minimum BLT set by particle stacking (D99 $\approx 10 \mu\text{m}$); +30% BLT at high squeezing rate; printed deposits 2–3 mil against 1 mil target	mechanism	[20], [21], [135]
TIM2 bond line / tilt	Heat-sink tilt: worst-case average BLT $\approx 333 \mu\text{m}$ (bare die) vs $\approx 21 \mu\text{m}$ (molded); BLT map from warpage within 2 μm on a 2.5D module	map	[22], [23]
TIM1 voids, solder	1.1–2.3% (formic-acid fluxless), 9.8–13.2% (pressure), 36.4% (non-optimised); 15.9% $\rightarrow$ 3.8% across vacuum-reflow profiles; 1.6–2.9% fluxless vs up to 35% with flux residue; 0.07–0.18% growth after 1,000 h; 1.1% after nine reflows with plasma-treated BSM (abstract-level)	process window	[24]–[27], [136]
TIM1 voids, solder, distribution	Log-normal diameters: mean 320 $\rightarrow$ 450 μm and fraction 23.1 $\rightarrow$ 28.9% as lid Ra rises from < 0.2 to 0.8–1.0 μm (atmospheric); 165 $\rightarrow$ 172 μm under positive pressure	distribution	[6]
TIM1 voids, shape-driven	Near-zero for concave lids $< 60 \mu\text{m}$ PV, sharp rise beyond; zero for 60 μm concave lid on 60 μm convex die; indium void correlated with 150–260 $^{\circ}\text{C}$ warpage change; non-wetting when substrate deflection $\approx 50\%$ of BLT	mechanism	[24], [28], [29]
TIM1 voids, polymer	2.0% mean (6/6 modules, in-spec lid and TIM lots); up to 25% of die area on a large-die package (ring void from warpage); 0–1.3% after 500 cycles; > 30 voids on printed deposits vs none dispensed; 1–7% areal content sampled in Monte Carlo	per unit; MC	[30]–[32], [88], [135]
TIM coverage after stress	Indium $> 90\% \rightarrow \approx 20\%$ after 1,000 cycles; polymer TIM1 average 58.5% after 1,800 shock cycles at 30 psi (tabulated per sample); -6% average / -8% worst after 1,200 cycles; corner/edge degradation with substrate warpage to 184 μm ; as-built 65–95% at 80–300 μm on a 77.5 mm vehicle	per unit; tables	[7], [8], [33], [34], [38]
TIM in-situ properties	Interface-inclusive $k \approx 40\%$ below vendor (silicone, graphite); gap-filler k map $4.39 \pm 0.68 \text{ W/mK}$ at 10 μm (sd 15%); layered vs bulk coupons 1.7 vs 3.1, 0.6 vs 0.8, 21 vs 12.5 W/mK; grease k 3–5 W/mK with R_c 5–10 $\text{mm}^2\text{K/W}$ ($\pm 17\%$); viscosity of > 190 TIM lots, $R^2 = 0.083$ vs modulus	map; lot	[30], [31], [38]–[40]
TIM degradation	Grease pump-out after ≈ 985 cycles; contact-area loss within 30 cycles, stable by 100; +45% resistance after 4,500 power cycles; T_j rise after $\approx 10,000$ power cycles for one grease supplier vs $< 5.1\%$ change over 18,000 for another; aging degradation larger at 150 $^{\circ}\text{C}$ than at 100–125 $^{\circ}\text{C}$; saturation-model fits (mean + 2.3 sd) with Arrhenius scaling	relative change	[35], [41]–[45]
Warpage, flip-chip	Bare die 36–61 μm centre-to-corner (16 mm), 36 $\rightarrow$ 9 μm at 400 kPa (abstract-level); 40 $\mu\text{m} \rightarrow < 5 \mu\text{m}$ on board mounting (corners 15 μm flatter); lid 76 μm (25 $^{\circ}\text{C}$) $\rightarrow$ 20 μm (150 $^{\circ}\text{C}$), substrate 107 $\rightarrow$ 184 μm ; laminate 40.8 μm (U-lid) vs 31.9 μm (W-lid); lid flatness lot means 17.3–23.3 μm ; $\approx 200 \mu\text{m}$ diagonal on a 25 mm test chip	value; lot mean	[31], [34], [36], [37], [46], [47], [93]
Warpage, CSP/molded (FCCSP core; molded and PBGA adjacent)	12–62 μm (25 $^{\circ}\text{C}$) and 35–74 μm (245 $^{\circ}\text{C}$) vs 100 μm JEDEC limit, grouped mean 97 μm for one option and one lot breaching 100 μm (FCCSP); nine molded samples span 133 μm (start) / 60 μm (min) / 85 μm (260 $^{\circ}\text{C}$); material scatter propagated to warpage bounds (PBGA)	range; bounds	[48]–[50]
Wafer-level bond warpage voids)	Pre-bond nanotopography 3σ and local warp separate good and bad hybrid-bonding lots (CSAM	3σ per site	[51]
Die thickness / TTV	TTV worsens with removal depth in extreme thinning; thin die ($< 50 \mu\text{m}$) tolerates central void of only 0.28% of area (RF power package)	process; FE	[52], [53]
Bonded interfaces	Fusion-bond TBR 0.2 and 0.5 $\text{m}^2\text{K/MW}$ (200 / 470 nm SiO_2); hybrid-bond Cu pads 160–220 W/mK ($\approx -40\%$ vs blanket) with perimeter air gap; tile-to-tile sd of bonding-layer conductivity computed; hybrid-bond voids from particles/topography	property	[9], [54], [56], [57]
TSV / BEOL	BEOL stack conductivity mapped layer by layer (28–3 nm), Kapitza length $\approx 2 \mu\text{m}$ SiO_2 ; tile-wise conductivity tensor with sd; TSV misalignment and bump height 21–42 μm as simulation levels	map; levels	[56], [58], [59]
Die-attach voids (adjacent)	1,800 LEDs: $< 4\text{--}5\%$ average (best paste 1.5%), means and sd by type; 70 assemblies: 5,119 voids, mean radius 0.08 mm, sd 0.11 mm; three LED types: 721–2,474 voids, Cpk 1.9–4.1; PQFN 7.0–39.3% (80 units); TO-247 total $\leq 23.2\%$, largest $\leq 16.6\%$; MOSFETs 0–55% with cycling; power module 20.2% vs 10.7% by process; log-normal diameter fits as model inputs	distributions	[61]–[66], [69]–[71]
Die-attach bond line / tilt (adjacent)	Void-rate minimum for full-area preforms of 180–240 μm ; die tilt 50 $\rightarrow$ 75 μm ; Ag-sinter and SAC bond lines 8–98 μm with voids by CSAM	process window	[72], [73], [113]

spatial standard deviation of 15% of the mean [39]; layered coupons differed from bulk values in both directions [30]; and phase-sensitive thermoreflectance separated a grease's bulk conductivity (3–5 W/mK) from its contact resistance (5–10 mm²K/W) with an overall uncertainty of about 17% [40]. Incoming-material variation across lots is documented once, as the viscosity of more than 190 TIM lots over several years and the modulus of two lots at opposite ends of the range, the two uncorrelated ($R^2 = 0.083$) [31]. Degradation with time is reported as a relative change of resistance rather than as a distribution—pump-out, dry-out and contact-area loss over hundreds to thousands of cycles (Table II) [35], [41]–[44]—with one exception: a saturation model of the form $R(t) = R_0 + \theta_2[1 - \exp(-(t/\alpha)^\beta)]$ with Arrhenius temperature scaling, fitted to phase-change TIM2 data reported as mean plus 2.3 standard deviations [45].

E. Warpage and coplanarity

Warpage is the best-quantified source in the set because it is measured routinely for assembly yield, and the reported magnitudes span from 5 μm to 200 μm depending on package, temperature and mounting (Table II). Three regularities matter for the thermal path. First, the warpage that the TIM sees is the mismatch between two moving surfaces, not a single value: a lid that is 76 μm convex at room temperature flattens to 20 μm at 150 °C while the substrate under it rises from 107 to 184 μm [34]. Second, mounting and clamping change it by more than the unit-to-unit spread: a 40 μm bare-die package flattened to below 5 μm when soldered to a motherboard, with the corners 15 μm flatter mounted than unmounted [46], and a 36 μm unloaded die warpage flattened to 9 μm at 400 kPa (abstract-level value) [47]. Third, sample-to-sample variation is reported in only two studies, both outside the core set—nine molded bilayer samples spanning 133 μm at the start of heating and 85 μm at 260 °C, with the extremes cylindrical rather than spherical [48], and material-property scatter measured on ten samples propagated to warpage bounds for a 17 mm PBGA [49]—while in the core set the JEDEC coplanarity limit frames the numbers, with a grouped mean of 97 μm for one FCCSP option against a 100 μm limit that a second lot breached [50], and lot averages of lid-cavity flatness of 17–23 μm over 12 lids $\times$ 24 cavities [31]. At the wafer level, pre-bond nanotopography and local warp measured by patterned-wafer-geometry interferometry separated good from bad hybrid-bonding lots through their within-site three-sigma statistics [51].

F. Die thickness and total thickness variation

The set contains no study that reports the distribution of die thickness in an advanced package together with a thermal outcome. Extreme thinning to 5 μm for wafer-to-wafer stacking is characterised by damage, roughness and thickness maps, with the total thickness variation at the wafer edge degrading once more than about 20 μm of silicon is removed by CMP [52]; a thin-die (below 50 μm) RF power package is the only case in which die thickness enters a thermal analysis, as a factor that lowers the tolerable void size [53].

G. Bonded interfaces

For hybrid, micro-bump and fusion bonds the reported magnitudes are property values and defect statistics rather than unit distributions: fusion-bond thermal boundary resistances of 0.2 and 0.5 m²K/MW for 200 and 470 nm of SiO₂ [54]; damascene copper pads of 5 μm radius with a conductivity of 160–220 W/mK, about 40% below blanket films, with a nanoscale air gap at the pad perimeter [9]; molecular-dynamics evidence that nanoscale pores on the copper side of a Cu/SiO₂ interface suppress interfacial conductance far more than pores on the oxide side (abstract-level) [55]; and the tile-to-tile standard deviation of the effective conductivity of a hybrid-bonding layer computed from layout data [56]. Void formation in hybrid Cu bonding is attributed to particles and surface topography, with a linear particle-size-to-void-size relation that yields a particle-screening criterion of 46 μm for a 1,000 μm void limit [57], and at wafer scale to nanotopography and local warp [51]. Micro-bump height (21–42 μm) and TSV misalignment enter one simulation study as design levels rather than measured distributions [58].

H. TSV and BEOL stacks

The effective thermal conductivity of BEOL interconnect stacks was mapped layer by layer for 28 nm to 3 nm chips, with a Kapitza length of about 2 μm of SiO₂-equivalent for the whole stack [59]; a multiscale model computed the in-plane distribution of the BEOL conductivity tensor over 144 tiles with its standard deviation [56]; and a thermal test key was built to detect seams and voids in blind TSVs on 300 mm wafers before thinning [60]. No study reports the wafer- or lot-level variation of these quantities.

I. Die-attach voids and bond line (adjacent)

The adjacent literature reports void statistics far more completely, and its reporting practice is the model the core literature lacks: distributions with sample sizes for 1,800 LEDs [61], for 70 flip-chip LED assemblies with 5,119 individual voids (mean radius 0.08 mm, standard deviation 0.11 mm) [62], for three automotive LED types with right-skewed diameter distributions and solder-coverage Cpk of 1.9–4.1 [63], for 80 PQFN power packages (7.0–39.3% total void) [64], for ten TO-247 IGBTs with both total and largest void reported [65], for MOSFETs aged to 10,000 cycles [66], [67], for two groups of nine LED chip-scale packages [68] and for power modules before and after a process change [69]. Log-normal void-diameter distributions with fitted parameters are used as inputs for random-void models of IGBT solder layers [70], [71]. The process window for solder thickness has been mapped—a void-rate minimum for full-area preforms of 180–240 μm , thinner layers voiding under cycling and thicker ones trapping bubbles [72]—and die tilt from non-uniform die-attach BLT (50 μm nominal against 75 μm tilted) has been measured by cross-section [73]. Specification limits of 5–10% for power-module die attach [74], 5% for clip-bonded MOSFETs [75], 25% for BGA-type joints under IPC-A-610 [63], 40% under IPC-A-610F as cited for LED die

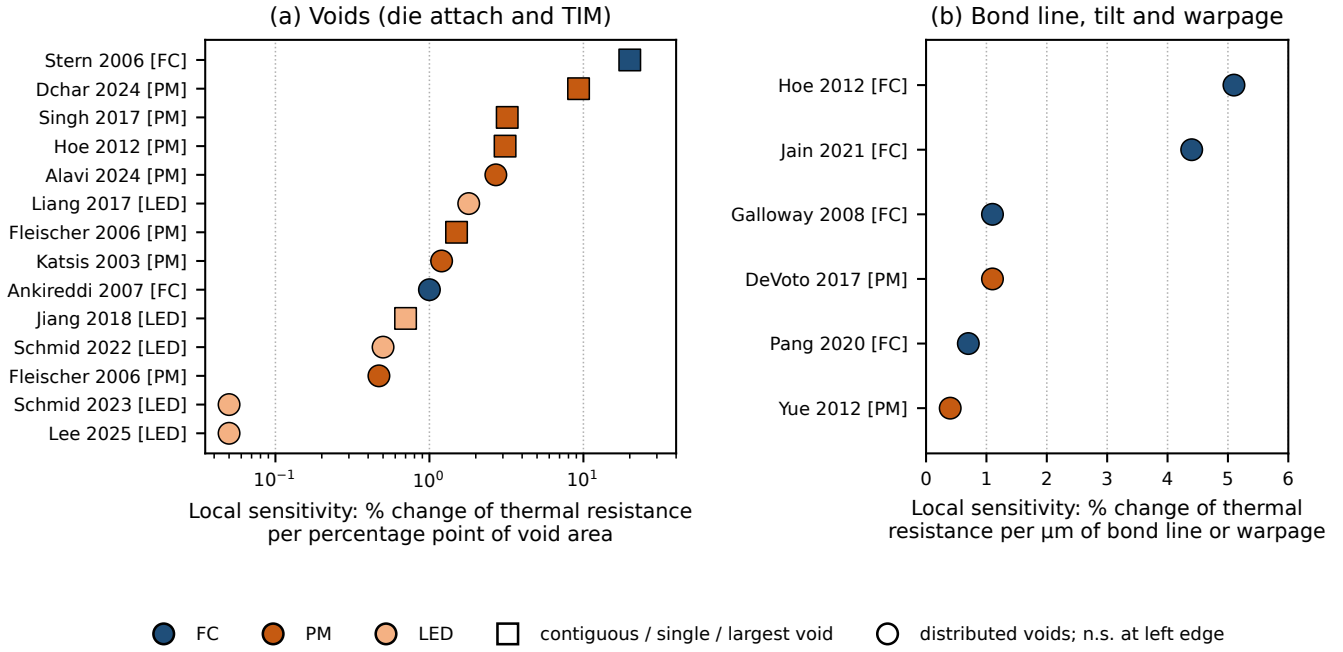


Fig. 4. Local thermal sensitivities normalised per unit of the variation source (Table III): (a) percentage change of thermal resistance per percentage point of void area, log scale; studies reporting no significant effect are plotted at the left edge; (b) percentage change per micrometre of bond line, tilt or corner warpage. Marker colour gives the package class; squares denote contiguous, single or largest-void metrics and circles distributed voids.

attach [68], and 50% total with 15% for a single void under MIL-STD-883 method 2030 [76] recur through the set.

V. THERMAL SENSITIVITIES (RQ2)

Table III lists every thermal sensitivity that could be normalised to a percentage change of thermal resistance (or of temperature rise) per unit of the source, with the base condition and the largest variation reported, and Fig. 4 plots the local sensitivities for the two sources with enough entries to compare: voids, per percentage point of area, and bond line or warpage, per micrometre. No pooled value is computed; the spread across studies is itself the finding.

A. Voids

Thirteen studies give a void sensitivity that can be expressed per percentage point of area (fourteen relations, Table III), and they fall into two populations that differ by an order of magnitude. Distributed or random voids produce 0.5–1.2% of resistance per percentage point in the measured studies: the linear relation $\theta_{jc} = 0.007V + 1.499$ for etched random voids in a chip-scale die attach, i.e. about one third higher at 73% voiding [77]; +50% of transient impedance at 40–45% voided area in aged MOSFETs [66]; +5% of solder-and-substrate resistance per 10 points on a flip-chip LED [61]; and, for TIM1 under a flip-chip lid, a Monte Carlo mean of +4% at 4% and +10% at 7% interfacial void content [32]; two studies sit above this band—+48% for 3–30% of mapped eutectic voidage in a flip-chip UV-LED (1.8% per point on average, about 3% per point between 20 and 30%) [78], and random void configurations in an IGBT finite-element model in which every

case at 7.5% voiding exceeded the +20% end-of-life criterion (2.7% per point) [79]. Contiguous, single or “largest” voids produce 1.5–9% per point and follow exponential or power-law relations: $\theta_{jc} = 1.427 \cdot \exp(0.015V)$ for contiguous etched voids (+200% at 73%) [77]; $\theta_{JC} = 0.1 \cdot \exp(0.032 \cdot V_{\text{largest}})$ for TO-247 IGBTs, where the largest-void metric predicted the resistance and the total-void metric did not [65]; +557% for a 60% single void in a clip-bonded MOSFET, with the resistance rising exponentially once the 5% assembly criterion was exceeded [75]; and a 3.5-fold increase from 0 to 80% central void in a QFN with a low-conductivity die attach [14]; the one exception is a single central void in a white-LED chip-scale package, whose small share of the thermal path gave only +29% at 40% (0.7% per point) [68]. The extreme value in the set, a 7-fold resistance increase for a 30% contiguous void placed over a hot spot in a solder TIM1 [80], and the rule that voids below 0.3% of the die area already degrade a thin-die RF package when they sit under the heat path [53], mark the other end of the same physics: what matters is the spreading resistance around the largest void relative to the local heat flux, not the void area. Two further regularities are consistent across studies. A threshold exists below which voids have no measurable effect—5% for clip-bonded MOSFETs [75], about 5% porosity for random IGBT voids [70], 10% for LED lifetime [81], 20% for etched voids [77], 25% within the IPC limit for automotive LEDs [63], and about 40% for distributed vertical voids in an IGBT solder when the die attach is a small fraction of the module resistance [82]—and, since a die attach contributes only about 15% of a module’s resistance [83] whereas a TIM1 contributes 30–50% of a flip-chip package’s junction-to-case budget [84], the threshold can

TABLE III
NORMALISED THERMAL SENSITIVITIES (ONE ROW PER STUDY $\times$ SOURCE; LOCAL VALUE AT THE STATED BASE, AND VALUE AT THE LARGEST VARIATION REPORTED)

Study	Pkg.	Source	Unit of variation	Base condition	Reported relation	Local sensitivity (% per unit)	At largest variation	Largest variation	Method
[77]	PM	DA VOID	pct-point void area	θ_{jc} 1.50 °C/W, CSP die attach	random voids: $\theta = 0.007V + 1.499$ (linear)	0.47	+34% (fitted; paper states about 30%)	73	EXP
[77]	PM	DA VOID	pct-point void area	θ_{jc} 1.43 °C/W, CSP die attach	contiguous voids: $\theta = 1.427 \exp(0.015V)$	1.5	+200%	73	EXP
[65]	PM	DA VOID	pct-point largest void	θ_{jc} 0.1 K/W, TO-247 IGBT	$\theta = 0.1 \exp(0.032V)$, V = largest-void area (%); total-void rate 0.019	3.2	+80%	16.6	EXP
[66]	PM	DA VOID	pct-point void area	Z_{th} (10–50 ms), power MOSFET	+50% at 40–45%; +100% at 50–55%	1.2	+100%	55	EXP
[32]	FC	TIM void	pct-point interfacial void (random)	R_{jc} , flip-chip 75 μ m TIM1 k = 5 W/(m·K)	Monte Carlo: +4% at 4%, +10% at 7% (mean); worst-case centred void +18% at 4%	1.0	+10% mean / +18% worst	7	FE;MC
[80]	FC	TIM void	pct-point void area (contiguous, over hot spot)	TIM1 joint resistance, solder TIM1	30% area void: 7 $\times$	20	+600%	30	EXP;FE
[14]	PM	DA VOID	pct-point central void	R_{jc} , QFN low-k die attach (< 8 W/(m·K))	0 to 80% central void: 3.5 $\times$	3.1	+250%	80	FE
[75]	PM	DA VOID	pct-point single void	R_{jc} , clip-bonded MOSFET	measured 60% single void: +557%; 20%: single +0.3 vs multiple +0.2 °C/W (FE)	9.3	+557%	60	EXP;FE
[79]	PM	DA VOID	pct-point void area (random configurations)	R_{th} 0.470 °C/W, IGBT	7.5% void: all 20 random cases > +20%; 5%: some cases	2.7	+20%	7.5	FE;EXP
[78]	LED	DA VOID	pct-point voidage (AuSn eutectic 3 μ m)	R_{js} 3.3 K/W, flip-chip UV-LED	3/10/20/30%: 3.3/3.6/3.9/4.9 K/W	1.8	+48%	27	EXP
[68]	LED	DA VOID	pct-point central void volume	solder-layer resistance, LED CSP	0 to 40%: +29%	0.7	+29%	40	FE
[61]	LED	DA VOID	pct-point void area	R_{th} -S&S, flip-chip LED (FC-SP1)	+0.3 K/W per 10 points = +5.0% R_{th} -S&S (+2.8% R_{th})	0.5	+5%	10	EXP
[63]	LED	DA VOID	pct-point void area	R_{th} , automotive LEDs	no significant correlation below 25% (one type weak, rho 0.58)	~ 0	n.s.	25	EXP
[81]	LED	DA VOID	pct-point void area	lifetime and R_{th} , LEDs	voids below 10%: no significant influence ($r = 0.05$)	~ 0	n.s.	10	EXP
[74]	PM	DA VOID	mm2 void area (position-dependent)	local R_{th}^* 0.554 K/W, IGBT centre	$R_{th}^* = 0.174 A_{void} + R_{th0}(x)$	31 %/mm2	n/a	1.5 mm2	FE
[76]	PM	DA VOID	void location (distance to source)	θR 0.26 °C/W, chip-level power package	0.26 (far) to 0.31 °C/W (adjacent)	n/a	+19%	n/a	FE
[53]	PM	DA VOID	pct-point void area (thin die)	R_{jc} , RF power package	void > 0.28–0.3% of area under heat path degrades thin-die R_{jc} to thick-die level	n/a	threshold	0.3	FE
[85]	PM	DA VOID	pct-point void fraction	chip-surface temperature difference 9.6 °C, IGBT	0 to 40%: 9.6 to 109.9 °C	n/a	+1045% (non-uniformity)	40	FE
[14]	FC	TIM BLT	μ m BLT	R_{jc} , FC-BGA low-k TIM (2 W/(m·K))	15 to 200 μ m: up to 10.5 $\times$, near-linear	5.1	+950%	185	FE
[88]	FC	TIM BLT	pct of nominal BLT	θ_{jc} , HFCBGA polymer TIM	$\pm 20\%$ BLT $\rightarrow \pm 10\%$ θ_{jc}	0.5 %/°C	+10%	20%	EXP
[42]	PM	TIM BLT	μ m BLT	R about 24 mm ² K/W at 75 μ m, grease k 3.7 W/(m·K)	dR/dBLT = 1/k = 0.27 mm ² K/W per μ m (five greases 0.27–1.4)	1.1	n/a	225	EXP
[73]	PM	DA BLT	μ m (die tilt)	R_{jc} 0.53 °C/W, TO-251 (50 μ m nominal)	tilt to 75 μ m: +8–11%	0.4	+11%	25	EXP;FE
[137]	PM	DA BLT	μ m solder thickness	T_j 62.7 °C, IGBT (FE)	+0.8 °C per 25 μ m	n/a	n/a	n/a	FE
[17]	FC	WARP; TIM BLT	μ m BLT at corner (warpage-induced)	TIM impedance 6.25 $\times 10^{-6}$ m ² K/W at 24 μ m centre	24 to 97 μ m: 6.25 $\times 10^{-6}$ to 26.25 $\times 10^{-6}$ m ² K/W (radius of curvature 1514 m)	4.4	+320% (corner)	73	ANA
[46]	FC	WARP; TIM BLT	μ m corner warpage	θ_{jcp} , bare-die MCP mounted	unmounted (+15 μ m corner warpage): +17%	1.1	+17%	15	EXP;FE
[18]	FC	WARP; TIM BLT	°C die temperature (warpage-driven BLT)	θ_{jc} , lidded FCBGA TTV	up to 20% variation over 40–105 °C	0.3 %/°C	+20%	65	EXP;FE
[36]	FC	WARP	μ m die warpage	total resistance, centre cell, STCD bare die	36 μ m warpage: corner 1.8 $\times$ centre (100 μ m pad, after bonding)	n/a	+80% (corner)	36	EXP
[37]	FC	WARP	μ m die warpage	normalized temperature rise, centre cell, STCD	61 μ m warpage: corner 1.5–2 $\times$ centre	n/a	+50–100% (corner)	61	EXP;FE
[93]	FC	WARP; TIM BLT	μ m warpage (200 μ m diagonal)	cell R_{th} mean 14.38 K/W, 25 mm TTV	cell-to-cell sd 1.2 K/W (8.3%); range $\pm 16\%$	n/a	$\pm 16\%$ range	200	EXP
[94]	FC	WARP	mm lid non-coplanarity gap	package R 1.0 °C/W	0.25 mm gap: 1.0 to 1.1 °C/W	40 %/mm	+10%	0.25 mm	FE;CFD

TABLE III
(CONTINUED.) NORMALISED THERMAL SENSITIVITIES (ONE ROW PER STUDY $\times$ SOURCE; LOCAL VALUE AT THE STATED BASE, AND VALUE AT THE LARGEST VARIATION REPORTED)

Study	Pkg.	Source	Unit of variation	Base condition	Reported relation	Local sensitivity (% per unit)	At largest variation	Largest variation	Method
[91]	FC	WARP; TIM BLT	μm BLT non-uniformity (135/100/80)	chip centre temperature, FCBGA with sink (CFD)	+3 °C at centre	n/a	small	35	CFD
[31]	FC	WARP; TIM void	lid cavity shape (U vs W) + TIM lot	die temperature, HPC module 250 W	+1 °C average; > 2.5 °C at hot spots; 6/6 modules voided (2.0% area)	n/a	+2.5 °C	n/a	EXP
[35]	FC	TIM coverage	adhesive separation at chip centre	thermal resistance, 32 nm SOI TV (20 μm TIM)	power cycling 4500 cycles: > +45%; aging 1000 h: none	n/a	+45%	n/a	EXP
[7]	FC	TIM coverage	pct-point coverage (indium)	coverage, FCLGA indium TIM	> 90% to about 20% after 1000 cycles	n/a	−70 pts	1000 cycles	EXP
[33]	FC	TIM coverage	pct-point coverage	R_{jc} , 20 $\times$ 20 mm lidded TTV	coverage −6% average (−8% worst) after 1200 cycles correlates with R_{jc} degradation	n/a	qualitative	8	EXP
[97]	FC	TIM coverage	pct-point coverage	θ_{jc} / T_j , large FCBGA (CFD)	T_j reaches 125 °C at coverage 48–81% depending on size and die/package ratio	n/a	limit	50	CFD
[8]	FC	TIM coverage	pct-point coverage	thermal resistance, lidded FCBGA	sharp increase below 60% coverage (threshold adopted)	n/a	threshold	60	EXP
[91]	FC	TIM prop	$\text{cm}^2\text{K/W}$ contact resistance	chip temperature, FCBGA (CFD)	0.03 to 0.1 $\text{cm}^2\text{K/W}$: +15 °C centre, +15.5 °C corner	n/a	+15 °C	0.07	CFD
[56]	3D	TIM prop	factor on TIM k	θ_{max} 1.78 (normalized), 3D stack	$k \times 2.5$: −20%; $\times 5$: −28%; BMB layer $\times 5$: −2%	n/a	−28%	5 $\times$	FE
[58]	3D	TSV BEOL; BOND	TSV misalignment level; bump height 21–42 μm	logic-die temperature, HBM-type stack	temperature rises with misalignment; steeper for taller bumps	n/a	fig-read	n/a	FE
[54]	3D	BOND	SiO_2 thickness 200 vs 470 nm	fusion-bond TBR	0.2 vs 0.5 $\text{m}^2\text{K/MW}$	n/a	2.5 $\times$	270 nm	EXP
[9]	3D	BOND	Cu pad radius 5 μm vs blanket	Cu pad conductivity	160–220 W/(m·K), about 40% below blanket film	n/a	−40%	n/a	EXP
[95]	FC	WARP	μm convex lid deflection	θ_{jc} , 60 $\times$ 60 mm flip-chip package, 150 W (CFD)	0 to 120 μm convex: θ_{jc} about $\times 2$; 70 μm : +46% (0.105 °C/W limit)	0.7	+100%	120	CFD
[96]	2.5D	TIM BLT	μm HBM-to-logic die height difference	logic-die and interposer temperature, multi-die 2.5D/3D (FE)	+17% of temperature per 200 μm height difference	0.085 %/ μm (temperature)	+17%	200	FE

Pkg.: FC flip-chip, 2.5D interposer module, PM power module or discrete, LED, 3D stack; n/a: not reported in a form that allows the local value to be computed; n.s.: no significant effect reported; rows marked abstract-only in Supplementary Table S5b rest on the abstract alone.

be expected to scale inversely with the share of the interface in the total resistance. Position matters as much as area: voids nearest the heat source raise resistance by 19% more than voids far from it in the same package [76], a permitted local void size can be written as a function of position [74], voids under the chip centre dominate below 20% fraction and the position dependence vanishes above 30% [85], and through-thickness and die-side voids are worse than mid-layer and lid-side voids [86], although in a power package with a thin solder layer the void-style effect was below 3% of the temperature rise [76]. The one probabilistic TIM1 study shows why these two populations must be kept apart in a specification: a worst-case single centred void would force a 1% void requirement (12% resistance increase at 2%, 18% at 4%), whereas the same 4–7% void content, distributed, costs 4–10% on average and permits a 5–7% specification once an acceptable failure fraction is stated [32].

B. Bond line thickness

Where the TIM's bulk resistance dominates, thermal resistance is linear in BLT with slope $1/k$, and the studies

confirm this over 25–250 μm for greases (0.27–1.4 $\text{mm}^2\text{K/W}$ per μm for k of 0.7–3.8 W/mK [42]) and in variable-BLT tester methods [87]. Expressed relative to a package resistance, the sensitivity depends on the TIM's share: a parametric FC-BGA model with a 2 W/mK TIM gave a near-linear 10.5-fold increase of R_{jc} between 15 and 200 μm (about 5% per μm) but a weak dependence for k above 10 W/mK, with the sensitivity concentrated above 50 μm [14]; a polymer-TIM HFCBGA measured θ_{jc} within $\pm 10\%$ for a $\pm 20\%$ BLT deviation (0.5% per percent of nominal BLT) [88]; a warpage-driven corner BLT of 97 μm against 24 μm at the centre raised the local TIM impedance 4.2-fold [17]; and die tilt from 50 to 75 μm of die-attach bond line raised $R_{th,jc}$ of a power discrete by 8–11% [73]. Two studies temper the linear picture. Below about 50 μm the resistance of gel TIMs is dominated by contact resistance, so that the apparent conductivity falls as the bond line thins, and only above 50 μm does the effective conductivity become weakly dependent on BLT [46]; and for silver-flake epoxies the resistance-versus-thickness line can have a negative intercept because the filler redistributes as the bond line thins [89]; conversely, thick, low-compressibility pads can show lower average resistance with increasing thickness on a warped die

because the extra thickness buys coverage [36], and excess TIM volume beyond an optimum (55 μm effective) raises resistance again [90]. In the coupled warpage–thermal simulations of a lidded FCBGA the non-uniform BLT itself (135/100/80 μm) changed the chip-centre temperature by only 3 $^{\circ}\text{C}$, whereas a contact-resistance change from 0.03 to 0.1 $\text{cm}^2\text{K/W}$ added 15 $^{\circ}\text{C}$ [91]; the same ordering—void area first, then thickness, then assembly pressure, with void location and dispersion last—came from a standardised regression on a graphene-TIM sandwich [92].

C. Warpage and coplanarity

Warpage reaches the thermal path through two mechanisms that the newer test-vehicle studies have separated. The first is the BLT map: temperature-dependent warpage changed the measured θ_{JC} of a lidded FCBGA by up to 20% between 40 and 105 $^{\circ}\text{C}$, of which the silicon’s own conductivity change explained less than 30% [18]; mounting a bare-die package to a motherboard, which flattened its corners by 15 μm , lowered $\theta_{\text{J-cp}}$ by about 17% [46]; and frequency-domain impedance measurements at the die centre rose steeply between 40 and 70 $^{\circ}\text{C}$ as the centre BLT grew, with a hysteresis loop on a large die that signals TIM degradation [19]. The second is loss of contact at the corners when the TIM cannot follow the die: on a 16 mm bare die with 36–61 μm of warpage, the corner cells ran at about twice the temperature rise of the centre cells before bonding, at 1.5 times with a compliant graphite pad on the 60 μm die [37], and at 1.8 times after bonding a 100 μm pad whose compressible thickness (17 μm) was less than the 36 μm warpage, whereas 200 and 300 μm pads restored a uniform distribution [36]; on a 25 mm test chip with 200 μm of diagonal warpage the per-cell resistance had a standard deviation of 8% of the mean and a range of $\pm 16\%$ [93]; a lid non-coplanarity gap of 0.25 mm raised a package resistance from 1.0 to 1.1 $^{\circ}\text{C/W}$ [94]; and in a CFD study of a 60 mm flip-chip package, convex deflection of the heat spreader doubled θ_{JC} by 0.12 mm (about 0.7% per micrometre) while concave deflection improved it, from which a co-planarity tolerance of 0.07 mm was derived for a 5 $^{\circ}\text{C}$ junction-temperature allowance [95]. For 2.5D modules, one simulation study reports that the logic-die and interposer temperatures change by about 17% for every 200 μm of height difference between the HBM and the logic die, i.e. with the TIM1 gap that the stack-height tolerance creates (abstract-level) [96]. Both mechanisms are amplified when incoming parts vary within their specifications: a U-shaped rather than W-shaped lid cavity, combined with a high-viscosity TIM lot, raised the die temperature of a 250 W module by 1 $^{\circ}\text{C}$ on average and by more than 2.5 $^{\circ}\text{C}$ at the core hot spots [31]. The design levers that reduce the sensitivity are the same ones the mechanical literature identifies for warpage itself—thicker substrate cores, matched lid and die shapes [28], [29], mounting to a stiff board [46]—together with TIMs whose compressible thickness exceeds the warpage or whose adhesion survives it [36], [47].

D. TIM properties, coverage and degradation

The sensitivity to bulk conductivity saturates: raising a TIM from 2 to 30 W/mK reduced R-jc of an FC-BGA by 87% with diminishing returns beyond [14], and in a 3D stack a 2.5-fold TIM conductivity increase reduced peak temperature by about 20% while a 5-fold increase in a bonding-layer conductivity reduced it by 2% [56]. Coverage, by contrast, is a first-order variable: a CFD study of large FCBGAs found that the junction temperature reached its 125 $^{\circ}\text{C}$ limit at coverages between 48% and 81% depending on package size and die-to-package ratio [97], the literature threshold of 60% coverage for a sharp resistance rise has been adopted as a failure criterion [8], a 6–8% coverage loss after 1,200 cycles correlated with the thermal degradation of a lidded test vehicle while bulk conductivity did not [33], adhesive separation at the chip centre produced a 45% resistance rise [35], and spatially resolved transient measurements show that localised corner or mid-die degradation of TIM1 can trigger a 100 $^{\circ}\text{C}$ junction-temperature failure while the average resistance remains stable [15]. Degradation sensitivities are reported as functions of time, temperature and pressure rather than of a geometric source (Section IV-D).

E. Bonded interfaces, TSV and BEOL

For 3D stacks the only sensitivities are simulated: tier temperature rises with TSV misalignment and rises more steeply for taller micro-bumps [58]; the peak temperature of a multiscale stack model is far more sensitive to the TIM’s conductivity than to the conductivity of the bonding or BEOL layers [56]; and direct integration of a heat sink without a TIM was predicted to halve θ_{JA} once the low BEOL conductivities were included [59]. No measured tier-temperature sensitivity to a bonded-interface property or defect exists in the set.

F. Appraisal

Supplementary Table S5 gives the four-item appraisal of the 142 extracted studies. The variation magnitude is measured rather than assumed in 106 of them, the exceptions being the probabilistic studies that assume input standard deviations and the parametric simulations; the thermal result is a measurement, or a model validated against one, in 111; a base condition and units sufficient for normalisation are present in the 41 studies that supply the 44 rows of Table III, and absent in the remainder, most often because the base resistance is normalised to an undisclosed target or the result is shown only graphically; and sample size, spread, uncertainty or confidence is reported in 81 studies, but distribution parameters that describe unit-to-unit variation—rather than a measurement uncertainty—in only 34, of which 16 concern a core package. The sensitivities in Fig. 4 should therefore be read as an inventory of single-condition results from which order-of-magnitude comparisons can be drawn, not as a meta-analytic estimate.

VI. METROLOGY CAPABILITY (RQ3)

Table IV collects the metrology capabilities reported by the included studies, grouped by the feature they resolve. Three observations organise the section: the geometric metrology is

TABLE IV
METROLOGY CAPABILITY REPORTED BY THE INCLUDED STUDIES

Feature	Method	Reported capability	Non-destructive	Studies
TIM / die-attach voids, coverage	C-mode scanning acoustic microscopy (C-SAM, SAT, T-SAM)	x-y resolution $\approx 40 \mu\text{m}$ (macro voids $> 50 \mu\text{m}$); $20 \mu\text{m}$; $5 \mu\text{m}$ at 230 MHz; through 3.2 mm lid at 50 MHz; area only (no depth)	Yes	[8], [31], [82], [98]
TIM void depth	Quantitative broadband acoustic microscopy (Q-BAM)	Void depth from cross-sectional slices, verified vs SEM	Yes	[99]
Void metric variation	Unified image-processing software for C-SAM / X-ray laminography	Large analyst- and system-dependent spread of void % on one MCM; spread reduced by common software	—	[100]
Voids, die attach and solder	2-D X-ray, X-ray laminography, 3-D CT / XRM	More sensitive than SAM for initial voids; CT $10 \mu\text{m}$ (3-D), XRM $4.4 \mu\text{m}$; blob analysis for size distributions; hours per 3-D scan; poor contrast for polymer TIM; cannot separate lid- from die-side voids	Yes	[6], [61], [62], [82], [99], [101]
Voids, delamination, cracks (thermal signature)	Pulse / lock-in infrared thermography	$130 \mu\text{m}$ voids under a $200 \mu\text{m}$ die; delaminations in stacked-die QFN after 30–200 periods; noise floor to $10 \mu\text{K}$ cited; distinguishes voided from micro-cracked lidded units where C-SAM cannot	Yes	[102]–[104]
Voids (transient detection)	Microsecond current-injection transient impedance	3% of die area detectable (vs 15% for classical cooldown methods); 2°C mean-temperature change resolvable	Yes	[83]
Bond line thickness	Cross-section (reference); acoustic A-scan / AMI; minimum-entropy deconvolution of echoes	Subtractive method misleading vs cross-section; A-scan max error $8 \mu\text{m}$ (25 MHz, 25 mm focal length) vs $22 \mu\text{m}$ (15 MHz); AMI 15 min vs 10.5 h destructive, 72% valid points; TON-MED $87.6 \pm 0.56 \mu\text{m}$, $< 2\%$ error at 10 dB SNR	Yes	[88], [101], [105], [106]
Bond line during reflow	In-situ laser profilometry; BLT reconstruction from lid topology + modelled warpage	$1 \mu\text{m}$ resolution; BLT map	Yes	[4], [5]
Die-attach BLT, tilt, warpage (in-line)	Dual confocal chromatic profilometry	Repeatability $\approx 1 \mu\text{m}$ (12 scans); accuracy $2\text{--}3 \mu\text{m}$; BLT/tilt/warpage contour maps	Yes	[138]
Warpage	Shadow moiré; digital image correlation; stylus / laser profilometry; precision-pin laser profilometry for in-situ TIM2 thickness	$2.5 \mu\text{m}$ (100 LPI grating), repeatable through $25\text{--}260\text{--}25^\circ\text{C}$; DIC to 125°C ; laser z-resolution $\pm 0.1 \mu\text{m}$; $\pm 1 \mu\text{m}$ with $\text{sd} \approx 1 \mu\text{m}$; JEDEC/JEITA require ≥ 3 samples (extremes not bounded)	Yes	[22], [23], [37], [48], [49], [139]
Die warpage inside a package	X-ray diffraction imaging (topography)	Relative tilt precision $\approx 0.004^\circ$; lab source divergence 0.2° limits range; in-situ to 200°C	Yes	[107]
Wafer nanotopography and local warp	Dual-Fizeau patterned-wafer-geometry interferometry	Sub-nm flatness precision; site-level 3σ NT and local warp	Yes	[51]
TIM property (coupon)	ASTM D5470-type steady-state testers; guarded heat flow; heat-meter bar with uncertainty analysis	Reproducibility $0.03^\circ\text{C}\cdot\text{cm}^2/\text{W}$ (95% CL); 1σ $0.0008^\circ\text{C}/\text{W}$, 4% total uncertainty with $5 \mu\text{m}$ flatness; resolution $0.03 \text{ cm}^2/\text{K}/\text{W}$ at 10% uncertainty; probe-position uncertainty raises error from 8% to 39% at $10^{-6} \text{ m}^2/\text{K}/\text{W}$; ASTM vs regression reductions differ $\approx 10\times$ for Cu–In	Coupon	[39], [80], [108], [109]
TIM property (coupon)	Laser flash, transient plane source, DynTIM	$\approx 25\%$ uncertainty on composite samples; thickness error dominates until $\pm 0.5 \mu\text{m}$ gauge used; resistances below vendor D5470 values	Coupon	[84], [110]
TIM property, spatially resolved	Phase-sensitive / frequency-domain thermoreflectance	Separates bulk k and contact resistance ($\approx 17\%$ uncertainty); k map at $10 \mu\text{m}$ ($3 \mu\text{m}$ spot); Cu-pad k with FEA fitting; fusion-bond TBR with phase imaging of defects	Yes (surface)	[9], [39], [40], [54]
BEOL / interconnect stacks	Layer-by-layer TDTR and SSSTR mapping	$\approx 10 \mu\text{m}$ step; cumulative R_{th} of stacks	Yes (surface)	[59]
Package θ_{JC} and layer resistances	JESD51-14 transient dual-interface, structure functions	θ_{JC} repeatability $\approx 0.01 \text{ K}/\text{W}$; separates die attach from downstream layers; ≥ 10 samples/decade needed; 1-D assumption fails for laterally heterogeneous stacks; TSP biased by hot spots above $\approx 15\%$ voids; SF metrics (area, DTW) for defect detection	Yes	[61], [65], [67], [111], [112]
Spatially resolved TIM1 resistance	Thermal test vehicles with sensor arrays ($R_{\text{th}}(x,y)$); STCD chip with $36 \mu\text{m}$ sensors; frequency-domain impedance	Location-dependent TIM1 R_{th} at 500-cycle intervals; cell resistance $\text{sd } 1.2 \text{ K}/\text{W}$ of $14.4 \text{ K}/\text{W}$; 0.015 K resolution, 0.085 K accuracy; corner/centre resolution; in-situ warpage–BLT effects vs temperature	Yes	[15], [18], [19], [36], [37], [93]
Thin die-attach bond lines	Transient heat-flux impedance (thermal test chip on diode)	$8\text{--}98 \mu\text{m}$ bond lines; $\pm 0.005 \text{ K}/\text{W}$ instrument floor; $\pm 0.015 \text{ K}/\text{W}$ from silicon k uncertainty	Yes	[113]
Buried bonded interfaces	Periodic-heating IR concepts; ML inversion of surface transients; movable transient probe (substrates)	Feasibility for $0.001\text{--}0.01 \text{ cm}^2/\text{K}/\text{W}$ a few hundred μm deep; $\approx 4\%$ localisation error and $< 10\%$ ITC error in simulation; 2-D map with $\text{sd } 3.5\text{--}6.8\%$, defects $> 2 \times 2 \text{ mm}^2$	Yes (proposed)	[112], [114], [115]
TSV integrity	Thermal test key on 300 mm wafers	Detects seams/voids via ΔR of traces before thinning	Yes	[60]

far more mature than the thermal metrology at the length scale that matters; the non-destructive geometric methods measure area, not the depth or the thermal weight of a defect; and the transient thermal methods that do resolve individual interfaces are only now being made spatially resolved.

A. Voids, coverage and delamination

Scanning acoustic microscopy (C-SAM, SAT) is the reference method for TIM and die-attach coverage in every production-oriented study in the set. Its lateral resolution depends on frequency and on the lid or die through which it images: about 40 μm for the 2004 study that correlated controlled voiding with in-situ resistance [98], 20 μm for a 2021 IGBT failure analysis [82], 5 μm at 230 MHz on lidded FCBGA test groups [8], and coarser through a 3.2 mm lid at 50 MHz, where a 2025 HPC-module study nonetheless resolved a 2.0% mean voided area [31]. Two limitations recur. First, a C-scan integrates over the bond line and gives an area, not a volume or a depth; quantitative broadband acoustic microscopy (Q-BAM) was proposed in 2024 to recover void depth in indium TIM and verified against SEM cross-sections [99], and X-ray cannot distinguish lid-side from die-side voids [99]. Second, the operator- and system-dependence of void quantification is large enough that a 2023 study introduced unified image-processing software specifically to reduce analyst and system variation [100]; the gauge repeatability of the void metric itself is otherwise unreported in the set. Two-dimensional X-ray is more sensitive than SAM for initial voids in LED solder joints [61] and, with blob analysis, supports size distributions [6]; three-dimensional X-ray tomography resolves voids at 10 μm [82] and 4.4 μm [62] but scans take hours [99], and X-ray contrast fails for polymer TIMs between silicon and copper [101]. Infrared and lock-in thermography detect voids and delaminations by their thermal signature—130 μm voids under a 200 μm die [102], delaminations in a stacked-die QFN after 30 to 200 excitation periods [103], voided and micro-cracked lidded units that C-SAM could not separate [104]—which is the only class of method in the set that measures the thermal consequence of the defect directly rather than its geometry.

B. Bond line thickness and warpage

Destructive cross-sectioning remains the reference for BLT, and one study notes that the subtractive (stack-height) method often misleads relative to cross-section [88]. Non-destructive BLT is obtained acoustically: acoustic micro-imaging of lid-TIM and TIM-die interfaces [105], A-scan thickness measurement with a correctly chosen probe focal length (maximum error 8 μm at 25 MHz versus 22 μm at 15 MHz) [106], and minimum-entropy deconvolution of overlapping echoes, which gave a BLT of $87.6 \pm 0.56 \mu\text{m}$ on a Si-TIM-Cu structure with less than 2% error at 10 dB signal-to-noise ratio [101]. In-situ BLT during reflow has been measured with a laser profilometer of 1 μm resolution [5], and BLT maps have been reconstructed from lid-surface topology and modelled chip warpage [4]. Warpage itself is measured by shadow moiré (2.5 μm resolution with a 100 lines-per-inch grating, repeatable

through a 25–260–25 $^{\circ}\text{C}$ cycle [48]), digital image correlation on chiplet surfaces to 125 $^{\circ}\text{C}$ [23], stylus profilometry along the die diagonal [37], and, for encapsulated die, X-ray diffraction imaging with a relative tilt precision of about 0.004° [107]. The JEDEC and JEITA warpage standards require as few as three samples, which several authors note cannot bound the extreme values that drive yield [48], [49].

C. Thermal resistance of interfaces and layers

Steady-state testers descended from ASTM D5470 dominate TIM property data. Their reported capability ranges from a reproducibility of 0.03 $^{\circ}\text{C}\cdot\text{cm}^2/\text{W}$ at 95% confidence for a package-level screening tester (abstract-level value) [108] and a one-sigma repeatability of 0.0008 $^{\circ}\text{C}/\text{W}$ with a 4% total uncertainty for a guarded heat-flow system with 5 μm flatness control [80], to a maximum resolution of 0.03 $\text{cm}^2\text{K}/\text{W}$ with 10% uncertainty for improved D5470 facilities cited in [39]. A dedicated uncertainty analysis of heat-meter-bar testers showed that the position uncertainty of the thermal probes (20–100 μm) dominates: at an interfacial resistance of $1 \times 10^{-6} \text{ m}^2\text{K}/\text{W}$ the uncertainty rises from 8% to 39% when a 100 μm location uncertainty is included, and the ASTM and linear-regression reductions differ by nearly an order of magnitude for a copper-indium interface [109]. Laser-flash characterisation of composite TIM samples carried an uncertainty of about 25% [84], and a comparison of LaserFlash, transient plane source and DynTIM testers found that the sample-thickness error dominates all three until a $\pm 0.5 \mu\text{m}$ length gauge is used [110]. Measured TIM resistances are frequently lower than those calculated from vendor conductivities [84] and interface-inclusive effective conductivities back-calculated from θ_{JC} , coverage and BLT on a 77.5 mm test vehicle were about 40% below the vendor values for silicone and graphite TIMs [38].

Transient methods resolve individual layers. The JESD51-14 transient dual-interface method with structure functions gave θ_{JC} with about 0.01 K/W repeatability on TO-247 IGBTs and separated die-attach from downstream layers [65]; applied to 1,800 LEDs it separated package from solder-and-substrate resistance [61]. Its limits are documented: fewer than 10 samples per decade or a late start of the transient distort the structure function [111]; the one-dimensional heat-flow assumption fails for laterally heterogeneous hybrid-bonded stacks [112]; and voids under the die bias the temperature-sensitive-parameter reading itself once hot spots form, at roughly 15% voided area, so that a void-dependent correction to the cooldown method was proposed [67]. Spatially resolved transient characterisation is the most significant recent development: thermal test vehicles with sensor arrays report a location-dependent TIM1 resistance $R_{\text{th}}(x,y)$ at 500-cycle intervals, resolving corner or mid-die degradation that the average resistance hides [15], [93], and a test chip with 36 μm sensors resolved a $1.5\text{--}2\times$ corner-to-centre difference under a 36–61 μm warped die [36], [37]. Thin bond lines below the resolution of these methods are addressed by phase-sensitive transient thermorefectance, which separates bulk conductivity from contact resistance with about 17% uncertainty [40]; by frequency-domain thermorefectance mapping at 10 μm , which gave a conductivity map of a gap

TABLE V
STATISTICAL TREATMENTS AND SPECIFICATIONS BY METHOD

Treatment	Package	What was varied	Inputs measured or assumed	Studies
Orthogonal arrays / RSM (nominal optimisation)	FCLGA, FCBGA, generic assembly (abstract-level), TO-247, RF power	Lid, TIM, adhesive, chip and solder dimensions; TIM and chip thickness; void size, number and spacing; heat-sink unflatness	Design levels	[7], [53], [116]–[119]
Process DOE with statistical comparison	Indium TIM1, polymer TIM1, solder TIM1	Reflow and flux conditions; aging time, temperature and load; process parameters vs void content	Measured	[24], [44], [120]
DOE + RSM + Monte Carlo	Power package	Solder thickness $\pm 20\%$, defect rate 5%, grease thickness $\pm 50\%$	Assumed	[121]
2 $\times$ 2 lot experiment	HPC module	Lid cavity shape $\times$ TIM lot	Measured (lot data)	[31]
Monte Carlo on interfacial void distribution	Flip-chip TIM1	Areal void content 1–7%, 3,000 samples; ACPL/AFL specification	Assumed (uniform areal)	[32]
Monte Carlo with random void generation	IGBT, LED	Void radius, position, count from measured (log-normal) statistics	Measured	[62], [70], [71], [79], [140]
Polynomial chaos / stochastic compact model	Generic package	Material and geometric parameters	Assumed	[122]
Stochastic FEM / FORM–SORM / Sobol' / RBDO	LED, BGA	Layer conductivities and thicknesses (5–10% sd)	Assumed	[123], [124], [141]
Multiscale sensitivity (power-law fits)	3D stack	Layer conductivities; tile-wise sd of bonding/BEOL conductivity	Computed	[56]
Machine-learning surrogates†	NAND package, FCBGA TIM1, hybrid bond, IGBT	Warpage yield at 38 μm limit from manufacturing sd; SVR of coverage vs cycles; ML inversion of ITC; void-feature regression	Measured (spec sd; coverage data; CT voids) / simulated	[8], [71], [79], [112], [125]
Standardised regression ranking	FCBGA TIM1 sandwich	Void area, TIM1 thickness, assembly pressure, void location and dispersion	Design levels (validated on FCBGA)	[92]
Distribution fitting	Indium TIM1; thinned wafer	Log-normal void diameter and fraction vs lid roughness and pressure; Weibull plots of wafer thickness	Measured	[6], [52]
Process capability / SPC / gauge studies†	LED, HPC module, FCBGA, TIM testers	Solder-coverage Cpk 1.9–4.1; lid-flatness and TIM-viscosity lot data; control charts of ψ_{JC} measurement repeatability; analyst/system variation of void %; 95% CL tester reproducibility	Measured	[18], [31], [63], [100], [108]
Degradation-model fitting†	FCBGA TIM2, greases	Saturation model with Arrhenius scaling; regression vs BLT	Measured	[42], [45]
Specification stated or checked against a thermal rating	Large-die FCBGA; FCCSP; thin-core FCBGA; hybrid bonding	Coverage $\geq 95\%$, BLT 30–45 μm and JEDEC warpage window checked by simulation against the rated die temperature; JEDEC warpage limits; warpage targets; particle-screening size from a permitted void size	Measured	[50], [57], [126], [142]
Specification derived from a thermal requirement	Flip-chip TIM1; IGBT die attach; large FCBGA (two studies); power package	Probabilistic 5–7% void limit from an R_{jc} limit and accepted failure fraction; location-dependent permitted void size; coverage at which $T_j = 125^\circ\text{C}$; heat-spreader co-planarity tolerance (0.07 mm) from a 5°C junction-temperature allowance; 95th-percentile fin design	Assumed (void distribution) / —	[32], [74], [95], [97], [121]

†Rows that also list treatments coded as metrology (C) or thermal-effect (B) evidence rather than type D under the definition of Section II-E: the tester reproducibility of [108], the ML metrology inversion of [112], and the regression fits of [42], [45].

filler with a standard deviation of 15% of the mean [39] and revealed a 40% conductivity deficit in 5 μm hybrid-bonding pads [9]; by layer-by-layer TDTR and SSTR mapping of BEOL stacks [59]; and by a transient heat-flux-impedance method between a thermal test chip and a diode that resolved die-attach bond lines of 8–98 μm with a ± 0.005 K/W instrument floor [113]. For interfaces buried a few hundred micrometres below the surface of a bonded stack, only feasibility studies exist—periodic infrared heating concepts for resistances of 0.001–0.01 $\text{cm}^2\text{K/W}$ [114] and simulation-trained machine-learning inversion for hybrid-bond conductance [112]—and the two-dimensional mapping of a bonded interface with a moving transient probe has been shown on power substrates rather than on dies [115].

VII. STATISTICAL TREATMENT AND SPECIFICATION PRACTICE (RQ4)

Only 72 of the 388 synthesised studies apply a statistical method to a variation source or to its thermal effect, or state a specification for the source (type D), and 43 of the 72 are in the adjacent set. Table V lists the treatments by method. Four groups can be distinguished.

A. Designed experiments and response surfaces

Designed experiments are the most common statistical device, but almost always in the service of nominal design or process development rather than of variation. Orthogonal-array and response-surface studies have optimised lid, TIM and adhesive parameters against TIM plastic strain in an indium-TIM FCLGA [7], correlated lid–substrate warpage mismatch

with metal-TIM creep strain through Spearman coefficients ($\rho = 0.59$ in the die area) [116], minimised the thermal resistance of a generic assembly over heat-sink base, TIM and chip thickness with a 15-run central composite design (abstract-level) [117], ranked the size, number and spacing of indium-TIM1 voids by their effect on junction temperature through an L9 Taguchi array with analysis of variance [118], and reduced the junction-to-case resistance of a TO-247 MOSFET by 33% with a quadratic response surface of chip, solder and frame dimensions ($R^2 = 0.994$) [119]. On the process side, designed experiments with statistical comparison of means have been used to select fluxless indium TIM1 reflow conditions [24], to identify the factors that trigger polymer-TIM degradation under aging [44], and, in an early solder-TIM study, to reduce solder-TIM void content while noting that the die-to-heat-spreader resistance depended on the location as well as the amount of voiding (abstract-level) [120]. The early study by Yokono et al. is the exception that treats the design variables as random: solder thickness ($\pm 20\%$), defect rate (5%) and grease thickness ($\pm 50\%$) were sampled through L9 and L18 arrays, a response surface was fitted, and Monte Carlo propagation showed the chip-to-ambient resistance spanning 0.2–0.8 K/W at one cooling condition and 0.6–1.2 K/W at another, so that a 1.0 K/W requirement could only be met at the 95th percentile by redesigning the fins [121]. A 2010 RF power-package study used orthogonal main effects to rank heat-sink unflatness parameters and found that a thin ($< 50 \mu\text{m}$) die tolerates a single central void of only 0.28% of the die area before its resistance falls to that of a thick die [53]. A 2×2 lot experiment on an HPC module showed that a U-shaped lid cavity combined with a high-viscosity, high-modulus TIM lot—both within incoming specification—voided 6 of 6 modules and raised hot-spot temperatures by more than 2.5°C [31], which is the clearest demonstration in the set that specification limits set without a thermal model do not bound the thermal outcome.

B. Probabilistic propagation

Monte Carlo, polynomial-chaos and reliability methods have been applied to package thermal problems in a handful of studies, mostly on LED or generic packages. A stochastic compact thermal model built on polynomial chaos expansion produced mean and standard-deviation fields of the temperature rise and the time evolution of its probability density [122]. Sobol' global sensitivity and first/second-order reliability methods applied to a multi-chip LED package with 5% standard deviations assumed on 28 parameters gave a probability of exceeding 120°C of 20.7% (20.4% by Monte Carlo with 4,000 samples), which reliability-based design optimisation reduced to 9% [123], [124]; the standard deviations were assumed, not measured. Random-void finite-element models seeded from measured void statistics (5,119 voids over 70 assemblies, mean radius 0.08 mm, standard deviation 0.11 mm) were used to relate junction temperature z-scores to void fraction, number and distance from the heat source [62]. In 3D stacks, a physics-informed multiscale model computed the tile-to-tile standard deviation of the effective conductivity of BEOL and hybrid-bonding layers and fitted power-law sensitivities of the peak

temperature to each layer's conductivity [56], and a neural-network surrogate of a NAND package predicted a 98% pass probability against a $38 \mu\text{m}$ warpage limit from manufacturing standard deviations, with the five leading parameters, headed by EMC thickness and substrate CTE, explaining over 67% of the variance [125].

C. Statistical process control, gauge studies and lot data

Process-capability and gauge treatments are rare. Solder-coverage Cpk values of 1.9–4.1 and void-diameter distributions were reported for three automotive LED types, with correlation tests showing no significant thermal effect within the 25% IPC void limit [63]; log-normal void-diameter distributions were fitted to indium TIM1 under different lid roughness and process pressures [6]; wafer-thickness distributions after extreme thinning were presented as Weibull plots [52]; lid-cavity flatness lot averages of 17–23 μm over $12 \text{ lids} \times 24 \text{ cavities}$ and TIM viscosity across more than 190 material lots were tabulated in the HPC-module study [31]; a support-vector regression of TIM1 coverage against temperature, chip size, pressure and cycle count predicted device-level coverage within 5% [8]; and the repeatability of a package-level TIM tester was stated at the 95% confidence level [108]. Measurement-system variation of the void metric was addressed once [100], and of the interface-resistance metric twice [109], [110].

D. Specifications and thresholds

The specification limits that appear in the set are geometric and were not derived from thermal models. MIL-STD-883 method 2030 limits total die-attach voiding to 50% of the joint area and a single void to 15% [76]; IPC-A-610 and J-STD-001 limit BGA-type voiding to 25% [63]; industry practice for power-module die attach is 5–10% [74]; a 5% limit on TIM voided area was applied to an HPC module [31] and a 10% initial void rate is considered controllable for indium TIM [34]; a TIM1 coverage of 60% has been adopted as the delamination-failure threshold [8], and one CFD study derived the coverage at which a 125°C limit is reached for each package size and die-to-package ratio (48–81%) [97]; JEDEC JEP95 SPP-024 sets 100 μm as the reflow-temperature warpage limit for a 14 mm FCCSP [50]; acceptance criteria of at least 95% TIM1 coverage, a 30–45 μm bond line and package warpage within the JEDEC window were set for large-die packages and checked against the rated die temperature by simulation [126]; a particle-screening criterion (46 μm) was derived from a permitted hybrid-bond void size through a fitted particle-to-void relation [57]; and a thin-die RF package was shown to require voids below 0.3% of the die area under the heat path [53]. Only five studies in the set turn a thermal requirement into a permitted variation: the probabilistic 5–7% void specification for flip-chip TIM1 derived from an R_{jc} limit and an accepted failure fraction [32], the location-dependent permitted void size of Ottinger et al. [74], the coverage limits of [97], the heat-spreader co-planarity tolerance of 0.07 mm derived from a 5°C junction-temperature limit for a 60 mm flip-chip package, at which θ_{JC} reaches 0.105°C/W and beyond which it doubles by 0.12 mm of convex deflection [95], and

TABLE VI
GAP MAP: CORE CELLS (FLIP-CHIP, 2.5D, 3D) WITH NO, FEW OR ONLY INDIRECT QUANTITATIVE EVIDENCE

Source	Cell	Core studies	What exists	What is missing
Die thickness / TTV	Thermal effect; statistics/spec	0; 1	Thickness distributions and TTV after extreme thinning, without a thermal metric [52]; die-thickness effect on warpage of a two-die stack, without a thermal metric [143]; outside the core set, thin-die void tolerance in an RF power package [53]	Any measured or simulated tier/die temperature sensitivity to die-thickness variation in a stacked package
Bonded interfaces	Thermal effect	6 (5 simulated; 1 measured, abstract-level)	Simulated effects of interfacial pores [55], of misalignment and bump height [58], of layer-conductivity spread [56], of interlayer phonon transmittance [127] and of non-conductive-film placement [128]; laser-flash interfacial resistances of a four-die stack [129]; outside the cell: fusion-bond TBR values [54], Cu-pad conductivity deficit [9], wafer-level void predictors [51], particle-to-void relation [57]	Measured distribution of bond-interface conductance across a wafer or across dies, propagated to a tier temperature
TSV / BEOL	Thermal effect; statistics/spec	5 (4 simulated); 1 (simulated)	Tile-wise sd and power-law sensitivities [56]; simulated TSV misalignment [58] and filling defects [130]; simulated void signature of a measured wafer-level TSV thermal test key [60]; laser-flash interfaces of a through-via stack [129]; outside the cell: layer-by-layer BEOL conductivity maps [59]	Unit-to-unit variation with a thermal effect; any specification
2.5D interposer modules	All	8 studies in total	TIM2 coverage/pressure, warpage-driven TIM2 BLT, coverage and BLT on a 77.5 mm vehicle, liquid-metal coverage, interposer warpage metrology, fan-out bridge warpage, TIM contact model, stack-height sensitivity (17% per 200 μm , abstract-level) [23], [38], [41], [96], [131]–[134]	Interposer-to-die micro-bump and underfill variation with a thermal outcome; any measured distribution
TIM coverage / delamination	Statistics/spec	5	Coverage limits from a T_j target [97]; acceptance criteria [126]; 60% delamination threshold and SVR coverage model [8]; 10% void-rate limit for indium TIM [34]; RSM on coverage-loss drivers [7]	Gauge repeatability of the coverage metric; coverage distribution across units
TIM bond line	Statistics/spec	8	Co-planarity tolerance derived from a 5 $^{\circ}\text{C}$ limit [95]; RSM over TIM and chip thickness (abstract-level) [117]; RSM and Spearman studies of lid, TIM and adhesive parameters [7], [116]; DOE on reflow conditions [24]; standardised regression of thickness effect [92]; BLT acceptance criteria [126]; control charts of ψ_{JC} measurement [18]; outside the cell: one sd across units [16] and a $\pm 20\%$ tolerance vs θ_{JC} [88]	Measured BLT distribution paired with measured θ_{JC} distribution on the same units
TIM voids	Statistics/spec	12	Monte Carlo specification [32]; log-normal fits [6]; Taguchi ranking of void geometry [118]; process DOEs [24], [120]; 2 $\times$ 2 lot experiment [31]; gauge study of the void metric [100]; standardised regression [92]; stated limits [34], [126], [142]	Gauge R&R of the void metric in more than one study; void distribution paired with θ_{JC} distribution
TIM property / degradation	Statistics/spec	3	DOE on degradation factors [44]; lot rheology data [31]; tile-wise conductivity spread in a 3D stack [56]; outside the cell: degradation fits reported as mean + 2.3 σ [45]	Lot-to-lot in-situ conductivity or contact-resistance distribution
Warpage / coplanarity	Statistics/spec	12	Co-planarity tolerance derived from a 5 $^{\circ}\text{C}$ limit [95]; JEDEC limits [50], [126]; warpage targets [142]; RSM and Spearman correlation of warpage-driven strain [7], [116]; lot experiment [31]; control charts under temperature-dependent warpage [18]; wafer nanotopography 3 σ metrics [51]; substrate-deflection limit for indium wetting [24]; outside the core set: material-scatter bounds [49]	Warpage distribution across units propagated to a θ_{JC} distribution
All core sources	Specification derived from a thermal requirement	3	Probabilistic void limit from an R_{jc} limit [32]; coverage limits from a T_j target [97]; heat-spreader co-planarity tolerance from a 5 $^{\circ}\text{C}$ allowance [95]	Void, BLT or warpage limits derived from a thermal requirement and a measured distribution with a gauge study

the 95th-percentile fin design of [121]. Three of them address a flip-chip package [32], [95], [97], and only the first does so at the unit-distribution level, with an assumed rather than a measured void distribution; none addresses a 2.5D or 3D package.

VIII. GAP MAP AND RESEARCH AGENDA (RQ5)

Fig. 2 and Table VI locate the gaps. Reading the core panel of the coverage matrix cell by cell, the evidence is concentrated in three places—the thermal effect of TIM properties, the magnitude of TIM voids, and the thermal effect of TIM bond line and warpage—and is thin or absent almost everywhere else. The following cells contain no quantitative study of a

flip-chip, 2.5D or 3D package, only a few, or only indirect evidence.

Die thickness and total thickness variation. No included study quantifies the thermal effect of die-thickness variation on an advanced package, although wafer thinning to below 50 μm is standard for stacked memory and the die is the primary lateral spreader for hot spots. The core studies that report thickness variation do so as a process outcome—for extreme thinning to 5 μm , wafer-thickness distributions presented as Weibull plots, with the uniformity at the wafer edge degrading once more than about 20 μm is removed by CMP—without a thermal metric [52]; the only die-thickness-to-thermal link in the set is the RF power-package study, which showed that a thin die tolerates a central void of only 0.28% of its area [53].

Bonded interfaces in 3D stacks. Ten core studies report metrology for hybrid, micro-bump or fusion-bonded interfaces and ten report magnitudes—void distributions correlated with pre-bond nanotopography and local warp [51], void size against particle size [57], a 40% conductivity deficit in damascene pads [9], fusion-bond thermal boundary resistances of 0.2 and 0.5 m²K/MW [54]—but only six report a thermal sensitivity at the interface or stack level: simulations of interfacial pores [55], misalignment and bump height [58], layer-conductivity spread [56], non-Fourier transport across HBM interlayers, where the phonon transmittance changes the junction temperature by up to 56.6 °C (abstract-level) [127], and non-conductive-film placement [128], together with a 2001 laser-flash characterisation of the interfaces of a four-die stack with copper through-vias (abstract-level) [129]. No study measures the distribution of bond-interface thermal conductance across a wafer or across dies and propagates it to a tier temperature. Non-destructive metrology of buried bond interfaces exists only as feasibility studies [112], [114].

TSV and BEOL stacks. The effective conductivity of BEOL stacks has been mapped layer by layer [59] and computed tile by tile [56], TSV misalignment and bump-height effects on tier temperature [58] and the temperature signature of TSV filling defects [130] have been simulated, and a wafer-level thermal test key has been built for which simulation places the signature of a 20% void in a blind TSV at a 1.2–2.0 °C/W change of a measured trace resistance difference [60], but no study reports the unit-to-unit or wafer-level variation of these quantities together with a thermal effect, and none reports a specification.

2.5D interposer modules. Only eight synthesised studies concern 2.5D packages, and they address TIM2 coverage under a large heat sink [41], warpage-driven BLT of TIM2 [23], TIM coverage and BLT on a 77.5 mm test vehicle [38], liquid-metal TIM coverage on a 50 mm package [131], synchrotron X-ray warpage metrology of a silicon interposer [132], the warpage of a bridge-type fan-out module [133], a contact model for the interfacial resistance of TIMs on a chiplet package [134], and the stack-height sensitivity of a multi-die module, in which the logic-die temperature changes by about 17% per 200 µm of HBM-to-logic height difference [96]. The interposer-to-die micro-bump layer and the underfill between them do not appear as variation sources with a thermal outcome in any included study.

Unit-level distributions for flip-chip TIM1. Although 67 core studies treat TIM bond line and 46 treat TIM voids, only a handful report a distribution across units rather than a single or a nominal value: a BLT standard deviation of about 20% on a 65 mm test vehicle [16], a shim-controlled 97 ± 4 µm [15], a specification of 50 ± 20 µm with more than 90% coverage [14], lot averages of lid flatness [31], and the log-normal void-size fits for indium TIM1 [6]. No study reports a measured BLT or void distribution together with the measured θ_{JC} distribution of the same units.

Statistical treatment and specifications in the core set. A statistical treatment or a specification (type D) appears in 29 core studies, but most are designed experiments for nominal design or process development, specification statements quoted

from standards, or probabilistic models with assumed inputs; only the probabilistic void specification of [32], the coverage limits of [97] and the heat-spreader co-planarity tolerance of [95] were derived from a thermal requirement for an advanced package. Gauge repeatability of the void, coverage and BLT metrics—the quantities that the specifications are written on—is reported once [100].

Adjacent evidence that does not transfer directly. The die-attach void literature is the richest cell in the matrix (82 thermal-effect studies), but its base conditions—a solder layer of 25–100 µm under a power die on a copper lead frame or DBC, with the die-attach contributing about 15% of the module resistance [83]—differ from a TIM1 under a large logic die with a lid, where the TIM is 30–50% of the junction-to-case budget [84] and the void-to-hot-spot proximity is set by a power map rather than by a uniformly heated die. The exponential dependence on the largest void [65], [75], [77] and the position dependence [74], [76] are the transferable findings; the numerical sensitivities are not.

Research agenda

Five studies would close the largest gaps at modest cost. (1) A unit-level dataset on one lidded flip-chip test vehicle reporting, for each unit, the BLT map (acoustic or profilometric), the void and coverage map (C-SAM with a stated gauge repeatability), the lid and die warpage, and the measured θ_{JC} , so that the spread-weighted sensitivities of Table III can be estimated from data rather than assembled from single-condition studies. (2) The same for a hybrid-bonded two-tier stack, with the interfacial conductance of the bond layer mapped by a thermorefectance or ML-inversion method and the tier temperature difference measured on a thermal test chip. (3) A die-thickness study on a stacked-memory-like vehicle, since the cell is empty. (4) A reporting standard for variation data in package-thermal papers—base condition, units, sample size, spread and metrology uncertainty—without which normalisation across studies remains partly a matter of reading values off figures, as fourteen rows of the extraction table had to (Supplementary Table S4). (5) Derivation of at least one geometric specification (a void limit, a coverage limit or a BLT tolerance) from a thermal requirement and a measured distribution, with a gauge study of the metric, following the pattern of [74], [97] and [95] but with a measured distribution and for a 3D logic package.

IX. LIMITATIONS OF THE REVIEW

The review has six limitations that the reader should weigh. First, the systematic search used a single index (OpenAlex), every sub-query was capped at its 3,000 most relevant records, and the citation chasing resolved only references that carry a DOI; although OpenAlex covers the IEEE, Elsevier, ASME, IMAPS, Springer and MDPI venues in which this literature appears, records with no abstract or with non-standard terminology may have been missed. The completed search and the adjudicated re-screening added 44 studies to the 346 found at the first pass, so the first pass had an estimated sensitivity of about 89%, and the 84% inclusion agreement of the blind re-screen

implies that some eligible records remain among the exclusions. Second, title/abstract screening and coding were performed by a large-language-model assistant under the direction of the author, with every decision recorded; the 10% blind re-screening was performed by an independent run of the same assistant rather than by a second human reviewer (deviation D4), so the reported agreement measures the reproducibility of the assistant’s reading of the written codes, not human-machine agreement. Third, full texts could be read for 136 of the 388 synthesised studies within the review period, and 137 of the 362 first-pass assessed records and 33 of the 90 first-pass background records had no abstract in the metadata sources; the remaining studies were coded from abstracts read in the search results, and every extraction row that rests on an abstract is flagged. Reconciling the coding of the full-text studies with their full texts changed the evidence-type flags of 58 of the 136 (adding a magnitude in 25 cases, a metrology capability in 18, a statistical treatment or specification in 15 and a thermal effect in 5, and removing a thermal effect in 2 and a metrology capability in 1) and added at least one variation source to 56 of them; the coverage matrix (Fig. 2) is therefore a lower bound for the 252 abstract-level studies in the cells where abstracts are least informative—magnitude, metrology and statistics—and may be an upper bound where abstracts overstate what the paper delivers. The abstract-level studies do not enter the quantitative synthesis except through six flagged extraction rows: Tables II–IV and Fig. 4 draw on the 142 extracted studies, and the few abstract-level values that appear in the text are flagged; the 24 high-priority reports whose full text could not be obtained within the review period are the studies most likely to add rows to Tables II–IV, and they are identified in Supplementary Table S3b (priority H with the full-text flag N). Fourth, the extraction of thermal sensitivities depended on what the studies report; in fourteen rows a value was read from a figure and is marked as such, and the normalisation to percentage change per unit source uses the base resistance of each study, so that studies with very different base conditions appear side by side in Table III without a common denominator. Fifth, the adjacent power-module and LED literature was included as a comparator and dominates the void cells; its findings are reported separately and were not pooled with the core set. Sixth, no pooled effect sizes or formal heterogeneity statistics were computed, because the studies differ in package, method, base condition and outcome definition to a degree that would make a pooled value misleading; the synthesis is narrative with structured tables, and the tables are provided in full as supplementary material so that a reader can re-weight them.

X. CONCLUSION

Manufacturing variation in the thermally relevant features of advanced packages has been studied one source at a time, one evidence type at a time, and mostly on packages other than the flip-chip, 2.5D and 3D stacks that now carry the highest heat fluxes. Across 388 studies, the strongest quantitative evidence concerns the thermal effect of TIM properties, bond line and warpage in flip-chip packages, and the effect of die-attach voids in power modules and LEDs, where thermal resistance rises

linearly with the area of small distributed voids (0.5–1.2% per percentage point in the measured studies) and exponentially with the size of the largest contiguous void (growth constants of 0.015–0.032 per percentage point, giving a doubling by 22–46% voiding). Warpage acts on the thermal path through two mechanisms that the literature has now separated—a two- to four-fold thickening of the TIM at the die corners and a loss of contact wherever the compressible thickness of the TIM is less than the warpage height—and the corner-to-centre temperature-rise ratio of 1.5–2 measured on warped bare dies is the single most useful figure the review found for variation-aware design. Metrology is adequate for the geometry (voids and coverage to 5–40 μm , BLT to 1–8 μm , warpage to 1–2.5 μm) and increasingly adequate for the thermal resistance of single layers, but the gauge repeatability of the inspection metrics on which specifications are written is almost never reported, and the resistance of interfaces buried inside bonded stacks cannot yet be measured non-destructively. A statistical treatment or a specification appears in 72 studies, mostly designed experiments for nominal design or probabilistic models with assumed rather than measured input distributions, and only five studies derive a permitted variation from a thermal requirement. The empty cells—die thickness, bonded-interface variation with a measured stack-level thermal effect, TSV and BEOL variation, 2.5D interconnect layers, and any unit-level dataset that pairs a measured variation distribution with a measured θ_{JC} distribution—define the work that a variation-aware thermal design methodology for advanced packages requires.

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SUPPLEMENTARY MATERIAL

S1 Review protocol. S2 Search log with the 34 sub-queries, dates and hit counts, and the citation-chasing log with its candidate lists. S3a Screening decisions for all 2,253 records with exclusion codes; S3b coding of the 404 assessed records (408 rows: the records excluded or reclassified at coding are retained and marked; a column flags the 136 studies read in full text); S3c log of coding reconciliations made after full-text reading; S3d metadata of the included and background records; S3e metadata corrections; S3f the written screening codes; S3g blind re-screening decisions and adjudication. S4 Extraction table, one row per study $\times$ source $\times$ outcome,

with its README. S5a appraisal of the extracted studies; S5b normalised sensitivities.

REFERENCES

- [1] Y. Zhang, Y. Zhang, and M. S. Bakir, "Thermal Design and Constraints for Heterogeneous Integrated Chip Stacks and Isolation Technology Using Air Gap and Thermal Bridge," *IEEE Transactions on Components Packaging and Manufacturing Technology*, vol. 4, pp. 1914–1924, 2014, doi: 10.1109/tcpmt.2014.2364742.
- [2] S.-H. Lee, S.-J. Kim, J.-S. Lee, and S.-H. Rhi, "Thermal Issues Related to Hybrid Bonding of 3D-Stacked High Bandwidth Memory: A Comprehensive Review," *Electronics*, vol. 14, p. 2682, 2025, doi: 10.3390/electronics14132682.
- [3] B. Jiang, Y. Wu, Z. Zhong, K. Fan, Q. Lin, J. Liang, et al., "Cu–Cu hybrid bonding technology: from physical mechanisms to system integration for 3D ICs," *Moore and More*, vol. 2, 2025, doi: 10.1007/s44275-025-00036-1.
- [4] X. Wei, K. Marston, and K. K. Sikka, "Thermal modeling for warpage effects in organic packages," in *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)*, 2008, pp. 310–314, doi: 10.1109/itherm.2008.4544285.
- [5] C. Nelson, J. E. Galloway, C. Henry, and W. Kelley, "Thermal performance of TIMs during compressive and tensile stress states," in *2017 33rd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, 2017, pp. 261–268, doi: 10.1109/semi-therm.2017.7896939.
- [6] Y. Qiu, Z. Liu, P. Wu, L. Fu, H. Wang, L. Li, et al., "Void suppression in indium thermal interface materials for high-power packaging based on bubble dynamics modeling and process optimization," *Applied Thermal Engineering*, vol. 303, p. 131876, 2026, doi: 10.1016/j.applthermaleng.2026.131876.
- [7] K. Ouyang, Z. Wu, Z. Wang, W. Wang, D. Yang, and N. Mei, "Reliability analysis of metal thermal interface materials for ultra-large size FCLGA package," in *2023 China Semiconductor Technology International Conference (CSTIC)*, 2023, pp. 1–3, doi: 10.1109/cstic58779.2023.10219399.
- [8] W. Du, X. Wang, X. Yan, W. Li, L. Cai, G. Yang, et al., "Thermal-mechanical reliability enhancement of thermal interface material in lidded FCBGA packaging via SVR-based coverage degradation prediction," *Microelectronics Reliability*, vol. 182, p. 116180, 2026, doi: 10.1016/j.microrel.2026.116180.
- [9] Y. Lu, R. Zhou, H. Jiang, S. Qiao, J. Gu, Y. Zhou, et al., "Process-induced thermal conductivity degradation in Cu micro pads for 3D-IC hybrid bonding revealed by spatially resolved frequency-domain thermoreflectance," *Applied Thermal Engineering*, vol. 292, p. 130339, 2026, doi: 10.1016/j.applthermaleng.2026.130339.
- [10] F. Sarvar, D. C. Whalley, and P. P. Conway, "Thermal Interface Materials - A Review of the State of the Art," in *2006 1st Electronic System Integration Technology Conference*, 2006, pp. 1292–1302, doi: 10.1109/estc.2006.280178.
- [11] P. Rodgers, V. C. Evely, E. Rahim, and D. Morgan, "Thermal Performance and Reliability of Thermal Interface Materials: A Review," in *7th. Int. Conf. on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems*, 2006, pp. 1–2, doi: 10.1109/esime.2006.1644070.
- [12] B. Wei, W. Luo, J. Du, Y. Ding, Y. Guo, G. Zhu, et al., "Thermal interface materials: From fundamental research to applications," *SusMat*, vol. 4, 2024, doi: 10.1002/sus2.239.
- [13] J. Park, D. Kim, S. Yang, M. K. Kim, and H. So, "A comprehensive review of machine learning approaches for predicting warpage and thermal resistance in advanced semiconductor packaging," *JMST Advances*, vol. 8, pp. 71–90, 2026, doi: 10.1007/s42791-026-00131-w.
- [14] Y. Y. G. Hoe, Y. G. Jie, V. S. Rao, and M. W. D. Rhee, "Modeling and characterization of the thermal performance of advanced packaging materials in the flip-chip BGA and QFN packages," in *2012 IEEE 14th Electronics Packaging Technology Conference (EPTC)*, 2012, pp. 525–532, doi: 10.1109/eptc.2012.6507138.
- [15] M. Sternberg, D. May, D. R. Wargulski, K. A. Pareek, B. Wunderle, and M. A. Ras, "Thermal-Resistance-Based Reliability of TIM1 Materials in a Lidded Thermal Test Vehicle Under Active Thermal Load-Cycling," in *2025 31st International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2025, pp. 1–6, doi: 10.1109/therminic65879.2025.11216935.
- [16] I. Hu, J.-C. Tsai, F. Cheng, S.-F. Yen, M.-K. Shih, D. Tarng, et al., "High Power Large Size HFCBGA Thermal Characterization," in *2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)*, 2019, pp. 467–471, doi: 10.1109/eptc47984.2019.9026583.
- [17] A. Jain, D. P. Parekh, M. Bergendahl, and K. K. Sikka, "Analytical Solution for a Chip Temperature Distribution in a Multilayer Chip-Package with Thermal Warpage," in *2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)*, 2021, pp. 114–122, doi: 10.1109/itherm51669.2021.9503285.
- [18] T. Nordstog, C. Henry, C. Nelson, J. Galloway, P. Fosnot, and Q. Pham, "Junction to case thermal resistance variability due to temperature induced package warpage," in *2017 33rd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)*, 2017, pp. 235–245, doi: 10.1109/semi-therm.2017.7896936.
- [19] Y. Yang, Z. Zhang, and M. Touzelbaev, "Impact of temperature-dependent die warpage on TIM1 thermal resistance in field conditions," in *2009 25th Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 2009, pp. 285–292, doi: 10.1109/therm.2009.4810777.
- [20] R. J. Linderman, T. Brunschweiler, U. Kloter, H. Toy, and B. Michel, "Hierarchical Nested Surface Channels for Reduced Particle Stacking and Low-Resistance Thermal Interfaces," in *Twenty-Third Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 2007, pp. 87–94, doi: 10.1109/stherm.2007.352392.
- [21] M. R. Shirazy, S. Allard, M. Beaumier, and L. G. Frechette, "Effect of squeezing conditions on the particle distribution and bond line thickness of particle filled polymeric thermal interface materials," in *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)*, 2014, pp. 251–259, doi: 10.1109/itherm.2014.6892289.
- [22] S. L. Kanuparthi, J. E. Galloway, and S. McCain, "Impact of heatsink attach loading on FCBGA package thermal performance," in *13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2012, pp. 216–223, doi: 10.1109/itherm.2012.6231433.
- [23] Y. Lai, J. X. J. Ha, K. A. Deo, J. Yang, and S. Park, "Bond-line Thickness Prediction for Thermal Interface Material under Usage Conditions," in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*, 2024, pp. 1538–1542, doi: 10.1109/ectc51529.2024.00251.
- [24] D. Lee, R. Mayberry, A. Mackie, B. Hable, D. Heller, B. Jarrett, et al., "Optimizing Reflowed Solder TIM (sTIMs) Processes for Emerging Heterogeneous Integrated Packages," in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, 2022, pp. 1228–1237, doi: 10.1109/ectc51906.2022.00197.
- [25] P. Kulkarni, A. Davoodabadi, and S. Schiffrès, "Optimization of Reflow Profile for Solder Thermal Interface Materials with an Inline Vacuum Oven," in *2025 IEEE 75th Electronic Components and Technology Conference (ECTC)*, 2025, pp. 2211–2217, doi: 10.1109/ectc51687.2025.00376.
- [26] J. Wen, G. Sun, J. Su, Y. Fan, L. Fu, Z. Chen, et al., "AgIn2 thickness on void rate, microstructure, IMC growth, thermal and mechanical properties of fluxless In@AgIn2 joint," *Journal of Materials Research and Technology*, vol. 35, pp. 1072–1089, 2025, doi: 10.1016/j.jmrt.2025.01.098.
- [27] S. S. Too, M. Khan, E. Goh, X. Zhou, and K.-H. Keok, "Indium Thermal Interface Material Assembly Manufacturability and Reliability," in *Proc. 42nd Int. Symp. on Microelectronics (IMAPS 2009)*, IMAPS Source Proceedings, 2009, doi: 10.4071/001c.162061.
- [28] N. A. M. N. Aman, M. Z. Abdullah, L. W. Keat, and O. C. Keang, "Influence of die and lid shapes on void formation in solder thermal interface materials," *Microelectronics Reliability*, vol. 173, p. 115847, 2025, doi: 10.1016/j.microrel.2025.115847.
- [29] Y. Luo, F. Wang, W. Wang, N. Mei, and J. Fang, "Study on the Coverage of Metal Thermal Interface Material for Ultra-Large FCBGA Packaging," in *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*, 2022, pp. 1–5, doi: 10.1109/icept56209.2022.9873241.
- [30] K. Cox, J. Painter, G. Abu-Hamdeh, S. Tonthat, M. Borden, and J. Krantz, "Evaluation and Process Optimization of Heat-Curable Thermal Interface Materials for Advanced Packages," in *Proc. 57th Int. Symp. on Microelectronics (IMAPS 2024)*, IMAPS Source Proceedings, 2024, doi: 10.4071/001c.129521.
- [31] A. Jacques-Fortin, S. Allard, and K. C. Marston, "Quantitative and Qualitative Evaluation on the Influence of Heat Spreader Topography and Thermal Interface Material Properties on Thermal Performance of High-Power Computing (HPC) Semiconductor Packaging," in *2025 24th IEEE Intersociety Conference on Thermal and Thermomechanical*

- Phenomena in Electronic Systems (ITherm)*, 2025, pp. 1–6, doi: 10.1109/itherm55376.2025.11235750.
- [32] S. Ankireddi and D. Copeland, “A Statistical Approach For Characterizing The Thermal Impact Of TIM Voids,” in *Twenty-Third Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 2007, pp. 79–82, doi: 10.1109/stherm.2007.352390.
 - [33] G. Refai-Ahmed, H. H. Lee, and H. Do, “Impact of Lifetime and Mechanical Behaviors on TIM Performance for High-End Processor,” in *2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)*, 2018, pp. 776–780, doi: 10.1109/eptc.2018.8654267.
 - [34] J. Hua, F. Wang, Z. Hu, Z. Tang, J. Fang, and G. Li, “The Degradation Mechanism of Indium TIM Coverage in Ultra-Large Size FCBGA Packaging,” in *2024 25th International Conference on Electronic Packaging Technology (ICEPT)*, 2024, pp. 1–3, doi: 10.1109/icept63120.2024.10668656.
 - [35] H. Zhang, S. Li, H. Liu, J. Bunt, F. Pompeo, K. Sikka, et al., “Failure analysis of thermal degradation of TIM during power cycling,” in *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2014, pp. 404–408, doi: 10.1109/itherm.2014.6892309.
 - [36] O. Yenigun, V. O. Cherman, H. Oprins, G. Van der Plas, E. Beyne, and I. De Wolf, “Temperature and pressure dependent thermal interface material characterization using packaged thermal test vehicle assemblies,” in *2024 23rd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2024, pp. 1–9, doi: 10.1109/itherm55375.2024.10709569.
 - [37] O. Yenigun, M. González, V. O. Cherman, M. Lofrano, Y. Yao, G. Van der Plas, et al., “Coupled Thermal and Mechanical Analysis of Thermal Interface Materials in Electronic Packaging,” *IEEE Transactions on Components Packaging and Manufacturing Technology*, vol. 16, pp. 1567–1575, 2026, doi: 10.1109/tcpmt.2025.3633174.
 - [38] S. Lin, V. Lin, A. Kang, and Y. Wang, “Thermal Performance of High Thermal Conductivity TIM for Large Advanced Package through TTV Measurement and FEM Analysis Approach,” in *Proc. 58th Int. Symp. on Microelectronics (IMAPS 2025)*, *IMAPSource Proceedings*, 2025, doi: 10.4071/001c.147482.
 - [39] Z. Zhang, P. Kulkarni, M. A. Daeumer, A. R. Gharaibeh, J.-Y. Chang, B. G. Sammakia, et al., “Spatial Thermal Conductivity Variation of Particulate-Filled Thermal Interface Materials,” in *2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2022, pp. 1–7, doi: 10.1109/itherm54085.2022.9899581.
 - [40] X. Feng, C. King, D. DeVoto, M. Mihalic, and S. Narumanchi, “Investigation of thermal interface materials using phase-sensitive transient thermoreflectance technique,” in *Fourteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2014, pp. 1296–1307, doi: 10.1109/itherm.2014.6892430.
 - [41] P.-Y. Lin, C. Chen, K. Yan, and J. R. He, “Analysis of Package-to-System Interaction on Thermal Performance of Large 2.5D Packages Using 3DFabric® Platform,” in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, 2023, pp. 918–922, doi: 10.1109/ectc51909.2023.00157.
 - [42] D. DeVoto, J. Major, P. Paret, G. S. Blackman, A. Wong, and J. S. Meth, “Degradation characterization of thermal interface greases,” in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 394–399, doi: 10.1109/itherm.2017.7992501.
 - [43] G. K. Morris, M. Polakowski, L. Wei, M. D. Ball, M. G. Phillips, C. Mosey, et al., “Thermal interface material evaluation for IGBT modules under realistic power cycling conditions,” in *2015 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, 2015, pp. 111–114, doi: 10.1109/iwipp.2015.7295991.
 - [44] T. Sinha and J. A. Zitz, “A systematic experimental investigation of thermal degradation mechanisms in lidded flip-chip packages: Effects of thermal aging and cyclic loading,” in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 537–543, doi: 10.1109/itherm.2017.7992533.
 - [45] L. Bharatham, W. S. Fong, C. J. Leong, and C.-P. Chiu, “A Study of Application Pressure on Thermal Interface Material Performance and Reliability on FCBGA Package,” in *2006 International Conference on Electronic Materials and Packaging*, 2006, pp. 1–7, doi: 10.1109/emap.2006.4430584.
 - [46] J. Galloway and S. Kanuparthi, “BLT control and its impact on FCBGA thermal performance,” in *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2008, pp. 388–394, doi: 10.1109/itherm.2008.4544296.
 - [47] E. Anderson and C. Green, “Analysis of Die Warpage and TIM Process Parameters: Thermal Resiliency Using Nanotube-Based Interface Material,” in *ASME 2025 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*, 2025, doi: 10.1115/ipack2025-164317.
 - [48] Y. Niu, W. Wang, Z. Wang, K. Dhandapani, M. Schwarz, and A. R. Syed, “Warpage Variation Analysis and Model Prediction for Molded Packages,” in *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*, 2019, pp. 819–824, doi: 10.1109/ectc.2019.00129.
 - [49] Q. Zhang, J. C. C. Lo, S. W. R. Lee, and W. P. Xu, “Determination of a Meaningful Warpage Acceptance Criterion for Large PBGA Components Through the Correlation with Scattering in Material Properties,” in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018, pp. 718–723, doi: 10.1109/ectc.2018.00112.
 - [50] C. Foong, A. Afripi, N. Lakhera, and T. Uehling, “Analysis of Thin Flip Chip Chip-Scale Package Warpage Causes and Variations,” in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*, 2024, pp. 1286–1292, doi: 10.1109/ectc51529.2024.00209.
 - [51] R.-Y. Hu, C.-H. Chen, H.-L. Liang, and S.-J. Chang, “Influence of Pre-bond Nanotopography and Local Warp on Post-bond Performance in Hybrid Bonding,” in *2026 37th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, 2026, pp. 1–6, doi: 10.1109/asmc69324.2026.11551257.
 - [52] F. Inoue, A. Jourdain, J. De Vos, E. Slecckx, E. Beyne, J. Patel, et al., “Characterization of Extreme Si Thinning Process for Wafer-to-Wafer Stacking,” in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 2095–2102, doi: 10.1109/ectc.2016.102.
 - [53] C. Yuan, A. Xiao, J. Salta, M. de Langen, and W. van Driel, “Thermal modeling for advanced high power packaging development and on-line performance monitoring,” in *3rd Electronics System Integration Technology Conference ESTC*, 2010, pp. 1–5, doi: 10.1109/estc.2010.5642900.
 - [54] S. H. Zandavi, A. J. Schmidt, and X. F. Brun, “Assessing thermal resistance in fusion bond layers of 3D heterogeneous electronics packaging,” *Journal of Applied Physics*, vol. 136, 2024, doi: 10.1063/5.0224398.
 - [55] Y. Li, L. Song, J. Lyu, S. Qiao, and L. Yang, “Passivating Interfacial Pore Defects with Light Atoms To Enhance Heat Transport Across Cu/a-SiO₂ Interfaces,” *Nano Letters*, vol. 26, pp. 3204–3212, 2026, doi: 10.1021/acs.nanolett.5c06478.
 - [56] H. Kabaria, S. D. B. Mohideen, J. L. Davenport, B. Cherukuri, J. Kocheemoolayil, N. Patil, et al., “Thermal Sensitivity Analysis of 3D IC Face-to-Back Stacking Using Foundation Models for Physics,” in *2025 IEEE 27th Electronics Packaging Technology Conference (EPTC)*, 2025, pp. 1–8, doi: 10.1109/eptc67330.2025.11392147.
 - [57] H. Kim, J. Kim, Y. Kim, S.-K. Seo, C. Jo, and D.-W. Kim, “Process and Design Optimization for Hybrid Cu Bonding Void,” in *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*, 2022, pp. 194–197, doi: 10.1109/ectc51906.2022.00041.
 - [58] J. Choi and J. Lim, “Thermal Impact of TSV Misalignment and Micro-Bump Height in 3D IC Packages,” in *2025 22nd International SoC Design Conference (ISOCC)*, 2025, pp. 1–2, doi: 10.1109/isocc66390.2025.11330057.
 - [59] Z. Huang, K. Yang, Y. He, Z. Dong, Z. Sun, X. Tang, et al., “First Demonstration of Three-Dimensional Thermal Conductivity Distribution Measurements of Interconnect Stacks Down to 3nm Process Nodes,” in *2025 IEEE International Electron Devices Meeting (IEDM)*, 2025, pp. 1–4, doi: 10.1109/iedm50572.2025.11353753.
 - [60] H.-C. Chien, Y.-L. Chao, J. H. Lau, R.-M. Tain, M.-J. Dai, P.-J. Tzeng, et al., “A thermal performance measurement method for blind through silicon vias (TSVs) in a 300mm wafer,” in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 1204–1210, doi: 10.1109/ectc.2011.5898663.
 - [61] M. Schmid, A. Zippelius, A. Hanß, S. Böckhorst, and G. Elger, “Investigations on High-Power LEDs and Solder Interconnects in Automotive Application: Part I—Initial Characterization,” *IEEE Transactions on Device and Materials Reliability*, vol. 22, pp. 175–186, 2022, doi: 10.1109/tdmr.2022.3152590.
 - [62] S. Y. Jo, G.-J. Sim, E. J. Park, J. Park, J. Y. Won, H. Kim, et al., “Effect of solder void on mechanical and thermal properties of flip-chip light-emitting diode: Statistical analysis based on finite element modeling,” *Heliyon*, vol. 10, p. e33242, 2024, doi: 10.1016/j.heliyon.2024.e33242.
 - [63] J. Lee, J. Jung, J. Bae, J. An, and J. Lee, “Statistical Study on the Characteristics and Thermal Quality of Solder Voids in Automotive LEDs,” *Journal of Korean Society for Quality Management*, vol. 53, pp. 461–486, 2025, doi: 10.7469/jksqm.2025.53.4.461.
 - [64] Y. Yu and V. A. Chiriac, “Effects of Solder Voids on Thermal and Reliability Performances of PQFN Packages,” in *Proc. 42nd Int. Symp.*

- on *Microelectronics (IMAPS 2009)*, *IMAPSource Proceedings*, 2009, doi: 10.4071/001c.161907.
- [65] S. Singh, J. Hao, D. Hoffman, T. Dixon, A. Zedolik, J. Fazio, et al., "Effects of Die-Attach Voids on the Thermal Impedance of Power Electronic Packages," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 7, pp. 1608–1616, 2017, doi: 10.1109/tcpmt.2017.2742467.
- [66] D. C. Katsis and J. D. van Wyk, "Void-induced thermal impedance in power semiconductor modules: Some transient temperature effects," *IEEE Transactions on Industry Applications*, vol. 39, pp. 1239–1246, 2003, doi: 10.1109/tia.2003.816527.
- [67] D. C. Katsis and J. D. van Wyk, "A thermal, mechanical, and electrical study of voiding in the solder die-attach of power MOSFETs," *IEEE Transactions on Components and Packaging Technologies*, vol. 29, pp. 127–136, 2006, doi: 10.1109/tcpmt.2005.853301.
- [68] C. Jiang, J. Fan, C. Qian, H. Zhang, X. Fan, W. Guo, et al., "Effects of Voids on Mechanical and Thermal Properties of the Die Attach Solder Layer Used in High-Power LED Chip-Scale Packages," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 8, pp. 1254–1262, 2018, doi: 10.1109/tcpmt.2018.2789345.
- [69] N. Carlson and N. Baker, "Solder Void Impact on Power Device Thermal Impedance using Transient Thermal Analysis," in *2025 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, 2025, pp. 1–6, doi: 10.1109/iwipp61784.2025.10971713.
- [70] Y. Shi, W. Zhu, and H. He, "A Novel Approach to Evaluate and Predict the Impact of Randomly Distributed Voids on Junction Temperature for Power Modules," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 12, pp. 42–50, 2022, doi: 10.1109/tcpmt.2021.3135628.
- [71] Y. Wei, X. Yang, P. Wu, and G. Liu, "A Data-Driven Approach to Predict the Impact of Void Characteristics on IGBT Junction Temperature," *IEEE Transactions on Electron Devices*, vol. 73, pp. 2106–2115, 2026, doi: 10.1109/ted.2026.3670798.
- [72] L. Wu, Y. Yang, X. Yang, H. Ma, H. Gong, and S. Hou, "Research on the Effects of Solder Layer THICKNESS on the Reliability of High Power IGBT Module," in *2023 6th International Conference on Electronics Technology (ICET)*, 2023, pp. 965–969, doi: 10.1109/icet58434.2023.10211457.
- [73] C. Yue, M. Lu, and Z. Niu, "The influence of die tilting on the thermal response and die attach stress of a bottom exposed package," in *2012 13th International Conference on Electronic Packaging Technology & High Density Packaging*, 2012, pp. 685–690, doi: 10.1109/icept-hdp.2012.6474711.
- [74] B. Ottinger, S. Murk, S. König, A. Zangarro, M. J. Müllmaier, D. L. Müller, et al., "Location dependent down-rating of voids in high power solder connections for automotive power modules," in *Proc. 55th Int. Symp. on Microelectronics (IMAPS 2022)*, *IMAPSource Proceedings*, 2022, doi: 10.4071/001c.89938.
- [75] I. Dchar and D. Yandoc, "Impact of Die-Attach Voids on the Thermal Performances of Clip-Bonded Packages," in *2024 IEEE 26th Electronics Packaging Technology Conference (EPTC)*, 2024, pp. 1166–1169, doi: 10.1109/eptc62800.2024.10909785.
- [76] K. C. Otiaba, R. Bhatti, N. N. Ekere, S. Mallik, E. H. Amalu, and M. Ekpu, "Thermal effects of die-attach voids location and style on performance of chip level package," in *3rd IEEE International Conference on Adaptive Science and Technology (ICAST 2011)*, 2011, pp. 231–236, doi: 10.1109/icastech.2011.6145176.
- [77] A. S. Fleischer, L.-H. Chang, and B. C. Johnson, "The effect of die attach voiding on the thermal resistance of chip level packages," *Microelectronics Reliability*, vol. 46, pp. 794–804, 2006, doi: 10.1016/j.microrel.2005.01.019.
- [78] R. Liang, J. Zhang, S. Wang, Q. Chen, L. Xu, J. Dai, et al., "Investigation on Thermal Characterization of Eutectic Flip-Chip UV-LEDs With Different Bonding Voidage," *IEEE Transactions on Electron Devices*, vol. 64, pp. 1174–1179, 2017, doi: 10.1109/ted.2017.2656240.
- [79] O. Alavi, W. De Ceuninck, and M. Daenen, "Impact of Solder Voids on IGBT Thermal Behavior: A Multi-Methodological Approach," *Electronics*, vol. 13, p. 2188, 2024, doi: 10.3390/electronics13112188.
- [80] M. B. Stern, D. Kearns, V. Gektin, and G. Jhoty, "A Methodology for Thermal Evaluation of Strongly Bonded Packaging Materials," in *Thermal and Thermomechanical Proceedings 10th Intersociety Conference on Phenomena in Electronics Systems*, 2006. *ITHERM 2006*, 2006, pp. 505–511, doi: 10.1109/itherm.2006.1645386.
- [81] M. Schmid, A. Zippelius, A. Hanß, S. Böckhorst, and G. Elger, "Investigations on High-Power LEDs and Solder Interconnects in Automotive Application: Part II—Reliability," *IEEE Transactions on Device and Materials Reliability*, vol. 23, pp. 419–429, 2023, doi: 10.1109/tdmr.2023.3300355.
- [82] P.-Y. Pichon and J. Brandelero, "Relative importance of solder and wire bond defects on the maximum junction temperature of IGBT devices," *Microelectronics Reliability*, vol. 126, p. 114250, 2021, doi: 10.1016/j.microrel.2021.114250.
- [83] B. Thollin, L. Dupont, Y. Avenas, J.-C. Crebier, Z. Khatir, and P.-O. Jeannin, "Numerical and Experimental Evaluation of the Microsecond Pulsed Heating Curve Technique Dedicated to Die Interconnection Characterization," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, pp. 835–845, 2016, doi: 10.1109/tcpmt.2016.2554538.
- [84] V. Khuu, M. D. Osterman, A. Bar-Cohen, and M. G. Pecht, "Effects of Temperature Cycling and Elevated Temperature/Humidity on the Thermal Performance of Thermal Interface Materials," *IEEE Transactions on Device and Materials Reliability*, vol. 9, pp. 379–391, 2009, doi: 10.1109/tdmr.2009.2025367.
- [85] Q. Li, F. Zhang, Y. Chen, T. Fu, and Z. Zheng, "A junction temperature model based on heat flow distribution in an IGBT module with solder layer voids," *Heliyon*, vol. 10, p. e33625, 2024, doi: 10.1016/j.heliyon.2024.e33625.
- [86] C. Chen, M. Su, R. Ma, F. Hou, L. Cao, and J. Li, "Analytical Assessment of the Effect of Thermal Interface Layer Voids on Temperature in Lid-Integral Microchannel Coldplate Cooling," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 10, pp. 1000–1009, 2020, doi: 10.1109/tcpmt.2020.2982012.
- [87] B. Smith, T. Brunschweiler, and B. Michel, "Utility of transient testing to characterize thermal interface materials," in *2007 13th International Workshop on Thermal Investigation of ICs and Systems (THERMINIC)*, 2007, pp. 6–11, doi: 10.1109/therminic.2007.4451738.
- [88] I. Hu, M. Shih, and G. Kao, "Performance and reliability of TIM in high power HFCBGA," in *2015 10th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2015, pp. 188–191, doi: 10.1109/impact.2015.7365218.
- [89] T. Z. Fullem, D. F. Rae, A. Sharma, J. A. Wolcott, and E. J. Cotts, "Thermal characterization of thermal interface material bondlines," in *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITHERM)*, 2008, pp. 174–179, doi: 10.1109/itherm.2008.4544268.
- [90] J. Lee and W. Park, "Investigation of thermal transport across volume-controlled thermal interface materials," *Polymer Testing*, vol. 146, p. 108780, 2025, doi: 10.1016/j.polymeresting.2025.108780.
- [91] R. Jiang, C. Zhong, H. Wang, C. Li, Y. Zheng, L. Ren, et al., "The Effect of Thermal-Induced Warpage and Degeneration of Thermal Interface Materials on the Thermal Performance of a Flip-Chip Package," in *2021 22nd International Conference on Electronic Packaging Technology (ICEPT)*, 2021, pp. 1–5, doi: 10.1109/icept52650.2021.9567944.
- [92] Y. Hu, S. Fei, L. Ma, N. Yan, and J. Wang, "Thermal and Mechanical Reliability of TIM1 in FCBGA Using a Simplified Sandwich Model," in *2025 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, 2025, pp. 222–223, doi: 10.1109/icta68203.2025.11329835.
- [93] M. Sternberg, D. May, K. A. Pareek, V. Bader, K.-F. Becker, B. Wunderle, et al., "Thermal Test Vehicle for HPC – System Level Approach for Investigation of the Thermal Heat Path Signature with the Property of Spatial Resolution," in *2023 29th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2023, pp. 1–7, doi: 10.1109/therminic60375.2023.10325887.
- [94] N. Bhawe and N. Okamoto, "Modeling noncoplanarity effects on thermal performance of computer chips," in *2007 12th International Symposium on Advanced Packaging Materials: Processes, Properties, and Interfaces*, 2007, pp. 47–52, doi: 10.1109/isapm.2007.4419927.
- [95] S. S. Pang and M. Z. Abdullah, "Thermal Impact of Heat Spreader Co-Planarity to Electronic Packaging," *Journal of Advanced Research in Fluid Mechanics and Thermal Sciences*, vol. 71, pp. 1–9, 2020, doi: 10.37934/arfm.71.1.19.
- [96] J. Xu, C. Chen, B. Chen, J. Luo, and B. Yuan, "Study of influencing factors on thermal characteristics in multidie 2.5D/3D packaging," in *Proc. SPIE, International Conference on Physics, Photonics and Optical Engineering (ICPPOE 2025)*, 2026, doi: 10.1117/12.3108548.
- [97] S. Lin, K. Zhang, V. Lin, D. Lai, and Y. Wang, "TIM Coverage Evaluation for High Performance Computing Application," in *2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)*, 2022, pp. 1–5, doi: 10.1109/itherm54085.2022.9899667.
- [98] A. Gowda, D. Esler, S. S. Tonapi, K. R. Nagarkar, and K. Srihari, "Voids in thermal interface material layers and their effect on thermal

- performance,” in *Proceedings of 6th Electronics Packaging Technology Conference (EPTC 2004)* (IEEE Cat. No.04EX971), 2004, pp. 41–46, doi: 10.1109/eptc.2004.1396574.
- [99] M.-H. Song and W. K. Tang, “Non-Destructive Analysis of Voiding in Thermal Interface Material of High-Performance Computing Devices Using B-Mode Scanning Acoustic Microscopy (B-SAM),” in *2024 IEEE 26th Electronics Packaging Technology Conference (EPTC)*, 2024, pp. 1047–1051, doi: 10.1109/eptc62800.2024.10909832.
- [100] M.-H. Song, Z.-Y. Oh, X.-W. Lee, M. Ng, B. Zee, F.-J. Foo, et al., “Robust Image Processing Software for Void Calculation in Thermal Interface Materials,” in *2023 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2023, pp. 1–8, doi: 10.1109/ipfa58228.2023.10249157.
- [101] S. Guo, Y. Huang, D. Chen, L. Ren, D. Wang, and W. Feng, “In-Situ Ultrasonic Inspection of Thickness and Morphology of Thermal Interface Material in Multilayer Structure Using Modified Minimum Entropy Deconvolution,” *IEEE Transactions on Instrumentation and Measurement*, vol. 71, pp. 1–10, 2022, doi: 10.1109/tim.2022.3210962.
- [102] D. May, S. Fritzsche, A. Cardoso, R. Schacht, and B. Wunderle, “IR pulse thermography as failure analytical tool applied to die attach processes,” in *2015 21st International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2015, pp. 1–7, doi: 10.1109/therminic.2015.7389622.
- [103] D. May, B. Wunderle, R. Schacht, and B. Michel, “Transient thermal analysis as failure analytical tool in electronic packaging,” in *2012 13th International Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, 2012, pp. 1–8, doi: 10.1109/esime.2012.6191725.
- [104] A. Gupta, Y. Liu, N. Zamora, and T. Paddock, “Thermal imaging for detecting thermal interface issues in assembly and reliability stressing,” in *Thermal and Thermomechanical Proceedings 10th Intersociety Conference on Phenomena in Electronics Systems*, 2006. *ITHERM 2006*, 2006, pp. 942–945, doi: 10.1109/itherm.2006.1645447.
- [105] H. Heng, V. Ben, K. Keok, and J. Riemer, “Nondestructive method of TIM bondline measurement in Flip Chips package,” in *2008 33rd IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT)*, 2008, pp. 1–5, doi: 10.1109/iemt.2008.5507830.
- [106] S. Chang and L.-P. Chen, “Advanced Measurement Method for Thermal Interface Material Thickness of Flip Chip Package,” in *2021 16th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2021, pp. 235–236, doi: 10.1109/impact53160.2021.9696757.
- [107] B. K. Tanner, P. J. McNally, and A. Danilewsky, “X-ray imaging of silicon die within fully packaged semiconductor devices,” *Powder Diffraction*, vol. 36, pp. 78–84, 2021, doi: 10.1017/s088571562100021x.
- [108] G. L. Solbrekken, C.-P. Chiu, B. Byers, and D. Reichenbacher, “The development of a tool to predict package level thermal interface material performance,” in *ITHERM 2000: Seventh Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2000, pp. 48–54, doi: 10.1109/itherm.2000.866807.
- [109] R. J. Warzoha, A. N. Smith, and M. Harris, “Improved methodology for calculating interfacial thermal resistance and uncertainty for steady-state TIM testers with embedded probes,” in *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2016, pp. 1040–1050, doi: 10.1109/itherm.2016.7517662.
- [110] F. Streb, M. Mengel, D. Schweitzer, C. Kasztelan, P. Schoderböck, G. G. Ruhl, et al., “Characterization Methods for Solid Thermal Interface Materials,” *IEEE Transactions on Components Packaging and Manufacturing Technology*, vol. 8, pp. 1024–1031, 2018, doi: 10.1109/tcpmt.2017.2748238.
- [111] W. Song, G. Lee, and B. D. Yoon, “Toward robust structure function-based thermal analysis: Quantitative metrics for semiconductor packaging evaluation,” *Microelectronics Reliability*, vol. 173, p. 115867, 2025, doi: 10.1016/j.microrel.2025.115867.
- [112] Y. Qiu, C. Liu, Y. Zeng, and Q. Zheng, “Physics-guided, uncertainty-aware machine learning for non-invasive deep thermal interface characterization in hybrid-bonded 3D ICs without prior geometric knowledge,” *International Journal of Heat and Mass Transfer*, vol. 263, p. 128717, 2026, doi: 10.1016/j.ijheatmasstransfer.2026.128717.
- [113] H. A. Martin, S. Libon, E. C. Smits, R. H. Poelma, W. D. van Driel, and G. Zhang, “Thermal characterization methodology for thin bondline interfaces with high conductive materials,” *Thermal Science and Engineering Progress*, vol. 53, p. 102754, 2024, doi: 10.1016/j.tsep.2024.102754.
- [114] A. U. Gaitonde, J. A. Weibel, and A. M. Marconnet, “Feasibility Assessment of Metrologies for Thermal Resistance Characterization of Deeply Buried Interfaces between Bonded Silicon Layers,” in *2023 22nd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2023, pp. 1–7, doi: 10.1109/itherm55368.2023.10177615.
- [115] S. Gao, K. D. T. Ngo, and G.-Q. Lu, “Two-Dimensional Mapping of Interface Thermal Resistance by Transient Thermal Measurement,” *IEEE Transactions on Industrial Electronics*, vol. 68, pp. 4448–4456, 2021, doi: 10.1109/tie.2020.2984997.
- [116] Z. Wu, Z. Wang, D. Qi, X. Lin, D. Yang, and N. Mei, “Correlation Analysis between Warpage and Metal Thermal Interface Materials Thermo-mechanical Reliability of Large size FCBGA,” in *2023 24th International Conference on Electronic Packaging Technology (ICEPT)*, 2023, pp. 1–4, doi: 10.1109/icept59018.2023.10492102.
- [117] M. Ekpu, “Optimisation of a microelectronic assembly package using response surface methodology,” *Nigerian Journal of Technology*, vol. 39, pp. 1058–1065, 2021, doi: 10.4314/njt.v39i4.12.
- [118] L. Fu, Q. Dai, B. Zheng, D. Cao, W. Zhu, and L. Wang, “Numerical Investigation on the Influence of Voiding in Indium-Based Thermal Interface Materials for Thermal Performance in Flip-Chip Packages,” in *2025 26th International Conference on Electronic Packaging Technology (ICEPT)*, 2025, pp. 1–5, doi: 10.1109/icept67137.2025.11157277.
- [119] W. Ren, Q. Wang, D. Chen, G. Wang, S. Cai, and H. Yang, “Global optimization of junction-to-case thermal resistance in TO-247 power MOSFETs using hybrid response surface methodology,” *Case Studies in Thermal Engineering*, vol. 76, p. 107399, 2025, doi: 10.1016/j.csite.2025.107399.
- [120] M. Montano, J. G. Garcia, W. Shi, M. T. Reiter, U. Vadakkan, K. L. Phillippe, et al., “Novel Process Techniques to Reduce Voids in Solder Thermal Interface Materials Used for Flip-Chip Package Applications,” in *Heat Transfer: Volume 4*, 2005, pp. 885–890, doi: 10.1115/ht2005-72747.
- [121] Y. Yokono, K. Hisano, and K. Hirohata, “Robust Thermal Design for Power Device Package Using Response Surface Method and Monte Carlo Simulation,” *Journal of Thermal Science and Technology*, vol. 3, pp. 452–460, 2008, doi: 10.1299/jtst.3.452.
- [122] L. Codecasa and L. Di Rienzo, “Stochastic thermal modeling by polynomial chaos expansion,” in *19th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2013, pp. 33–38, doi: 10.1109/therminic.2013.6675234.
- [123] H. E. Nouino, O. Bendaou, O. Bendaou, L. Canale, and A. Asselman, “Finite element sensitivity and reliability analysis with application in thermal management of LED packages,” in *2021 IEEE Industry Applications Society Annual Meeting (IAS)*, 2021, pp. 1–6, doi: 10.1109/ias48185.2021.9677138.
- [124] H. Elnouino, O. Bendaou, and O. Bendaou, “Reliability-based Design Optimization (RBDO) Study Applied to the Thermal Management of a Multi-Led Chip Package,” *Journal of Engineering and Technological Sciences*, vol. 56, pp. 521–534, 2024, doi: 10.5614/j.eng.technol.sci.2024.56.4.8.
- [125] M. Lin, C. Zheng, Y. Yang, N. Ye, and B. Yang, “NAND Package Warpage Prediction and Design with Tolerance Through Machine Learning,” in *2025 IEEE 75th Electronic Components and Technology Conference (ECTC)*, 2025, pp. 202–207, doi: 10.1109/ectc51687.2025.00040.
- [126] C. K. Chee, S. Hsu, J. Patel, and A. Bamido, “Thermal Solutions For Large Die and Package,” in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, 2023, pp. 929–934, doi: 10.1109/ectc51909.2023.00159.
- [127] Z. Zhou, Y. He, S. Liu, L. Yang, and N. Yang, “Effect of Non-Fourier Heat Transport on Temperature Distribution in High Bandwidth Memory,” *IEEE Transactions on Electron Devices*, vol. 73, pp. 561–568, 2026, doi: 10.1109/ted.2025.3628342.
- [128] Y. Lee and S. W. Yoon, “Thermal Conductivity Aware Design Approach of Non-Conductive Film Layers for Enhanced Vertical Heat Dissipation in 3D HBM Packages,” in *2025 IEEE CPMT Symposium Japan (ICSJ)*, 2025, pp. 84–87, doi: 10.1109/icsj66986.2025.11302612.
- [129] Y. Yamaji, T. Ando, T. Morifuji, M. Tomisaka, M. Sunohara, T. Sato, et al., “Thermal characterization of bare-die stacked modules with Cu through-vias,” in *2001 Proceedings. 51st Electronic Components and Technology Conference (ECTC)*, 2001, pp. 730–732, doi: 10.1109/ectc.2001.927813.
- [130] C. K. Jiang, L. Nie, W. Jia, and Y. N. Zhong, “Thermal distribution analysis of inner defects in TSV,” *E3S Web of Conferences*, vol. 38, p. 04026, 2018, doi: 10.1051/e3sconf/20183804026.
- [131] Y. L. Huang, C. K. Chung, C. Lin, K. H. Yu, R. J. Lin, and W. Hong, “Highly Thermal Dissipation for Large HPC Package Using Liquid Metal Materials,” in *2021 IEEE 71st Electronic Components and Technology*

- Conference (ECTC)*, 2021, pp. 1102–1108, doi: 10.1109/ectc32696.2021.00180.
- [132] H.-H. Hsu, C.-M. Wang, H. Lee, and A. T. Wu, “Non-destructive testing method for chip warpage -Applications of synchrotron radiation X-ray,” in *2016 International Conference on Electronics Packaging (ICEP)*, 2016, pp. 15–18, doi: 10.1109/icep.2016.7486772.
- [133] T. C. Lee, C. H. Chen, L. Cao, Y. S. Su, C. J. Zhuang, H. Kuo, et al., “Technology Enhancements on Focos-Bridge for Emerging Trends in High-Performance Computing (HPC) and Artificial Intelligence (AI),” in *2025 IEEE 75th Electronic Components and Technology Conference (ECTC)*, 2025, pp. 902–905, doi: 10.1109/ectc51687.2025.00158.
- [134] Z. Xu, Y. Q. Cao, C. Zhong, Y. Tian, Y. Feng, H. Nan, et al., “A Temperature-modified Semi-empirical Quantitative Physical Model for Predicting Interfacial Thermal Resistance for Chiplet Packaging,” in *2025 26th International Conference on Electronic Packaging Technology (ICEPT)*, 2025, pp. 1–4, doi: 10.1109/icept67137.2025.11157178.
- [135] M. Mukadam, J. Schake, P. Borgesen, and K. Srihari, “Effects of assembly process variables on voiding at a thermal interface,” in *The Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena In Electronic Systems (IEEE Cat. No.04CH37543)*, 2004, pp. 58–62, doi: 10.1109/therm.2004.1319154.
- [136] Y. Qiu, Z. Liu, L. Fu, P. Wu, L. Li, D. Cao, et al., “Influence of argon hydrogen plasma treatment on the wettability, void and high temperature reflow reliability of indium thermal interface material for FCBGA package,” *Materials Science in Semiconductor Processing*, vol. 205, p. 110314, 2026, doi: 10.1016/j.mssp.2025.110314.
- [137] P. Xu, P. Liu, L. Yan, and Z. Zhang, “Effect of Solder Layer Void Damage on the Temperature of IGBT Modules,” *Micromachines*, vol. 14, p. 1344, 2023, doi: 10.3390/mi14071344.
- [138] D. May, J. Heilmann, E. Boschman, M. A. Ras, and B. Wunderle, “Tilt- and warpage measurement of bonded dies as an inline quality assessment tool,” in *2021 22nd International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2021, pp. 1–7, doi: 10.1109/eurosimE2021.9410832.
- [139] S. S. Too, J. Hayward, R. Master, T.-S. Tan, and K.-H. Keok, “Effects of Organic Package Warpage on Microprocessor Thermal Performance,” in *2007 Proceedings 57th Electronic Components and Technology Conference*, 2007, pp. 748–754, doi: 10.1109/ectc.2007.373881.
- [140] J. Zhou, X. Long, J. He, F. Ren, and L. Fang, “Uncertainty Quantification for Junction Temperature of Automotive LED With Die-Attach Layer Microstructure,” *IEEE Transactions on Device and Materials Reliability*, vol. 18, pp. 86–96, 2018, doi: 10.1109/tdmr.2018.2796072.
- [141] R. Upreti, S. Chintamani, S. Patil, A. Akbariyeh, and B. H. Dennis, “Stochastic Finite Element Thermal Analysis of a Ball Grid Array Package,” *Journal of Electronic Packaging*, vol. 144, 2021, doi: 10.1115/1.4050696.
- [142] M. Koide, K. Fukuzono, T. Sato, K. Abe, and H. Fujisaki, “High-Performance Flip-Chip BGA Technology Based on Thin-Core and Coreless Package Substrate,” *Journal of Japan Institute of Electronics Packaging*, vol. 11, pp. 212–216, 2008, doi: 10.5104/jiep.11.212.
- [143] A. Salahouelhadj, M. González, and H. Oprins, “Die thickness impact on thermo-mechanical stress in 3D packages,” in *2015 16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2015, pp. 1–6, doi: 10.1109/eurosimE.2015.7103104.