

PowerScope: Preliminary Design of a Portable Dual-Channel Digital Oscilloscope and Programmable DC Power Supply

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Abstract—This paper presents the preliminary system architecture and circuit-level design of PowerScope, a proposed portable instrument that combines a two-channel digital oscilloscope with a programmable DC power supply. The oscilloscope path uses protected and selectable-range analog front ends, a dual 14-bit AD9251 analog-to-digital converter, a planned FPGA capture stage, and an ESP32-S3 supervisory controller for display and wireless monitoring. The power path uses a four-cell lithium-ion battery, battery monitoring and protection, a charger interface, and an LM5176-based buck-boost converter targeted at 1–15 V and up to 2 A. The paper reports analytical calculations for input scaling, ideal anti-alias response, sample throughput, record memory, converter sizing, and sampling/aliasing behavior. Draft schematics and design tables are included in monochrome form. The available project records do not contain completed Proteus simulations or hardware measurements; calculated values are therefore distinguished from results requiring validation. Conflicting bandwidth and sampling-rate baselines, analog-filter placement, converter current limiting, and several unselected digital interfaces are identified as open design decisions.

Index Terms—digital oscilloscope, programmable power supply, analog front end, analog-to-digital converter, buck-boost converter, battery management, embedded instrumentation

I. INTRODUCTION

Laboratory instruments often separate waveform observation from adjustable DC power delivery. PowerScope is a proposed battery-powered unit that combines a dual-channel oscilloscope, an adjustable DC output, local controls, a display, and wireless waveform monitoring. Combining these functions creates shared constraints: the analog acquisition path must remain within the ADC input limits, the capture interface must carry both sample streams, and switching power circuitry must not compromise measurement grounding or safety.

The current design baseline uses a dual 14-bit AD9251 converter [1], an ESP32-S3 supervisory controller [2], and an LM5176 four-switch buck-boost controller for the programmable output [3]. The charger draft uses an LTC4015 controller [4]. The AD9251 provides 14-bit CMOS data outputs and a data-clock output per channel; its output-driver supply supports 1.8 V to 3.3 V logic, so the receiving device's I/O bank voltage must be selected before the interface is fixed

[1]. Board layout, decoupling, ground return and exposed-pad connections remain part of the analog signal-chain design [9].

Reference digitizer designs such as Texas Instruments' TIDA-01028 use interleaved RF-sampling ADCs, low-phase-noise clock generation and high-speed serial links at rates far above the PowerScope target [10]. That design is not a direct performance comparator. It illustrates that converter choice, clocking, data capture and board implementation must be developed as one chain. PowerScope is targeted at 10 MS/s per channel, not GHz-bandwidth acquisition.

This paper records the system architecture and preliminary calculations assembled during the PowerScope design sessions. Its contributions are: (1) a system-level division of measurement, processing, user-interface, and power functions; (2) first-pass range scaling and sampling-memory calculations; (3) an initial buck-boost and battery-management design; and (4) a traceable list of unresolved checks and planned verification tasks. The document is a design paper, not a report of completed simulation or laboratory testing.

II. DESIGN METHOD AND REQUIREMENTS

The design was organized by subsystem. Session notes and draft schematics were used to extract target operating ranges, assign functional interfaces, calculate nominal component relationships, and identify checks that cannot be resolved by hand calculations. Calculated values are labelled as analytical estimates. Planned simulation cases are not described as completed tests.

A. System targets

Table I lists the working requirements and the conflicts retained in the source notes. The earlier notes specify a 5 MS/s per-channel sampling target and 1 MHz analog bandwidth, while later acquisition notes and front-end schematics use 10 MS/s per channel and a 2.5 MHz filter target. The newer values are used for the calculations in this paper, but the specification must be frozen before the analog filter and ADC clock are released.

TABLE I
POWERSCOPE WORKING REQUIREMENTS AND DESIGN STATUS

Function	Working target	Basis or unresolved point	Status
Oscilloscope inputs	Two BNC channels, 1 M Ω target, DC coupling, nominal ± 15 V range	Probe compensation, connector shield, grounding and input protection ratings remain open.	Draft
Analog front end	Selectable ± 15 , ± 5 , ± 1.5 , and ± 0.5 V ranges	Range-divider values are calculated; calibration, protection limits and overload behavior remain unverified.	Draft
Signal frequency	100 kHz specified waveform maximum	Earlier notes state a 1 MHz bandwidth target; the later filter blueprint uses 2.5 MHz. These are not yet reconciled.	Conflict
Sampling and ADC	Dual 14-bit AD9251; 10 MS/s/channel current baseline	Earlier notes also state 5 MS/s/channel. The AD9251-20 data sheet lists a 3–20 MS/s conversion range, so 10 MS/s is within the specified range; the earlier 5 MS/s target remains unresolved.	Conflict
Capture and memory	FPGA capture and trigger logic; 50,000 samples/channel	FPGA part, memory technology, I/O-bank voltage, timing closure and record-transfer protocol are not selected.	Draft
Programmable supply	1–15 V, up to 2 A, 30 W maximum	LM5176 synchronous buck-boost; compensation, current thresholds, thermal design and short-circuit cutoff require validation.	Draft
Battery system	Four INR18650-35E cells in 4S1P; 12.0–16.8 V design range	BQ76920 monitor/protection path, pack fuse, cell taps, charge temperature policy and cutoff behavior remain unverified.	Draft
Charger	20 V, 3 A adapter proposal; 16.8 V CV and 1.0 A CC starting target	LTC4015 settings and adapter/system-load budget require calculation and tests.	Draft
User interface	TFT, rotary encoder and buttons; ESP32-S3 and browser monitoring	Browser commands are limited to oscilloscope settings. PSU enable and current-limit operation remain local.	Draft

B. Subsystem partition

The system is divided into five connected groups: analog acquisition, digital capture, user interface, battery and rail distribution, and programmable power output. The analog and digital sections exchange ADC sample buses and timing signals. The MCU supervises display, local inputs, wireless scope settings, and power telemetry. The programmable output has a separate control path with a default-off enable interlock; wireless access is not intended to enable or set the power output.

III. OSCILLOSCOPE ACQUISITION DESIGN

A. Analog signal conditioning

Each channel follows a BNC input, current-limiting resistors, a proposed low-capacitance bidirectional TVS clamp, an input divider, a selectable gain stage, two Sallen–Key filter sections, a THS4551 fully differential driver, and one input of the AD9251. The OPA810 is the proposed amplifier for the gain and buffer stages [5], and the THS4551 is the proposed ADC driver [6]. The CH1 and CH2 drawings share the same functional sequence, with separate components and range selection. The shared ADC is dual-channel; a second ADC is not intended.

The latest integrated CH1 drawing changes the lower divider resistor from an earlier 66.5 k Ω draft to 56.2 k Ω to preserve nominal headroom. With three 15.8 k Ω series resistors, an 887 k Ω upper resistor, and a 56.2 k Ω lower resistor, the total resistance in the divider path is 990.6 k Ω . The nominal ratio is

$$k_{\text{div}} = \frac{56.2}{47.4 + 887 + 56.2} = 0.05673. \quad (1)$$

Thus, a ± 15 V peak input produces approximately ± 0.851 V at the divided node. The lower input ranges are paired with nominal voltage gains of 3, 10 and 30. These values are estimates from the component ratios; switch resistance, amplifier

TABLE II
NOMINAL INPUT SCALING CALCULATIONS

Input range	Divider output (Vpk)	Gain	Output (Vpk)	Status
± 15 V	0.851	1	0.851	Calculated
± 5 V	0.284	3	0.852	Calculated
± 1.5 V	0.0851	10	0.851	Calculated
± 0.5 V	0.0284	30	0.852	Calculated

tolerance, calibration, clipping and protection behavior have not been tested.

The input-protection network is not a certified protection interface. Resistor power and pulse ratings, TVS clamping under the intended transient, leakage, BNC shield bonding, and board return inductance must be verified. The input must never be connected directly to mains voltage. The nominal 1 M Ω input target also requires a probe-compensation design that is not yet present in the schematic.

B. Anti-alias filter

The current schematic uses two Sallen–Key sections with a 2.5 MHz natural-frequency target. The first section uses 1.00 k Ω resistors, 58.81 pF and 68.91 pF capacitors, and a nominal $Q = 0.5412$. The second uses 500 Ω and 1.00 k Ω resistors, 32.48 pF and 249.6 pF capacitors, and a nominal $Q = 1.3065$. The pair is intended to form a fourth-order Butterworth response. For an ideal fourth-order Butterworth low-pass filter,

$$|H(j2\pi f)|^2 = \frac{1}{1 + (f/f_c)^8}. \quad (2)$$

At $f = f_c = 2.5$ MHz, the ideal magnitude is approximately -3.01 dB. At 5 MHz, the ideal attenuation is approximately 24.10 dB. These are mathematical values for the ideal transfer function, not circuit-simulation measurements.

PowerScope — CH2 Analogue Front End

Companion to CH1 draft v0.3 • mirrored analogue path • Channel B input of shared AD9251-20

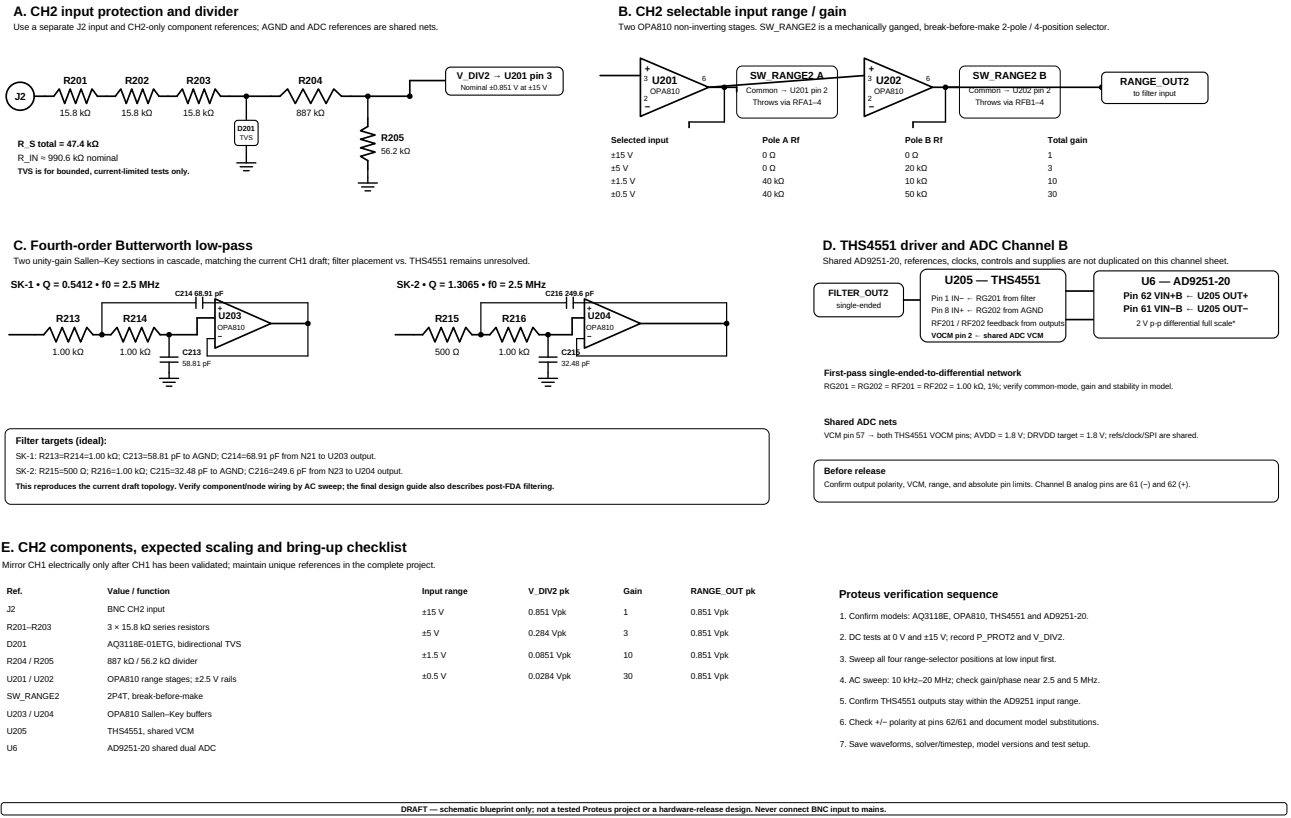


TABLE III
SAMPLING BASELINE COMPARISON

Item	Earlier baseline	Current baseline	Implication
Per-channel rate	5 MS/s	10 MS/s	Must be frozen
Nyquist frequency	2.5 MHz	5 MHz	Changes alias limit
Samples at 100 kHz	50/cycle	100/cycle	Both exceed 2 samples/cycle
2.5 MHz filter corner	At Nyquist	Below Nyquist	No transition band for 5 MS/s
Analog band-width target	1 MHz in earlier notes	2.5 MHz filter corner in later design	Specification conflict

only viable option. A direct-capture implementation should only be reconsidered after verifying bus timing, DMA rate, simultaneous channel capture, trigger behavior, record depth and memory-transfer limits.

For two channels sampled at 10 MS/s and stored at 14 bits per sample, the raw aggregate flow is

$$R_s = 2(10^7)(14) = 280 \times 10^6 \text{ bit/s} = 35 \text{ MB/s}. \quad (3)$$

If samples are stored in 16-bit words, the write rate is 40 MB/s. A record of 50,000 samples per channel at two bytes per sample requires 200,000 bytes, or about 195.3 KiB, before metadata or ping-pong buffering. A 256 KiB buffer is an initial minimum estimate, not a validated memory selection. Transferring full records at 30 records/s would require 6 MB/s of payload bandwidth. These figures define interface requirements; no capture or sustained-transfer measurement has been produced.

The sample count per signal cycle and the first Nyquist zone are described by

$$N_{\text{cycle}} = \frac{f_s}{f_{\text{in}}}, \quad f_N = \frac{f_s}{2}. \quad (4)$$

For the 10 MS/s working rate, a 100 kHz input produces 100 samples per cycle and a Nyquist frequency of 5 MHz. A 6 MHz input lies above Nyquist; its sampled values are also consistent with a negative-frequency 4 MHz sinusoid, so the apparent alias magnitude is 4 MHz. Under the ideal fourth-order Butterworth expression used in (3), the attenuation at 6 MHz is approximately 30.4 dB for a 2.5 MHz cutoff. This value describes the ideal transfer rejection of the component-level circuit.

The session notes contain sampling and aliasing exercises at 10 MS/s and an ideal fourth-order Butterworth response analysis. The raw MATLAB scripts and plots were not included with the files reviewed. Fig. 6 therefore reconstructs the examples from the ideal sine-wave sampling equations and labels them as analytical illustrations, not as a saved MATLAB result, Proteus trace or measurement.

IV. PROGRAMMABLE POWER AND BATTERY DESIGN

A. Buck-boost output stage

The proposed output stage uses the LM5176 synchronous four-switch buck-boost controller [3] to regulate a target range of 1–15 V from a nominal 12.0–16.8 V battery input. The design worksheet uses a 350 kHz switching frequency, a 10 μH inductor, and 100 μF effective ceramic plus 100 μF polymer output capacitance. The inductor, MOSFETs, capacitors, gate network and compensation must be finalized from their actual operating stresses and manufacturer models.

At the maximum output target, $P_{\text{out}} = 15 \times 2 = 30 \text{ W}$. A 90% efficiency assumption gives $P_{\text{in}} \approx 33.3 \text{ W}$, or $I_{\text{in}} \approx 2.78 \text{ A}$ at 12 V. These are sizing calculations, not an efficiency claim. For the 12 V to 15 V boost operating point, the ideal duty ratio is

$$D \approx 1 - \frac{12}{15} = 0.20. \quad (5)$$

With 10 μH and 350 kHz, the first-order ideal inductor ripple estimate is

$$\Delta I_L \approx \frac{V_{\text{in}} D}{L f_{\text{sw}}} = 0.686 A_{\text{pp}}. \quad (6)$$

An estimated 3.12 A peak follows from the 2.78 A average input current plus half the ripple. A 4.5 A minimum saturation-current target was recorded as an initial sizing allowance, not a final inductor approval.

B. Output feedback and protection

The proposed voltage monitor uses a 100 k Ω /22.1 k Ω divider. Its nominal ratio is 0.181, which yields 2.72 V at a 15 V output. The proposed current-monitor path uses a 20 m Ω shunt and an INA240A1 with gain 20. At 2 A, the shunt drop is 40 mV and its nominal dissipation is 80 mW; the current-sense output is about 0.80 V with zero reference offset.

A design mismatch remains: the LM5176 average-current threshold is noted as approximately 50 mV. A 20 m Ω shunt reaches 50 mV at 2.5 A, not 2 A. The shunt therefore does not by itself establish a 2 A average current limit. The controller's CS/CSG peak-current network and the optional ISNS current-limit path must be selected and calculated independently. The secondary comparator and fault latch in the control schematic are intended to request converter shutdown, but their thresholds, response time and fail-safe behavior also require simulation and hardware tests.

C. Battery, charger and system rails

The current battery concept is a four-cell INR18650-35E pack in series (4S1P), with a 16.8 V charge endpoint and a provisional 12.0 V operating-minimum assumption. The notes place a BQ76920 battery monitor/protection function beside a proposed LTC4015 charger interface [8]. The BQ76920 is specified for three to five series cells, so it covers the proposed 4S count; this does not validate the FET topology or protection thresholds [8]. The proposed charger source is an isolated 20 V, 3 A DC adapter, and the initial charge target is 1.0 A constant-current followed by 16.8 V constant-voltage control. The charger configuration, cell-tap network,

POWERSCOPE — DIGITAL ACQUISITION, MCU & USER INTERFACE

Interface schematic blueprint v0.1 • net-level diagram plus verified AD9251-20 digital pin map • not a released PCB netlist

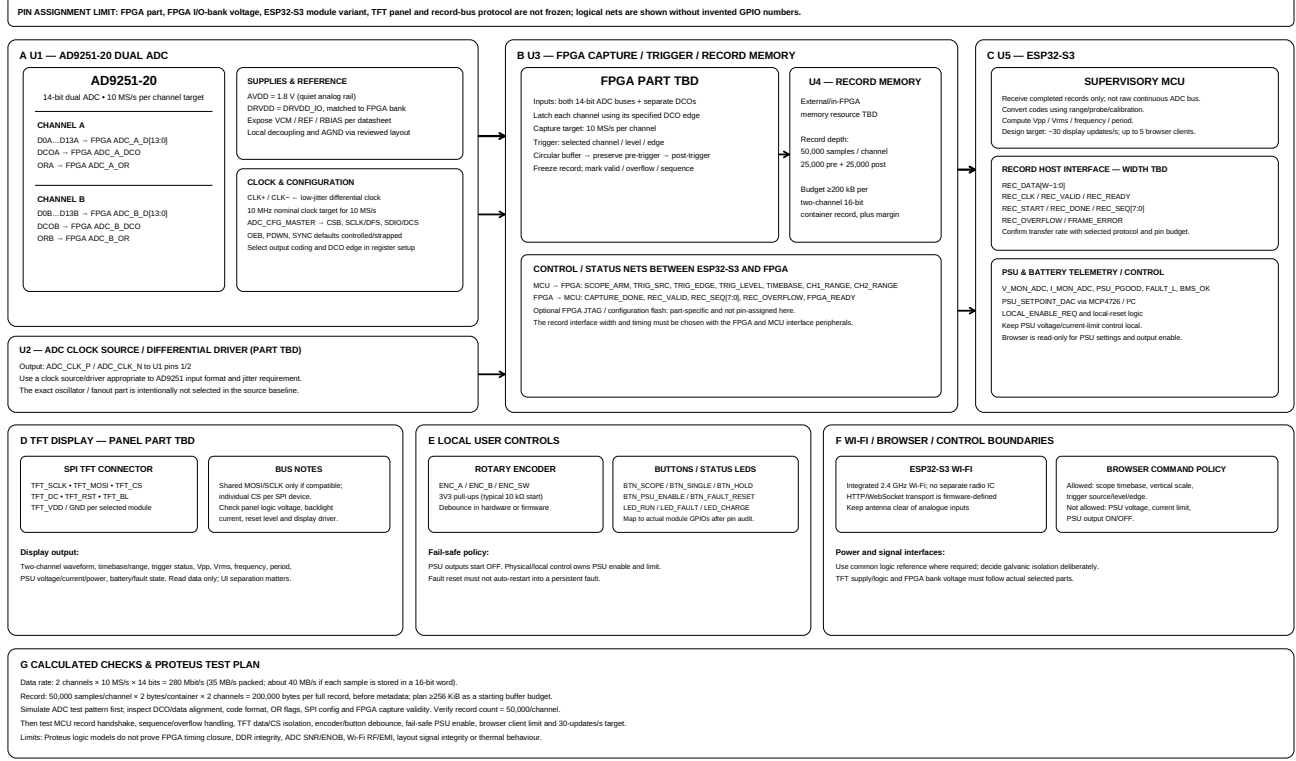


Fig. 5. Digital acquisition, supervisory MCU and user-interface interconnect blueprint. The FPGA family, memory part, FPGA-to-MCU transport, ESP32-S3 module pin map and TFT module are open selections.

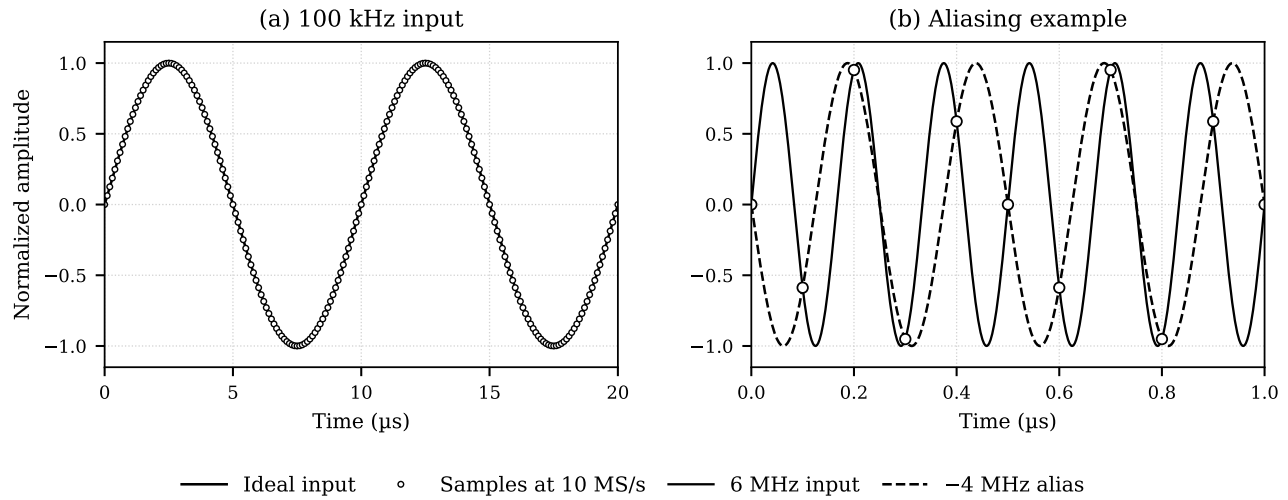


Fig. 6. Analytical sampling examples at 10 MS/s. (a) A 100 kHz input yields 100 samples per cycle. (b) Samples from a 6 MHz input coincide with a phase-reversed 4 MHz alias. The figure is calculated from ideal sine-wave equations and is not hardware evidence.

temperature limits, input current limit and fault cutoffs need to be checked against the cell and controller data sheets before physical use [4].

The distribution draft separates the protected battery bus

from the regulated 5 V, 3.3 V, 1.8 V ADC analog, digital-I/O and analog ± 2.5 V rails. The proposed LMR33630 step-down regulator is one candidate for low-voltage rails [7]. It proposes input overvoltage and undervoltage protection before system

AD9251-20 — DIGITAL PIN MAP FOR FPGA INTERFACE

Package pin numbers are datasheet-derived; the FPGA ball/pin assignments remain TBD until the FPGA part is selected.

LOGIC SUPPLY RULE: DRVDD (pins 10, 19, 28, 37) must match the FPGA input bank voltage, chosen within AD9251 datasheet limits.

CHANNEL A OUTPUTS

D0A = LSB; D13A = MSB; capture against DCOA per timing table.

Pin	Signal	FPGA logical net
27	D0A	ADC_A_D[0]
29	D1A	ADC_A_D[1]
30	D2A	ADC_A_D[2]
31	D3A	ADC_A_D[3]
32	D4A	ADC_A_D[4]
33	D5A	ADC_A_D[5]
34	D6A	ADC_A_D[6]
35	D7A	ADC_A_D[7]
36	D8A	ADC_A_D[8]
38	D9A	ADC_A_D[9]
39	D10A	ADC_A_D[10]
40	D11A	ADC_A_D[11]
41	D12A	ADC_A_D[12]
42	D13A	ADC_A_D[13]
24	DCOA	ADC_A_DCO
43	ORA	ADC_A_OR

CHANNEL B OUTPUTS

D0B = LSB; D13B = MSB; capture against DCOB per timing table.

Pin	Signal	FPGA logical net
6	D0B	ADC_B_D[0]
7	D1B	ADC_B_D[1]
8	D2B	ADC_B_D[2]
9	D3B	ADC_B_D[3]
11	D4B	ADC_B_D[4]
12	D5B	ADC_B_D[5]
13	D6B	ADC_B_D[6]
14	D7B	ADC_B_D[7]
15	D8B	ADC_B_D[8]
16	D9B	ADC_B_D[9]
17	D10B	ADC_B_D[10]
18	D11B	ADC_B_D[11]
20	D12B	ADC_B_D[12]
21	D13B	ADC_B_D[13]
23	DCOB	ADC_B_DCO
22	ORB	ADC_B_OR

CLOCK / CONFIG / CONTROL PINS

1,2	CLK+, CLK-	ADC_CLK_PIN; differential clock
3	SYNC	FPGA sync/control or documented static state
44	SDIO/DCS	ADC_SPI_SDIO or DCS strap; dual function
45	SCLK/DFS	ADC_SPI_SCLK or DFS strap; dual function
46	CSB	ADC_SPI_CSB; active low
47	OEB	ADC_OEB; low enables outputs
48	PDWN	ADC_PDWN; low = normal operation
10,19,28,37	DRVDD	DRVDD_IO; match FPGA I/O bank
0	Exposed padfile	Solder to PCB AGND per datasheet

PIN / ELECTRICAL CHECKS BEFORE PROTEUS

1. AVDD = 1.8 V nominal; DRVDD supported range per datasheet (1.8–3.3 V nominal family).
2. Keep D0, D13 and each DCO close together; load and series damping after layout review.
3. Choose one ADC SPI host only; never connect two active SPI masters to CSB/SCLK/SDIO.
4. If FPGA bank voltage does not match DRVDD, select a level translator after part selection.
5. The AD9251-20 is a 14-bit, dual-channel part; this is one ADC feeding two FPGA buses.
6. Use the DCO edgetime/delay requirements in the datasheet; do not infer timing from drawing.
7. If FPGA is unavailable in Proteus, use behavioural digital-pattern sources to test data capture logic only.

Source: Analog Devices AD9251 Rev. C datasheet, Figure 5 / Table 8 (pin configuration and functions).

Fig. 7. AD9251-to-FPGA signal mapping reference used in the design notes. It is a logical pin-map aid, not a selected FPGA pin assignment or proof of setup/hold timing.

loads. The FPGA I/O bank voltage is still not selected, so the AD9251 digital-driver supply and any level translation cannot be frozen. The exact relationships among BNC shield, analog ground, digital ground, power ground and chassis also remain open.

V. PRELIMINARY RESULTS AND ENGINEERING REVIEW

The outputs obtained so far are analytical estimates and draft interconnection diagrams. Table IV summarizes the numerical results that can be reproduced from the current component values. No oscilloscope waveform, AC-sweep data, converter transient trace, efficiency result, battery charging profile or hardware measurement was available in the records reviewed for this paper.

A. Verification status

The subsystem schematics provide a build sequence for later Proteus work, but they are not native, tested Proteus projects. In particular, the exact device models for the ADC, differential driver, protection devices, buck-boost controller, battery charger and regulators may not be available in the installed simulator. A symbol or simplified behavioral model

cannot establish ADC noise, differential linearity, sample-clock timing, controller loop stability, switching loss, battery safety, PCB parasitics, electromagnetic compatibility or thermal performance. The PCB stage must later verify return paths, decoupling placement and the AD9251 exposed-pad connection using the selected package and manufacturer layout guidance [9].

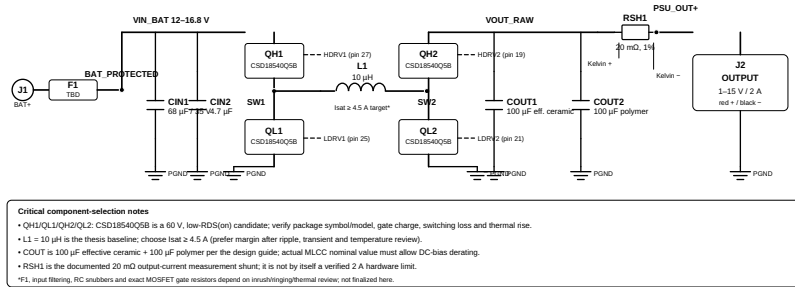
Table V separates current evidence from the tests still required. The planned AC sweep spans 10 kHz to 20 MHz to inspect the filter transfer function and phase. Front-end DC and transient cases should begin with small, current-limited inputs, then approach the defined ranges. PSU testing should begin with a light resistive load and a limited low-voltage source after the compensation and hardware current-limit networks are completed.

B. Unresolved design decisions

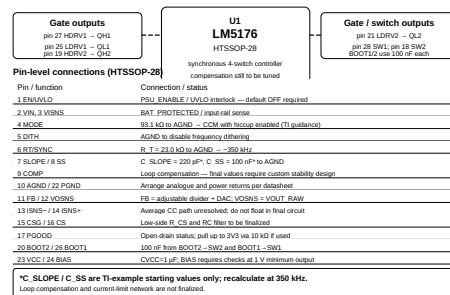
Five decisions should be closed before the design is treated as a single stable baseline. First, select either 5 or 10 MS/s per channel and reconcile the 1 MHz and 2.5 MHz bandwidth targets. Second, fix the anti-alias filter location: the integrated CH1 blueprint places the Sallen–Key sections before the THS4551, while an earlier architecture note describes a filter

Engineering draft v0.1 • 4S Li-ion 12–16.8 V • LM5176 synchronous 4-switch topology • 1–15 V / 2 A output target

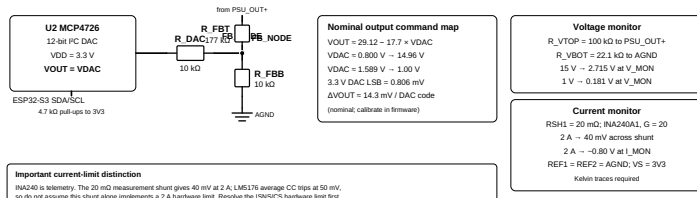
Use the exact LM5176 topology: two half-bridges and one inductor between SW1 and SW2. Gate lines are labelled by controller pin function



Use HTSSOP-28 package pin numbers from the TI datasheet.



The ESP32-S3 has PC but no on-chip DAC: use an external DAC/voltage command for analog FB setpoint



Parameter	Calculation / value	Design note
Output target	1-15 V, 0-2 A	from PowerScope guide
Maximum output power	$15\text{ V} \times 2\text{ A} = 30\text{ W}$	worst-case output point
Input current (assumed $\eta=90\%$)	$30\text{ W} / (0.90 \times 12\text{ V}) = 2.78\text{ A}$	at 12 V test minimum
RT resistor @ 350 kHz	$(1/350\text{K}) - 150\text{ nS} / 115\text{ pF} = 22.99\text{ k}\Omega$	choose 22.0 k Ω , 1%
Boost ripple at 12 V ~ 15 V	$D=1-12015/(0.20\text{ }\mu\text{S} \times 115\text{ pF} \times 350\text{K})=0.686\text{ A}$	ideal CCM estimate
Peak current estimate	$I_{\text{IN}}=2.78\text{ A}$, D pins $=2.78 \times 0.6862 = 3.12\text{ A}$	marg in lost needed
Voltage monitor ratio	$22.1\text{ k} / (100\text{K}+22.1\text{ k})=0.381$	$15\text{ V} = 2.715\text{ V}$
Output current shunt	$2\text{ A} \times 20\text{ m}\Omega = 40\text{ mV}$, $P = I^2R = 0.32\text{ W}$	choose $\omega 25\text{ W}$, Vishay

R_FFBT / R_DAC equation is a provisional quadratic FB method; top compensation & DAC f/safe need a custom stability check.

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Ref.	Value / part	Dataset basis	Role / status
U1	LM575C-AD500-28	T1 LM575C datasheet, Rev. D	Controller / switch boost
U1,PH1,PH2,LIQ1,2	CS20A48QDS-48 (varidatas)	T1 MOSFET-48QDS datasheet	90 V MOSFET, ceramic thermalpad
LIQ3	10 μ F, fast, target 45.5 A	Inductor vendor: datasheet T8D	DCR and saturation at temperature required
CO1U1,CO2	68 μ F / 35 V + 4.7 μ F / 100 mF	Capacitor MPN T8D	Input/bypass bypasses operational
CO1U1,COU1,2	100 μ F / effective ceramic + 100 μ F polymer	Capacitor 100F T8D	Avoid MLCC: DC-bias derating
U2	MP4726S, 12-bit 3C DAC (proposed)	Monorchip MCP47064T164T28TDS	3V3 VDD; verify Protes model
U3	INA240A1, SOC-8	T1 INA240S datasheet	Q=20 VHV; VDS=7.5-5.5 V
RSH1	20 m Ω , 5%, 20 W, Kelvin	Shunt resistor MPN T8D	Measure shunt, not 2A limit
S, F, R1, MODE	29.53 MHz, 1% 10 Ω	T1 LM67510 datasheet	350 MHz, CCM / H-bridge
R1, R2, R3, F1,PH1, PH2, PH3, PH4, PH5, PH6, PH7, PH8	33 Ω , 1%, 0.25 W, 10 Ω 1/4 W	Discreet: provisional values	Discreet: provisional values
R1, VTOP, VBOT	100 Ω / 20 Ω 1/4 W	Power/Sense baseline	Output voltage (injection to MCU)
C, SSC, SSC2	100 nF / 220 μ F	T1 example start values	Recalculate and verify for 350 kHz

Protes may build manufacturer transfer models for the controller, MOSFETS, DAC or current sense amplifier. Recycle every subdatasheet.

Official data: <https://www.ti.com/lit/ds/lm575.pdf>, <https://www.ti.com/lit/ds/cs20a48qds.pdf>, <https://www.ti.com/lit/ds/mcp47064.pdf>, <https://www.ti.com/lit/ds/ina240.pdf>, <https://www.ti.com/lit/ds/lm67510.pdf>

- 1 **Begin with a bounded source**
Use a battery-equivalent DC source swept 12.0-16.8 V. Set output enable OFF initially; never connect the simulation to mains.
- 2 **Check controller model availability**
If LM5176 has no usable model, use a validated averaged/behavioral buck-boost model for system-level plots. Do not claim switch-mode physics from an ideal averaged model.
- 3 **Low-risk power-stage tests**
Start with 5 V / 0.1 A load then increase gradually. Record VIN, VOUT, SW/SW2, inductor current, and startup.
- 4 **Transient evidence**
Test output commands at 1 V, 5 V, 12 V and 15 V; load steps and battery steps; quantify overshoot, ripple and settling.
- 5 **Current and voltage telemetry**
Check V_MON divider outputs and IN4500 output vs 0.5 A, 1 A and 2 A. Simulate switch voltage with 4-ns/10-ns series wiring.

Fig. 8. Preliminary LM5176 power-converter schematic. The 1–15 V, 2 A output is a design target. Compensation, thermal behavior, switching waveforms and current-limit thresholds have not been validated.

TABLE IV
CALCULATED VALUES FROM THE CURRENT DESIGN BASELINE

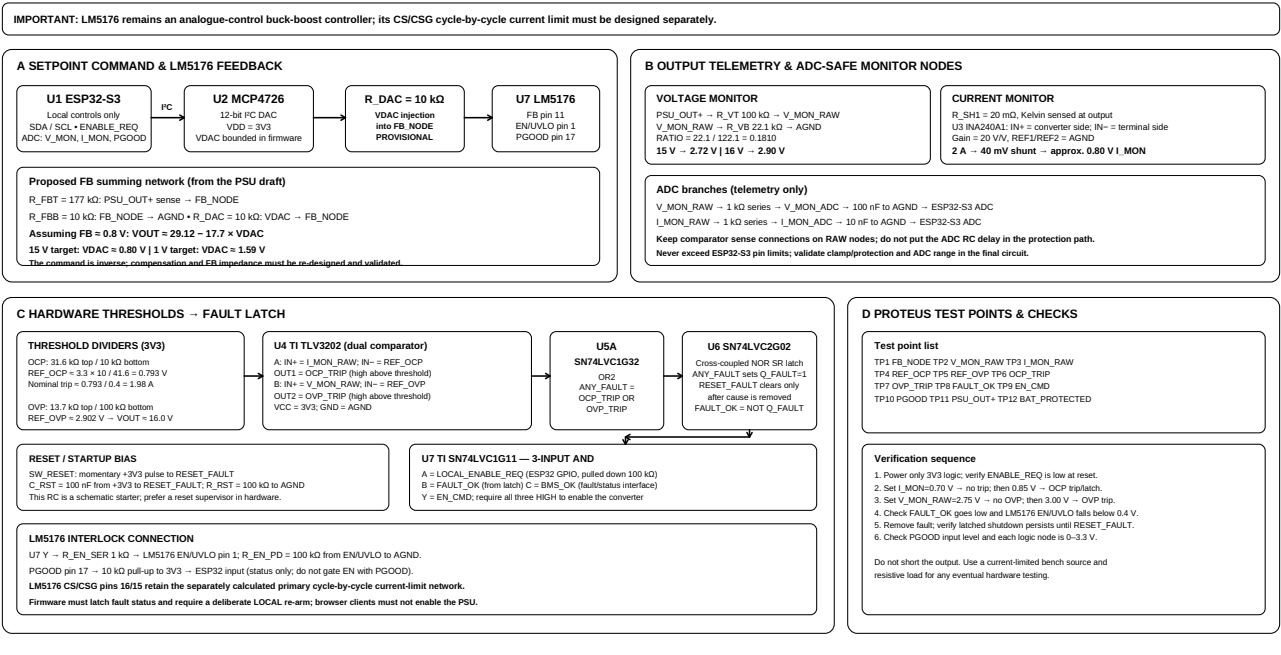
Calculation	Inputs	Calculated value	Evidence
Input divider ratio	47.4 k Ω series, 887 k Ω upper, 56.2 k Ω lower	$k_{div} = 0.05673$; ± 15 V becomes ± 0.851 Vpk	Analytical
Range matching	± 5 , ± 1.5 , ± 0.5 V ranges	Nominal gain settings 3, 10, 30; about 0.851 Vpk after scaling	Analytical
Ideal filter	Fourth-order Butterworth, $f_c = 2.5$ MHz	-3.01 dB at 2.5 MHz; -24.10 dB at 5 MHz	Analytical
Aggregate ADC payload	Two channels, 10 MS/s, 14 bits	280 Mbit/s, equivalent to 35 MB/s packed	Analytical
Record storage	Two channels, 50,000 samples/channel, 16-bit storage	200,000 bytes per record, about 195.3 KiB	Analytical
Full-record delivery	200,000 bytes per record, 30 records/s	6 MB/s payload, before protocol overhead	Analytical
Maximum PSU output	15 V, 2 A	30 W	Target arithmetic
PSU input estimate	30 W output, assumed 90% efficiency, 12 V input	33.3 W input; 2.78 A average input current	Assumption based
Boost inductor ripple	12 V to 15 V; 10 μ H; 350 kHz	Ideal duty ratio 0.20; $\Delta I_L \approx 0.686$ A pp	Analytical
Current shunt	20 m Ω at 2 A	40 mV drop, 80 mW dissipation, 0.80 V after gain 20	Analytical

after the differential driver. Third, redesign and verify both average and cycle-by-cycle current limiting so the 2 A target is not inferred from a telemetry shunt alone. Fourth, select the FPGA, memory, module pin map and digital voltage

levels. Fifth, complete the battery protection, charge policy, grounding and enclosure safety design. These items are not resolved by the figures in this paper.

POWERSCOPE — PSU CONTROL & PROTECTION

ESP32-S3 supervisory interface to LM5176 • draft schematic blueprint v0.1 • values requiring verification are explicitly marked



DESIGN LIMITATIONS

- INA240A1 is a monitor path (400 kHz bandwidth, ~9.6 μs settling); it is not the primary fast short-circuit limiter.
- LM5176 cycle-by-cycle CS/CSG network and any 2 A average-current loop must be calculated for the selected MOSFET/inductor topology.
- FB-DAC injection is provisional: re-check closed-loop stability, min/max command clamp, startup, DAC reset behaviour and OVP interaction.
- All signal names are logical nets; exact package footprints and logic-gate pin mappings must be checked against selected datasheets and Proteus models.

Fig. 9. PSU setpoint, telemetry and fault-control schematic. Hardware current limiting still depends on a correctly designed LM5176 current-sense network; the MCU and fault comparator do not replace the controller’s peak-current protection.

TABLE V
EVIDENCE STATUS AND NEXT VERIFICATION STEPS

Item	Current evidence	Required check	Status
CH1/CH2 DC transfer	Nominal divider/gain calculations and draft schematics	Simulate 0 V and bounded positive/negative inputs; record every range, internal node voltage, clipping and recovery	Not run
Analog filter	Ideal transfer function only	AC sweep 10 kHz–20 MHz; verify 2.5 MHz gain, 5 MHz attenuation, phase and peaking with actual models	Not run
ADC interface	AD9251 logical pin map and throughput calculation	Choose FPGA, I/O bank and memory; verify DCO timing, bus capture, record length and sample ordering	Not run
PSU regulation	First-pass component values and ideal calculations	Verify loop compensation, 1/5/12/15 V setpoints, line/load changes, ripple, startup and shutdown	Not run
PSU protection	Draft comparator/latch logic; shunt mismatch identified	Verify 2 A shutdown, peak current limit, OVP/OCP thresholds, latch reset and default-off behavior	Not run
Battery and charger	4S1P architecture and charger settings proposed	Validate cell taps, BMS MOSFET path, fuse, temperatures, CC/CV transition, input current limit and fault cutoff	Not run
System rails	Proposed buck/LDO rails and input protection	Test 12.0–16.8 V input range, startup sequence, load steps, rail accuracy and regulator temperature	Not run
Hardware prototype	No bench data in reviewed records	PCB inspection, safe low-voltage bring-up, calibrated measurements, thermal review and fault tests	Not run

VI. CONCLUSION

This paper consolidates the present PowerScope design into an IEEE conference-style manuscript. The project now has a documented functional architecture, draft analog front ends for both oscilloscope channels, a dual-ADC capture plan,

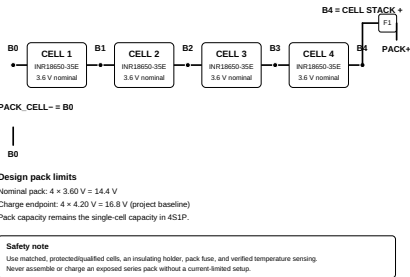
a preliminary buck-boost output stage, battery and charger interfaces, system rail distribution, and a proposed control and protection path. Hand calculations establish nominal range scaling, ideal filter response, sample throughput, record storage and first-pass converter loading. The work remains at the

PowerScope — 4S Battery Pack and BMS Interface

Engineering draft v0.2 • 4S1P INR18650-35E • BQ76920 20-TSSOP • cell taps, monitoring, and low-side protection path

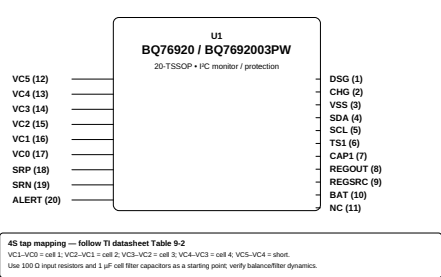
A. 4S1P lithium-ion cell stack

Each cell is one INR18650-35E; series taps B0-B4 are separate sense points.



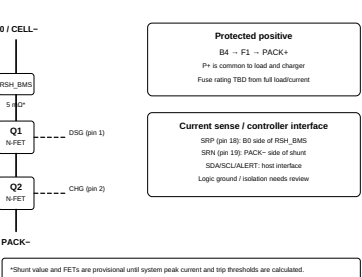
B. BQ76920 cell monitor and filter interface

Candidate exact variant: BQ7692003PW (3.3 V REGOUT option); verify order code/model.



C. Pack protection and current path

Low-side back-to-back N-MOSFET arrangement shown as a design option.



D. Cell-input filter and support network

Tap wiring (each sense input passes through its own series resistor before the IC pin):

Ref.	Value / part	Connection / design instruction
RVC0	100 Ω	B0 → VCO pin 17
RVC1	100 Ω	B1 → VC1 pin 16
RVC2	100 Ω	B2 → VC2 pin 15
RVC3	100 Ω	B3 → VC3 pin 14
RVC4	100 Ω	B4 → VC4 pin 13
JMP1	0 Ω / direct short	VCS pin 12 → VC4 pin 13 (4S configuration)
CCD-CCA	1 μF each	Cell-differential filter capacitors across adjacent filtered taps; CCD from VCO node to VSS per TI topology
R_BAT_F	100 Ω provisional	B4 / pack tap to BAT pin 10; implement D_BAT and C_BAT exactly as TI Figure 9-1
D_BAT	1N4148 (candidate)	Conventional PN diode from tap-cell input toward BAT supply node; orientation per TI figure
C_BAT	10 μF provisional	BAT power-filter capacitor to VSS; use datasheet reference values/ranges
C_CAP1	1 μF	CAP1 pin 7 to VSS
C_REGOUT	4.7 μF	REGOUT pin 8 to VSS; required even if REGOUT not used as rail
NTC_BMS	10 kΩ @ 25°C	Cell-pack thermistor to TS1 pin 6 with the TI-recommended boot/thermistor network
PC	3.3 V logic	SDA pin 4, SCL pin 5; pull-ups on chosen rail; decide ground reference/isolation before tying to ESP32

Important application constraints

- BQ76920 hardware has configurable OV/UV/OC/OSCD features; thresholds, delays and boot/thermistor sequence must be configured.
- TI requires BAT power pin filtering and conventional diode protection; use official Figure 9-19-2 wiring, not guessed pin-only wiring.
- The host may sit at PACK- while U1 VSS is B0; do not wire shared PC directly until ground and isolation are resolved.
- 4S cell voltages, current short polarity, balance-cell restrictions and MOSFET body-diode direction must be reviewed.

Reference: TI BQ76920 datasheet Rev. 1, Sections 6, 9.1.7–9.1.8 and Fig. 9-1.

E. Connectors, nets and validation plan

Ref.	Pins / net	Role	Notes
J_BAT	B4, B3, B2, B1, B0	Battery stack / taps	5-wire balance harness plus power terminals; keyed connector strongly preferred
J_PACK	PACK+, PACK-	Protected external pack port	Load/charger positive to fused B4; negative through the BMS switch path
J_HOST	SDA, SCL, ALERT, VCC, GND	ESP32-S3 supervisory host	PC levels and ground reference must be validated; isolates/level-shift if grounds differ
J_NTC	NTC_BMS	Pack temperature	Place thermistor thermally against cell body; separate BMS/charger NTC networks
J_CHG	CHG_N+, CHG_N-	To LTC4015 charger output	Do not bypass the BMS charge path; LTC4015 does not replace cell-level protection
TP1–TP5	B0–B4	Cell tap test points	Measure each cell differential, not just stack total
TP6	SRN–SRP	BMS current sense	Check polarity during charge/discharge and verify threshold trip calculations

Proteus build sequence	
1	Build cell stack with four isolated cell DC sources or cell models; label B0–B4. Never place ideal voltage sources that short a cell through the tap filters.
2	Wire VCO–VC4 through input resistors and filter capacitors; short VCS–VC4 for four cells as TI Table 9-2 explicitly specifies.
3	Add BQ76920 supply/boost/NTC network following TI Figure 9-1. Use a functional model only if its register/protection behavior is real.
4	Add short and back-to-back FETs; initially test with current-limited sources and a small load. Verify BMS sense polarity.
5	Apply per-cell overvoltage/undervoltage and overcurrent fault simul.; record ALERT and CHG/DSG outputs and actual model limitations.
6	Document all model substitutions. No diagram or behavioral block proves cell thermal safety, fault interruption, balancing accuracy or pack certification.
This is an engineering draft, not a certified pack protection design; complete the thermal/current/short-circuit review before hardware.	

Fig. 10. 4S battery monitoring and protection draft. Cell monitoring, switching devices, fuse coordination, balance behavior, temperature sensing and pack cutoff behavior are unvalidated.

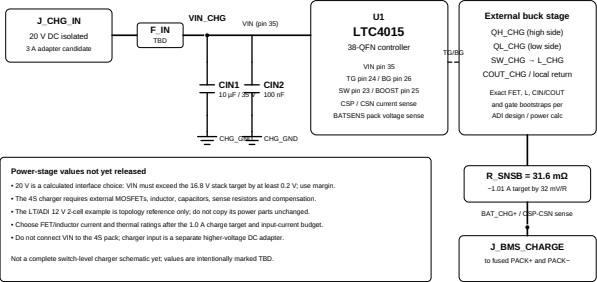
design and integration stage. No successful Proteus run or hardware measurement is reported. The next engineering work is to freeze the rate and bandwidth requirements, close the current-limit and grounding designs, select the unassigned digital components, and capture reproducible simulations before hardware construction.

PowerScope — LTC4015 4S Charger Interface

Engineering draft v0.2 • 20 V external buck-charger input • 4S Li-ion fixed 4.2 V/cell • BQ76920 remains the cell-level protection monitor

A. Charger input and synchronous buck power train

LTC4015 is a buck charger; input must remain above 4 × 4.2 V plus headroom.



B. Calculated cell-count / chemistry settings and charge target

Parameter	Value / setting	Design note
Battery	4S1P Samsung NRI8650-35E	Pack capacity equals one cell; 4 cells in series
Chemistry selector	CHEM1 = H, CHEM0 = H	Fixed Li-ion, 4.2 V/cell per LTC4015 table
Cell count selector	CELLS2 = L, CELLS1 = L, CELLS0 = Z	4 cells per LTC4015 Table; open = three-state Z
Charge voltage	4 × 4.2 V = 16.8 V	Matches PowerScope guide charge endpoint
Adapter headroom	VIN ≥ VBAT + 0.2 V; select 20 V	LTC4015 internal constraints; practical margin required
Chosen charge current	1.0 A provisional	Near 1.02 A cell cycle-life current; thermal validation needed
Battery-current sense	R_SN5B = 32 mV / 1.0 A = 32 mΩ	Choose 31.6 mΩ, predicts about 1.01 A nominal
R_SN5B dissipation	PR = 1.02² × 0.0316 = 0.032 W	Use 20.25 W with low TCR and suitable Kelvin layout
Thermistor	NTC 10 kΩ at 25°C (candidate)	NTC/BAS / NTC network; choose exact B-value and temperature table
Input current limit	RSNSI and CLP/CLN network TBD	Set for adapter capability and any system load sharing

Datasheet rules

LTC4015 can support 4 Li-ion cells and selects a total pack algorithm only; it does not measure each cell or balance the stack. BQ76920 must remain in the battery protection path; configure protections and charge enable/fault response.

C. LTC4015 pin-level wiring table (38-QFN top view)

Use actual pin numbers when creating the Proteus symbol; verify the exposed pad is GND.

Pin / function	Connection	Purpose / review
1 CELLS1	GND / L	4-cell selector
2 CELLS2	GND / L	4-cell selector
38 CELLS0	OPEN / Z	4-cell selector
36 CHEM0	INTVCC / H	fixed Li-ion 4.2 V/cell
37 CHEM1	INTVCC / H	fixed Li-ion 4.2 V/cell
35 VIN	VIN_CHG 20 V	local ceramic bypass; OVP protection TBD
3 DVCC	3.3 V logic	IC logic rail, reference to host
4 SCL / 5 SDA	Host IC	pull-ups to DVCC; ground relationship must be finalized
6 SMBALERT	Host interrupt	open-drain pull-up to DVCC
7 S0ND / 14 GND / 39 EP	charger return / PCB ground	exposed pad to ground plane per datasheet
8 UVCLFB	input current limit loop	divider/current-limit config TBD
9 VCI / 10 RT	control / timer programming	implement values per LTC4015 datasheet procedure
11 NTC / 12 NTCBAS	battery thermistor	NTC 10 kΩ @25°C candidate
18 BATSENS	Battery voltage sense	sense PACK+ relative to charger return
19 CSIN / 20 CSP	R_SN5B 31.6 mΩ	battery charge current sense pair
15 CSIPM5 / 16 CCREFM / 17 CCREFP	current-reference network	per charger datasheet; not fully calculated
21 MPPT / 13 EQ	GND / disabled if not used	confirm allowed unused pin state
22 2P5VCC	local capacitor	decouple per datasheet
23 SW / 24 TG / 25 BOOST / 26 BG	external synchronous buck stage	MOSFET/inductor design pending
27 DRVCC / 28 INTVCC	diver/frog supply	decouple; follow datasheet application circuit
29 OUTFRET / 30 SYSMS / 31 SYS	power-path management	system operating while charging remains unresisted
32 CLN / 33 CLP / 34 INFET	input current sense / front-end FET	RSNSI and input path require final design

Datasheet: Analog Devices LTC4015 Rev. B, pin configuration and Cells Selection / Chemistry Selection sections.

D. Battery/charger connections and Proteus test plan

Interface	Nets	Connection / constraint
J_CHG_IN	VIN_CHG+, VIN_CHG-	Separate 20 V DC adapter input; use isolated low-voltage supply only
J_PACK	PACK+, PACK-	LTC4015 charger output pins through pack charge path; do not bypass BMS FETs
BMS - Charger	P+, P-, NTC, FAULT, / ENABLE	Charge inhibit on BMS fault; exact hard-wire fault interlock is a system design item
IC host	SDA/SCL/SMBALERT	Do not directly pin LTC4015 bus until ground references are agreed
NTC_BMS vs NTC_CHG	Separate thermistor networks	May sense same physical cell region but must not electrically share bias pins
System while charging	SYS power-path output	Not assumed; validate system load and charger headroom separately

Proteus validation steps

- 1 Start with four cell emulators at 3.0–4.2 V each; verify B0–B4 and every differential cell voltage.
- 2 Verify pin voltages and VCS–VC4 short. Test ALERTCHG/DSD only with a model that supports its registers.
- 3 Use 20 V input, 12–16.8 V stack, 1.0 A target and no system load. Capture CC-to-CV transition.
- 4 Test NTC open/short, cell OCV/V, charger loss, reversed input and BMS FET off-response; this is not safety proof.
- 5 Check RSNSB >32 mV at 1 A; separately validate input-current limit via RSNSI/CLP/CLN.
- 6 Log substitutions, solver settings, sources/loads and fault plots. Without an LTC4015 model, label CC/CV behavior behavioral/simulated.

Do not charge a physical pack until cell-match, thermal sensing, current limits, cutoff and grounding have been verified.

Fig. 11. Proposed LTC4015 4S charger interface. The 16.8 V endpoint and 1.0 A charge target are preliminary settings; no charge-cycle result is available.

POWERSCOPE | SYSTEM POWER DISTRIBUTION & PROTECTION

Design draft Rev A | 4S Li-ion: 12.0-16.8 V | based on project rail names and manufacturer starter circuits

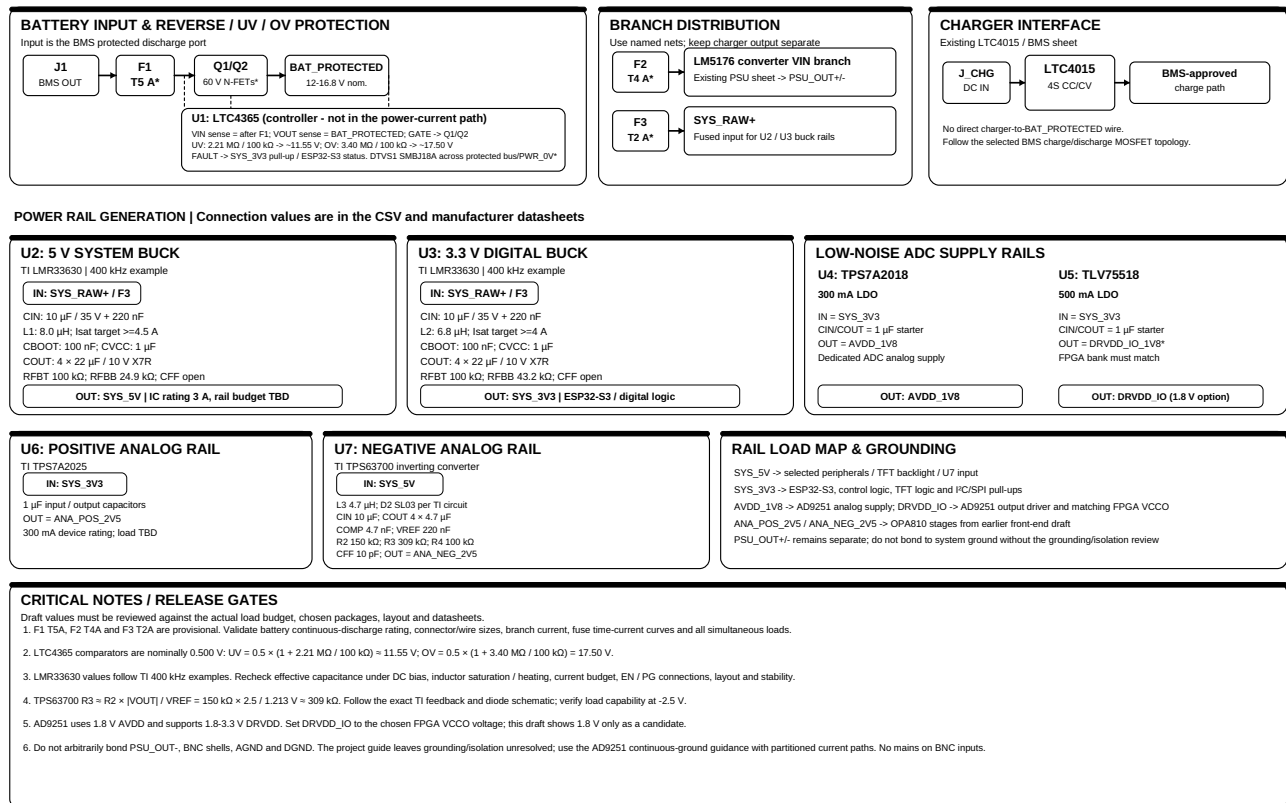


Fig. 12. System power distribution and input-protection blueprint. Fuse values, external MOSFETs, converter models, power budgets and grounding are provisional.

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