

Testing for a Dead-Time Threshold in Class-D Amplifier Distortion: An LTSpice Simulation Study

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Abstract:

Class-D Amplifiers create high power efficiency by rapidly switching their output between two supply rails, as long as the two switches are not conducting at the same time. If both were conducted at the same time, it would result in a short circuit known as shoot-through. To prevent this, an interval called dead-time is included between the switching transitions. Longer dead-time would generally increase total harmonic distortion (THD). This study hypothesized that THD would remain relatively flat at small dead-time values then rises sharply past a critical threshold, producing a nonlinear “knee.” A half-bridge Class-D output stage using IRFH5302D MOSFETs was simulated in LTSpice, with pulse-width modulation (PWM) generated by comparing a 1kHz audio signal against a 50 kHz triangle carrier. The circuit ran on 15V supply rails (+/-) and drove an LC output filter with an 8 Ω resistor load. Dead-time was swept from 5ns to 200ns in 5ns increments, resulting in 40 simulation runs, and THD at the filtered output was measured with LTSpice’s Fourier Analysis. THD stayed narrow with a range of 8.44% to 8.46% throughout the entire sweep, with no threshold behavior, making the hypothesis not supported. This suggests that the simplified model which used: an idealized gate drive, a limited dead-time range, and a fixed resistive load, is mostly resistant to any threshold that exists in the hardware. Further work should extend the dead-time range and include a realistic gate driver.

Keywords: Class-D Amplifier, Dead-Time (DT), Total Harmonic Distortion (THD), Shoot-Through, Pulse-Width Modulation (PWM), Half-Bridge, LTSpice, Power MOSFET

1. Introduction

Class-D amplifiers are used widely in modern audio devices - smartphones, speakers, and other electronics - due to their high power efficiency compared to linear amplifiers [1]. While traditional amplifiers operate continuously, class-D amplifiers rapidly switch the output between two supply voltage rails using complementary switches. A pulse-width modulation (PWM) is used to encode the input signals while the switches are transitioned. A low pass filter then recovers the amplified signal by averaging the switching waveform [1]. Switches are mostly fully on or fully off, meaning that little energy is dissipated. This makes the Class-D approach significantly more efficient than those that rely on a continuous voltage output (Figure 1).

A design constraint for Class-D amplifiers is that two switches should never conduct simultaneously. If two switches are conducted at the same time, a direct short circuit would occur between the supply rails, also known as shoot-through. To prevent this, a small forced delay called dead-time would need to be introduced between the switch turning off and on [1] (Figure 2). While integrating dead-time

reduces the safety issues, it is also known to introduce distortion to the output, due to voltage not being determined by the intended switching pattern [1]-[3].

The relationship between dead-time and distortion is measured as total harmonic distortion (THD) [4]. THD is often linear in common designs, meaning that distortion incrementation is proportional with the dead-time while dead-time increases. In this study, it was hypothesized that this relationship would not be linear; the THD would rather remain constant among the small dead time values then rise sharply once a certain threshold was exceeded. This would produce a nonlinear “knee” in the THD vs. dead-time relationship rather than a smooth, linear relationship.

Understanding whether this nonlinear behavior exists determines if distortion remains minimal within the “safe” range of dead-time values. Designers could use this to select dead-time values that protect against shoot-through without overtly compromising the audio, rather than just a strict linear cutoff [1].

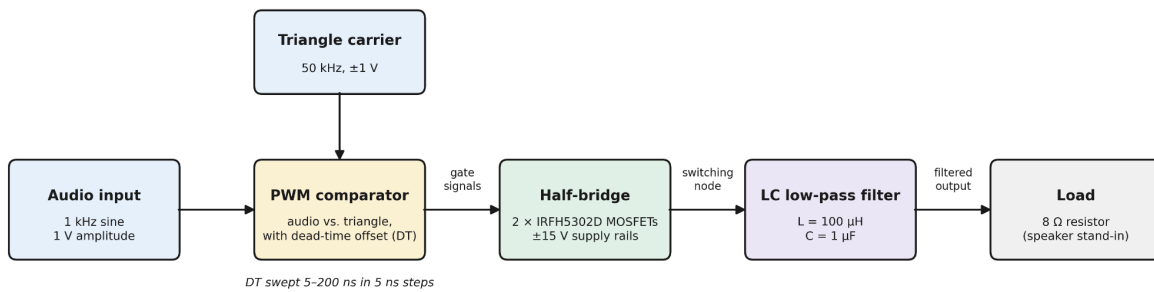


Figure 1. Block diagram of the simulated Class-D amplifier

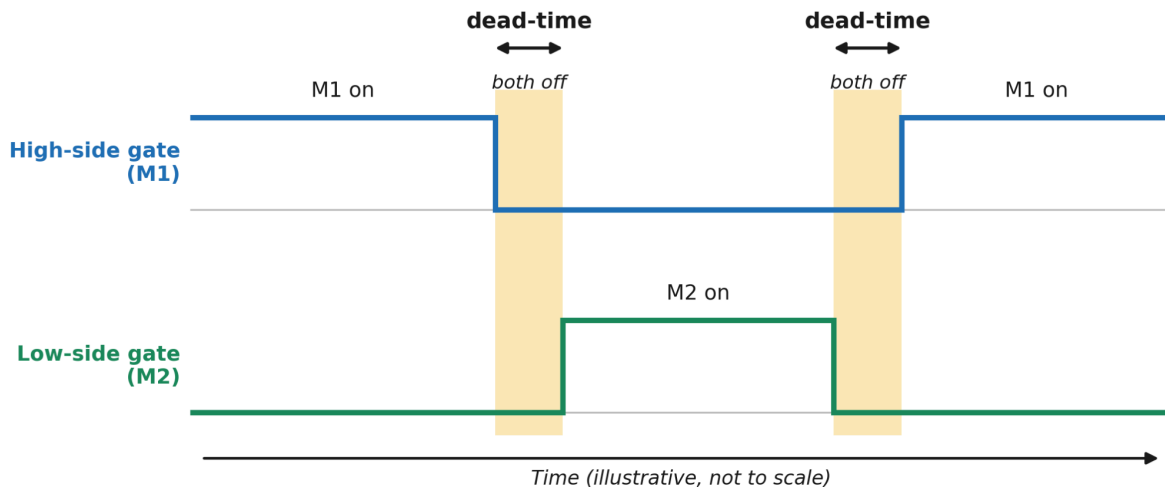


Figure 2. Gate signals of the high-side (M1) and the low-side (M2) MOSFET's with the dead-time intervals (shaded) during which both are off

2. Methods

A half-bridge Class-D Amplifier circuit was designed and simulated in LTspice version 26.0.2 [6] (Figure 3). It consists of two N-channel power MOSFETs (IRFH5302D, rated for 30V with an on-resistance of 2.0 mΩ) [5], with the high-side MOSFET's drain connected to +15V of the circuit's

power supply and source connected to the switching node, and the low-side MOSFET's drain connected to the switching node and source connected to -15V of the supply.

A behavioral voltage source was used to generate Pulse-width modulation (PWM). This was done by comparing a 1 kHz sinusoidal audio signal (amplitude 1 V) to a 50 kHz triangular carrier wave (amplitude ± 1 V). The high-side MOSFET's gate was driven high when the audio signal exceeded the triangle wave (Equation 1a), and the low-side gate was driven high when the triangle wave exceeded the audio signal (Equation 1b). Dead time - a time during which neither MOSFET conducts - was introduced into this logic as a voltage offset (Equation 2).

To recover the amplified audio signal from the switched waveform, the switching node was passed through a second-order LC low-pass filter ($L = 100 \mu\text{H}$, $C = 1 \mu\text{F}$) with an 8Ω resistor, resembling a simplified speaker.

40 simulations were run using LTspice's directive to sweep dead-time from 5ns to 200ns in 5ns increments [6]. A 4ms transient simulated for each dead-time value, and total harmonic distortion (THD) at the 1 kHz fundamental was computed at the filtered output using LTspice's built-in Fourier analysis. THD is defined in Equation 3 [4], and the total THD value reported by LTspice is the figure used through this paper. All component values are listed in Table 1, and the symbols of the equations are listed in Table 2.

Table 1. List of all components used for the Class-D amplifier circuit in the LTSpice digital simulator

Component	Value
MOSFETs	IRFH5302D (30V, $R_{on} = 1.8\text{m}\Omega$)
Supply rails	$\pm 15\text{V}$
Audio signal	1kHz, 1V amplitude
Triangle carrier	50kHz, $\pm 1\text{V}$ amplitude
Output filter	$L = 100\mu\text{H}$, $C = 1\mu\text{F}$, $R = 8\Omega$
Dead-time range	5ns–200ns (5ns steps, 40 runs)
Simulation length	4ms transient per step

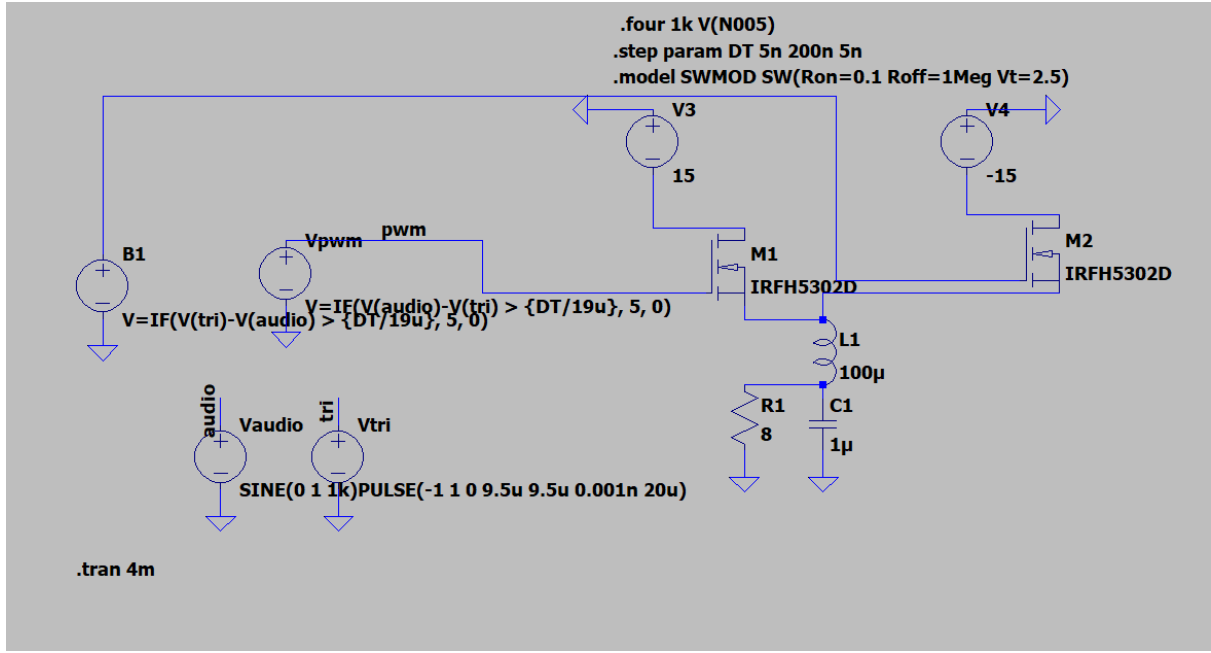


Figure 3. LTSpice schematic of the half-bridge output stage

$$V_{G,HS}(t) = 5 \text{ V if } v_a(t) - v_c(t) > V_{th}, \text{ otherwise } 0 \text{ V} \quad (1a)$$

$$V_{G,LS}(t) = 5 \text{ V if } v_c(t) - v_a(t) > V_{th}, \text{ otherwise } 0 \text{ V} \quad (1b)$$

$$V_{th} = \frac{DT}{19 \mu s} \quad (2)$$

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \dots + V_N^2}}{V_1} \times 100\% \quad (3)$$

Table 2. Symbols that are included in Equations 1-3

Symbol	Meaning
$v_a(t)$	Audio input signal (1 kHz sine, 1 V amplitude)
$v_c(t)$	Triangle carrier (50 kHz, ± 1 V)
V_{th}	Threshold voltage set by the dead-time parameter (V)
DT	Dead-time parameter, in seconds, used as a numeric value (swept 5–200 ns)
$V_{G,HS}, V_{G,LS}$	Gate-drive voltage of the high-side and low-side MOSFET
V_1	Amplitude of the 1 kHz fundamental at the filtered output
V_n	Amplitude of the nth harmonic ($n \times 1$ kHz); N is the highest harmonic included

3. Results

The original hypothesis was that the THD would stay relatively flat across the dead-time values, then rise sharply past a threshold (making a “knee” shape). But during the actual data collecting process, THD did not behave as predicted. With a total range of approximately 0.02 percent points, no smooth increase/decrease nor sharp threshold stayed consistent during the sweep – the THD was roughly flat and narrow as dead-time increased from 5ns to 200ns. The switching node and the filtered output as shown in Figure 4, and the total THD for each dead-time value is plotted in Figure 5 and listed in Table 3.

- Minimum THD: 8.441188% (at DT = 25ns)
- Maximum THD: 8.463662% (at DT = 125ns)
- Total range: 0.022474%
 - Values fluctuated around this narrow area across all 40 steps
 - No consistent increase or decrease patterns

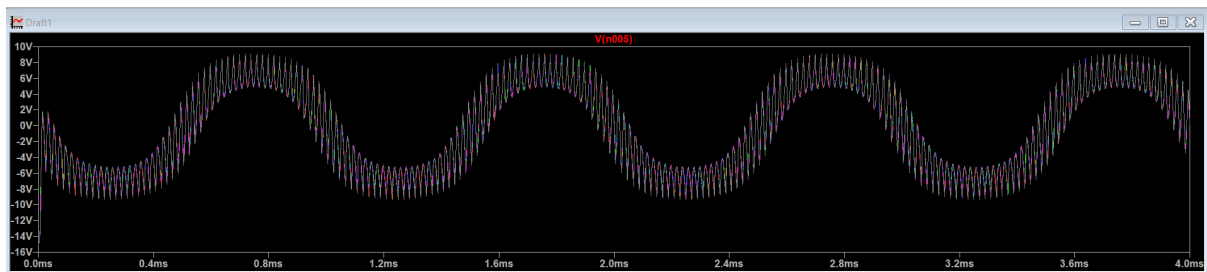


Figure 4. Simulated switching node and filtered output voltage over time

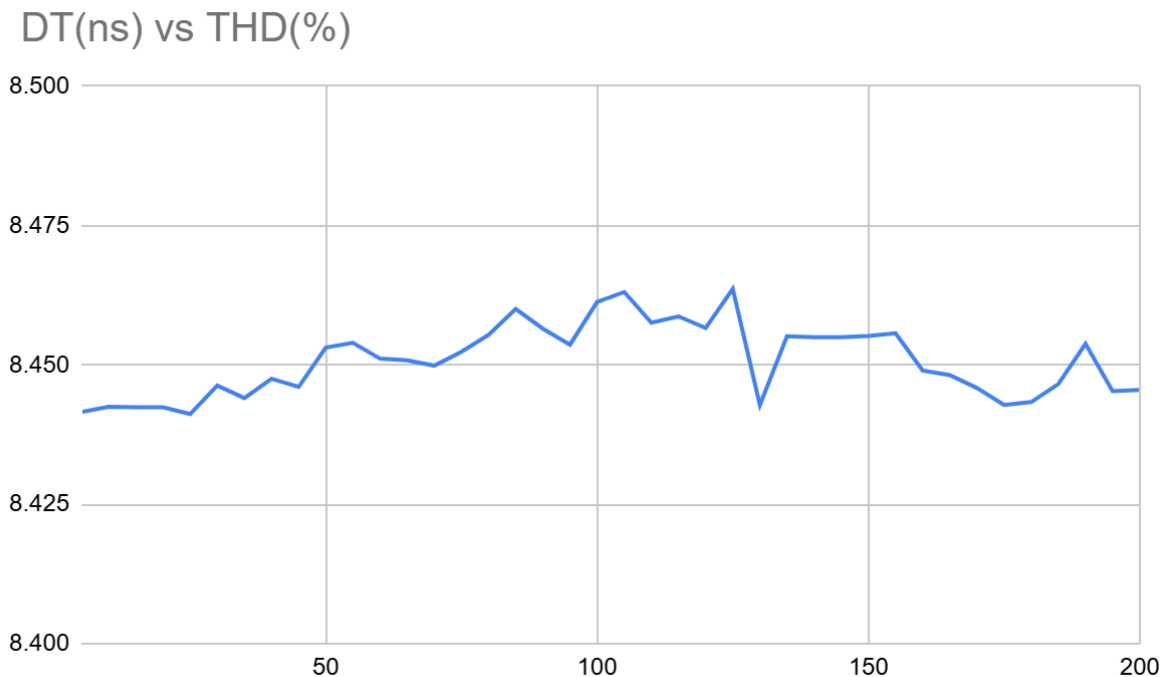


Figure 5. Total THD at the filtered output versus dead-time (5–200 ns, 40 runs)

Table 3. List of all THD (%) for each dead-time value

Dead-time (ns)	Total THD (%)
5	8.441560
10	8.442515
15	8.442414
20	8.442391
25	8.441188
30	8.446295
35	8.444060
40	8.447521
45	8.446055
50	8.453118
55	8.453961
60	8.451127
65	8.450822
70	8.449879
75	8.452372
80	8.455412
85	8.460062
90	8.456510
95	8.453636
100	8.461298
105	8.463085
110	8.457592
115	8.458708

120	8.456619
125	8.463662
130	8.442824
135	8.455138
140	8.454969
145	8.455221
150	8.455695
155	8.449006
160	8.448169
165	8.445858
170	8.442830
175	8.443343
180	8.446587
185	8.453788
190	8.445295
195	8.450085
200	8.445506

4. Discussion

With the absence of a clear threshold - a flat sharp progression of approximately 8.44% to 8.46% between 5ns to 200ns was instead present - the results conducted by the modified Class-D amplifier circuit did not support the hypothesized claim.

Several factors could explain the outcome. First, the dead time tested (between 5ns and 200ns) may have been too little to meaningfully show a threshold distortion. In a real switching converter, distortion effects may only be statistically significant at dead time values substantially larger than 200ns. Second, the gate used in this experiment was highly simplified (it was used as an ideal comparator rather than a real driver IC), preventing it from having realistic rise and fall times. A real driver can interact with the dead time values so easily that the simplified driver simply cannot,

altering the effect of the original hypothesized prediction [3]. Third, the fixed resistive load does not capture the frequency dependence of a real speaker, which could have affected the outputs of the dead time values [2]. Finally, dead-time was added as a voltage offset in the computer, so the actual time gap between the gate signal is estimated rather than measured.

With that being said, these limitations suggest that the absence of a threshold effect, does not rule out the existence of a threshold effect on a real Class-D Amplifier. Work in the future can improve upon this by extending the dead time value beyond 200ns, incorporating a more realistic driver, and testing if the hypothesized relationship would emerge under real physical conditions [7].

5. Conclusion

The study examined if the dead-time in a simulated half bridge Class-D Amplifier causes total harmonic distortion to remain flat before rising sharply past a threshold. Across a dead time sweep between 5ns to 200ns using a MOSFET based circuit, THD stayed within a narrow range of 8.44% and 8.46%. The data showed no clear trend or threshold behavior. The results of the experiment do not support the original hypothesis, but it also does not rule out the effect of threshold on real life hardware; it suggests a wider dead time range, a more realistic gate drive, and a larger range of conditions, could have been necessary to see a significant effect. Future work regarding this simulation, could extend into determining existing nonlinear relationships between dead time and distortion under more physically representative conditions.

Acknowledgments

I thank Professor Shoba Krishnan of Santa Clara University for mentoring this project. Her guidance on the research direction, and her suggestion to examine second-order effects in the circuit, shaped the final simulation.

AI-Use Statement

Artificial intelligence (Claude) was used during this project to debug the LTspice circuit, suggest paper structure, suggest edits on portions of the text, find sources, and generate Figures 1 and 2. The topic and hypothesis were developed with AI assistance. simulation design, circuit, data collection, and analysis were carried out by the author. The author wrote and reviewed all the text and takes responsibility for the content.

Data Availability

The simulation data, total THD for all 40 dead-time values, are provided in Table 1. The LTspice netlist is provided in Appendix A. Additional data is available from the authors LTSpice simulation.

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Appendix A. LTspice netlist

```
* C:\Users\arjun\OneDrive\Documents\LTspice\Draft1.asc
* Generated by LTspice 26.0.2 for Windows.
V3 0 N003 15
V4 0 N002 -15
L1 N004 N005 100μ Rser=1m
C1 N005 0 1μ
R1 N005 0 8
Vtri tri 0 PULSE(-1 1 0 9.5u 9.5u 0.001n 20u)
Vaudio audio 0 SINE(0 1 1k)
B$Vpwm pwm 0 V=IF(V(audio)-V(tri) > {DT/19u}, 5, 0)
B1 N001 0 V=IF(V(tri)-V(audio) > {DT/19u}, 5, 0)
M1 N003 pwm N004 N004 IRFH5302D
M2 N002 N001 N004 N004 IRFH5302D
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\arjun\AppData\Local\LTspice\lib\cmp\standard.mos
.model SWMOD SW(Ron=0.1 Roff=1Meg Vt=2.5)
.step param DT 5n 200n 5n
.four 1k V(N005)
.tran 4m
.backanno
.end
```

